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Prototype of a 250 µm Pitch 36-channel SiPM Array Using SOI Technology for Photon Counting CT

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Outline

- ✓ Introduction
- ✓ Device Design
- ✓ Measurement Results

✓ Conclusion

Hard X-ray (20-120 keV) imaging

- Conventional medical X-ray Computed Tomography (CT)
 - Integrate all transmitted X-ray's energy and calculate attenuation coefficients



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- Photon counting Computed Tomography (PCCT)
 - Discriminate each transmitted X-ray's energy and provide spectrum information



→ Attenuation characteristics at each energy depends on materials

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Inspection of material composition in the object by spectrum shape analysis Contrast enhanced image can be achieved at low radiation dose

The principle of X-ray photon counting



Pixel size: One factor that greatly affects count rate performance The smaller pixel size, the less spectra deterioration due to pile up effect

The principle of X-ray photon counting



The principle of X-ray photon counting



A small pixel size is not always desirable since the spectra would be degraded due to the charge sharing, K-escape x-ray, and Compton scattering

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 \rightarrow Target value is 2 Mcps/mm² with pixel size of 0.2-0.5 mm

Indirect conversion detector

• Detector system of clinical X-ray CT : Scintillator + Photo sensor



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- How to achieve X-ray photon counting ?



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Small pixel size availability and high detection sensitivity are required for photo sensor to read light output of sub-mm pitch scintillators

Silicon Photomultiplier (SiPM)

- In order to minimize photo sensor size
- Silicon base sensor has attractive features for small pixel size, • while photo diode has worse sensitivity (no internal gain) toward weak light
- Silicon photomultiplier (SiPM)
- \rightarrow achieves photo electron multiplication characteristics (avalanche) by operating photo diode at higher voltage than breakdown voltage

	Photo Multiplier Tube (PMT)	Silicon PIN Photo Diode (PD)	Silicon Photomultiplier (SiPM)	SiPM PMT
Gain	10 ⁶	1	10 ⁶	PI
Form factor	Bulky	Compact	Compact	
Sensitive to magnetic fields?	Yes	No	No	Light inten +V _D
Noise	Low	Low	High	Quench resist
Rise time	Fast	Medium	Fast	N c c
		Town and		Light e- e- e









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Geiger avalanche multiplication provides large gain comparable to PMT Development of sub-mm pixel SiPM took great interests

Objective

X-ray Photon Counting using indirect detector
 Development of sub-mm pitch Silicon photomultiplier

Requirements			
Pulse resolution time	< 1 µs		
Pixel size	< 0.5 mm		
Detectable light output levels	1000 ~ 2000 photon from scintillator (GAGG:Ce)		
Multiplication Gain	10 ^{5~7}		



Development of low noise, fast and high sensitivity photo sensor under 1 us pulse resolution time, sub-mm pixel size and high sensitivity are needs to be achieved

Device Design

Silicon on Insulator (SOI)-SiPM

For monolithic sensor design including SiPM and processing electronics....

- Silicon on Insulator (SOI)
 - Semiconductor wafer technology that separate circuit layer from bulk layer by buried oxide layer
 - By using bulk layer as detector, <u>3-D integrated system</u> can be achieved



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SOI provides 3-D monolithic integrated SiPM with readout circuit Smaller pixel size and fast electronics will be achieved **Device Design**

Sub-mm pitch SOI-SiPM prototype

36 CH SiPM Array was designed and fabricated by 0.2 μm SOI process (LAPIS)

- Total Size: 1500 x 1500 μm^2
- Single channel (Pixel)
 - Num. of microcells: 81 (9 x 9)
 - Channel pitch: 250 x 250 μm^2
- Single microcell
 - microcell size: $27.52 \times 27.52 \ \mu m^2$
 - Active area: 15 x 13 μ m²
 - Quench : 200 kohm









For feasibility study of signal readout, two read out methods selectable design was applied

Cathode : 36 CH discrete negative signal readout (36 line)

Anode : X-Y strip line readout (12 line)

→ Applicable to various fields (Not only PCCT, but also PET or LIDER...)

Current-Voltage characteristics (Position dependency)

- Measured breakdown voltage and leak current distribution among 36 CH
- 50 mV step, Temperature: 25 °C
- Breakdown voltages were extracted by using relative derivative methods



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Average breakdown voltage of 45.66 V (±100 mV) was measured among 36 CH Dark current was 8 nA (±3 nA) at breakdown voltage

Current-Voltage characteristics (Temperature dependency)

- Temperature dependency of leak current was measured at 1 CH
- 50 mV step



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- Temperature dependency of leak current was measured at 1 CH
- 50 mV step



Leak current and breakdown voltage increase with temperature Temperature dependency of breakdown voltage was 35 mV/°C

Capacitance-Voltage characteristics

- To estimate achievable gain from cell capacitance
- CV were measured three times, and average value was plotted
- 1CH : 81 cell
- Measured by using Keithley 4200SCS





Parasitic capacitance between adjacent wires : 1.3 pF @ CH1



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Cell capacitance of 20 fF was measured \rightarrow Achievable gain at 47 V: 20fF x 1.02 V /1.6e-19 = 127,500 \approx 10⁵

Gain evaluation

- Output Charge per cell Q = $\int [Waveform V / Oscillo input Z] dt / 81 cell$
- Gain = Q / 1.6e-19, 510 nm wavelength laser (1 kHz, intensity 15)
- Oscilloscope: LeCroy waverunner (10GS/sec, bandwidth 1GHz)
- HV: Keithley 6517A Room Temp. = 25 degC
- Oscilloscope input : DC 50 ohm // SiPM load resistance 1k ohm



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Multiplication gain of 10⁵ with fast recovery time under 20 ns was measured at over voltage = 1 V

→ Matches to expected gain from cell capacitance

Dark count rate (DCR)

- Number of dark count pulse was recorded for 300 us × 3 times
- Temperature was controlled by temperature control box (ESPEC)
- Waveforms were acquired by oscilloscope (Lecroy 10GS/s, Bandwidth 200MHz)
- Preamplifier (KETEK Evaluation Kit, Gain=13) was connected to anode of SOI-SiPM
- Over voltage = Bias voltage breakdown voltage



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Photon spectrum (Preliminary)

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Single photon level was roughly discriminated

Conclusion

- In order to develop Photon Counting CT (PCCT),
 Sub-mm silicon photo-multiplier was designed by using SOI wafer
- Fast recovery time of less than 20 ns and avalanche multiplication gain of 10⁵ was acquired by operating over breakdown voltage of 1~2 V
- → Sufficient levels to use for PCCT

Future works

- High dark count rate (>1 Mcps) needs to be reduced
- → Optimization of sensor structure or changing wafer profile Threshold adjustable readout circuit design is desirable for dark count elimination

Supplemental slide

Device simulation

• Guard ring structure contributed to enlarge high electric field area, and increase breakdown voltage



Comparison between simulation and measurement results

- Guard ring effect was inspected using test chip
- Measurement results also showed high break down voltage at guard ring type

