



# Development and performance of double SOI pixel sensors

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HSTD11 and SOIPIX2017  
10-15 Dec. 2017  
OIST

Thursday, 14 Dec. 2017  
14:00-14:20

# Outlines

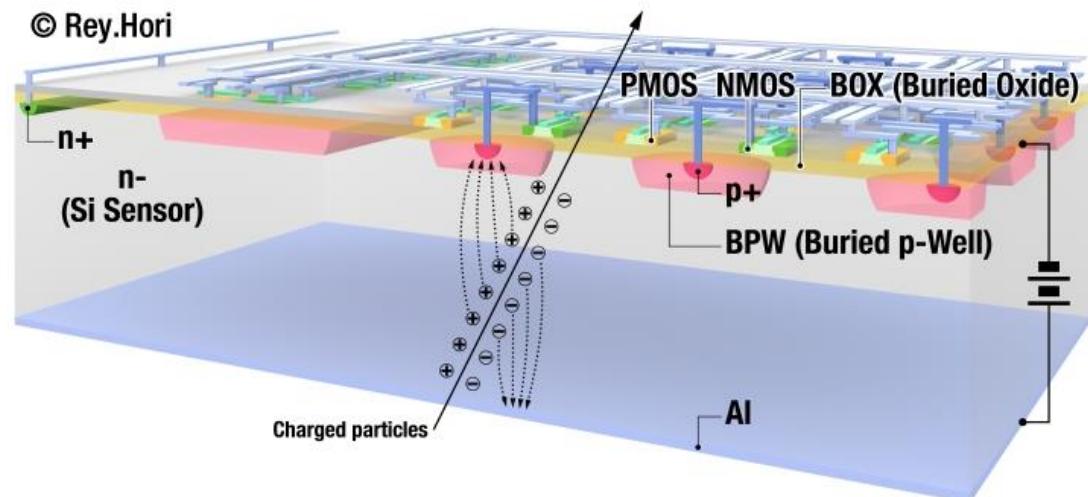
Introduction (skip)

Single SOI (SSOI) and Double SOI (DSOI)

Evaluation test:

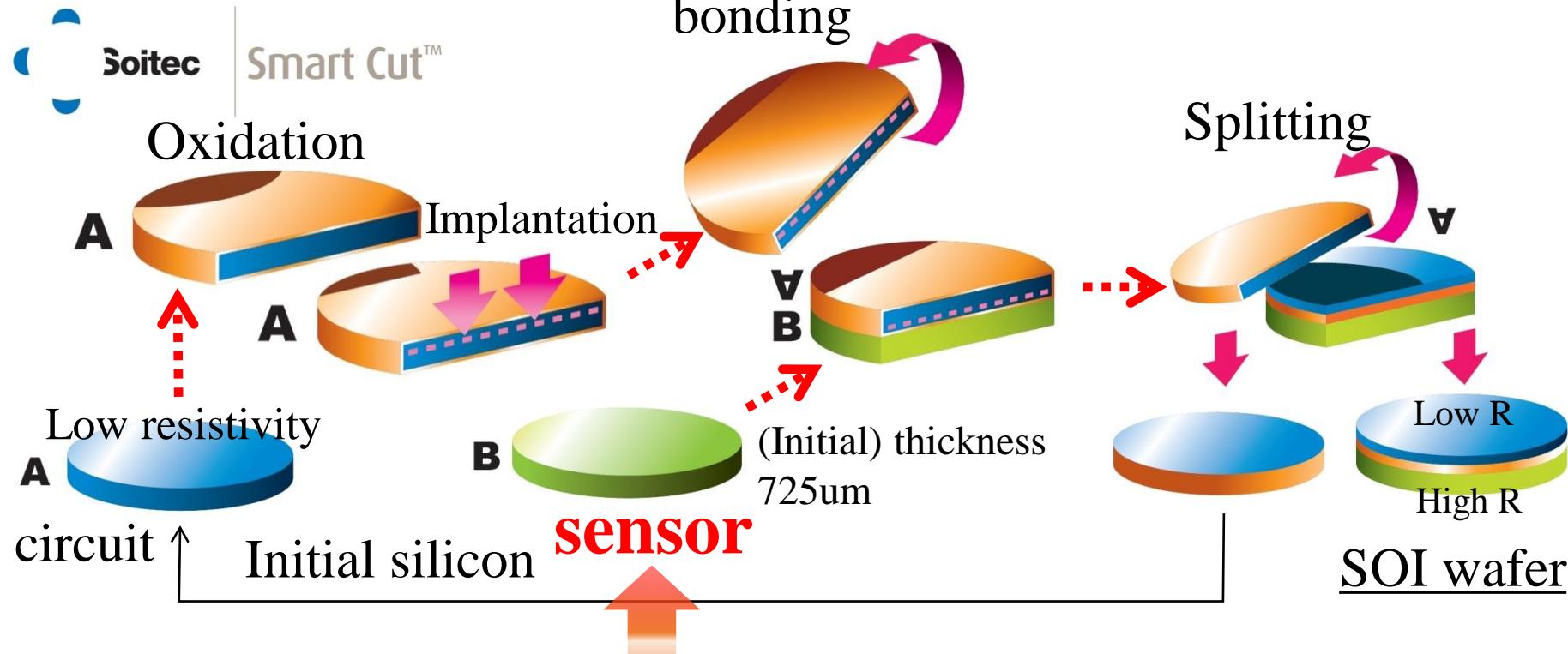
- Breakdown voltage
- Sensor gain
- Leakage current
- Energy resolution
- Readout noise

Summary and future plan



# SOI wafer for monolithic sensor

Smart cut™ by Soitec



High Resistivity Silicon:

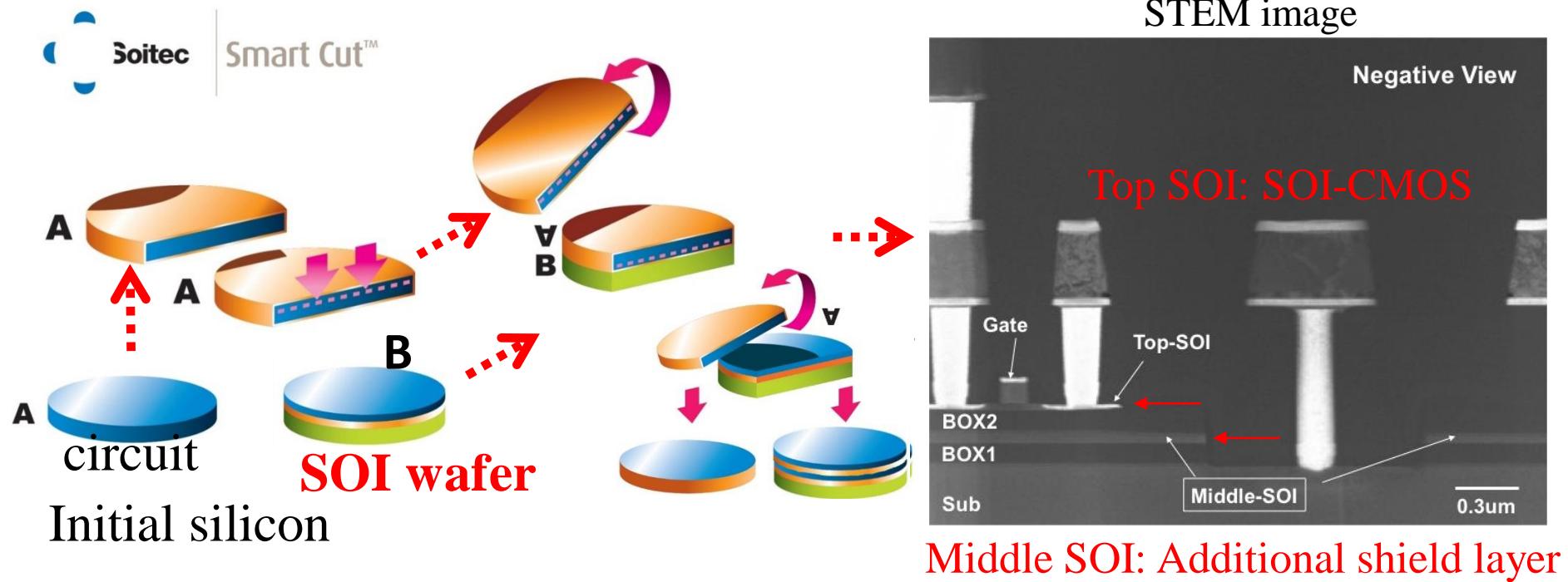
N-type Czochralski (NCz), 0.7 kOhm-cm, thinned to 300  $\mu\text{m}$ -thick

N-type Float Zone (NFZ), 2-7k Ohm-cm, thinned to 500  $\mu\text{m}$ -thick

P-type Czochralski (PCz), 1k Ohm-cm, thinned to 300  $\mu\text{m}$ -thick

P-type Float Zone (PFZ), 2-40k Ohm-cm, thinned to 500  $\mu\text{m}$ -thick

# Double SOI (DSOI) pixel sensor



Double SOI N-type sensor (2011-2013) MPW11(MX1501),12-1(MX1542),12-2(MX1594)

Double SOI P-type sensor (2014-) MPW13-1(MX1655), MPW13-2(MX1711),  
MPW14(MX1786), MPW15(MX1850), MPW16(MX2040), MPW17-1(MX2166),  
MPW17-2()

Utilization of double SOI: we can solve

## Major issues

Back-gate effect

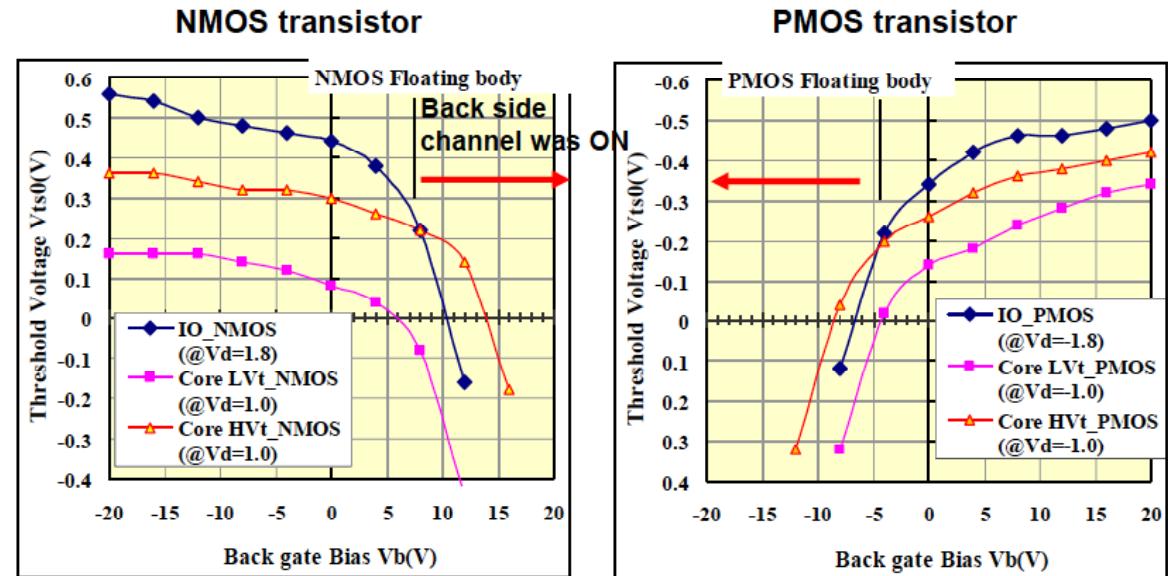
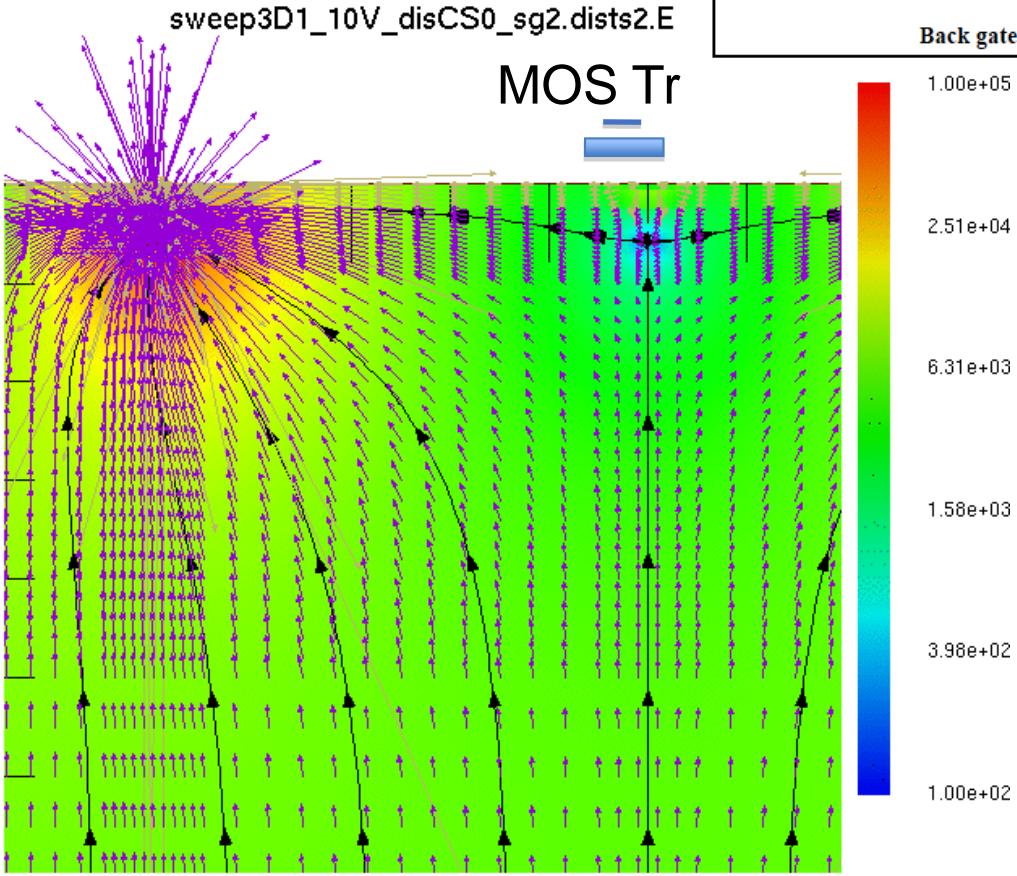
Crosstalk

Radiation tolerance → Hara-san's talk

# Back-gate effect

TCAD simulation  
HyENEXSS (TAC, Japan)

Potential distribution



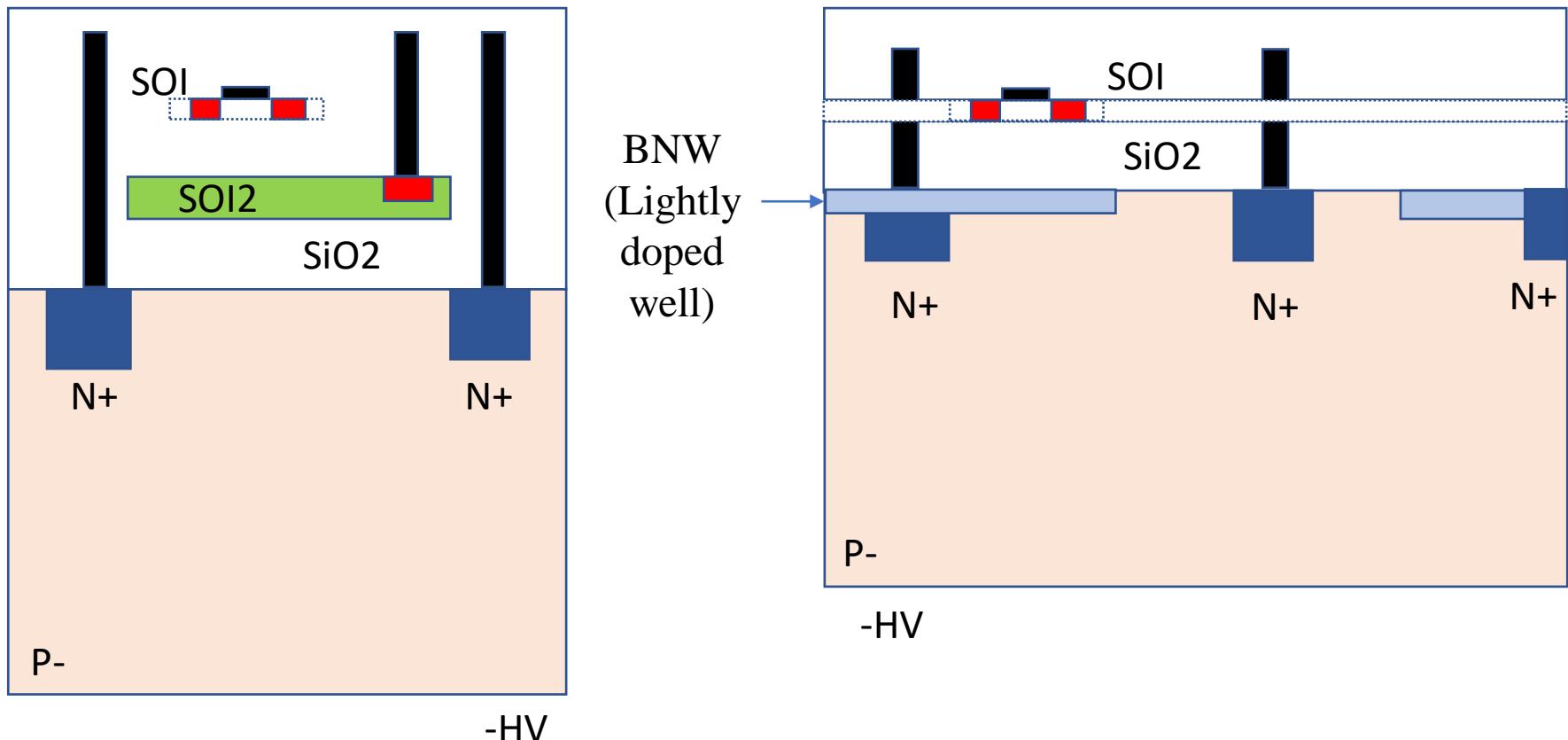
Copyright 2007 Oki Electric Industry Co.,Ltd

Threshold Variation

Substrate voltages act as back gate, and change transistor threshold.

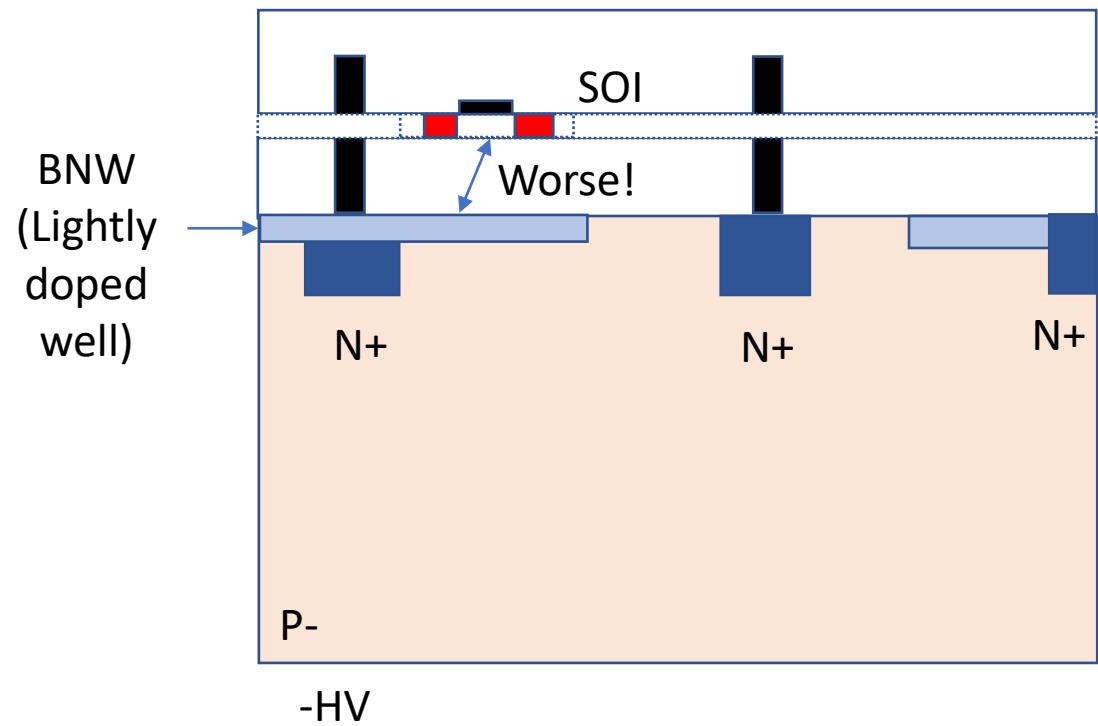
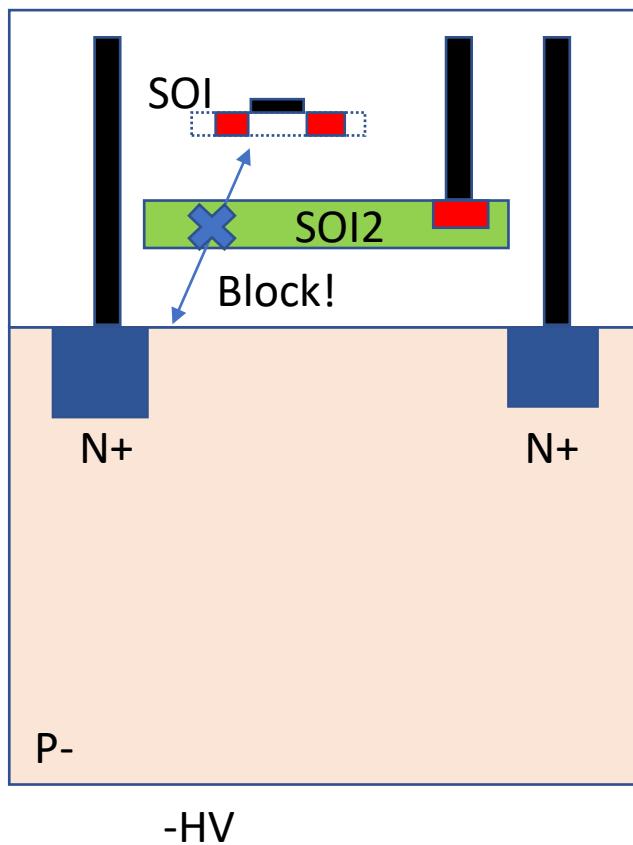
# Suppression of the back-gate effect

Two methods (DSOI, BNW)

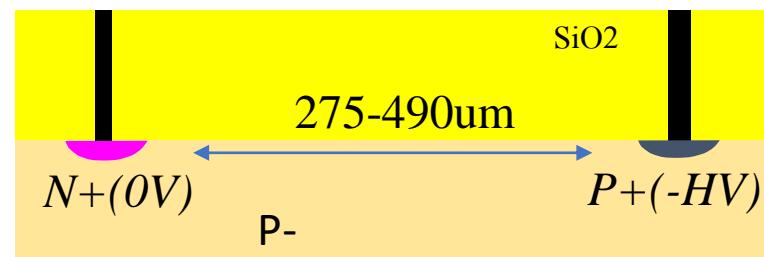
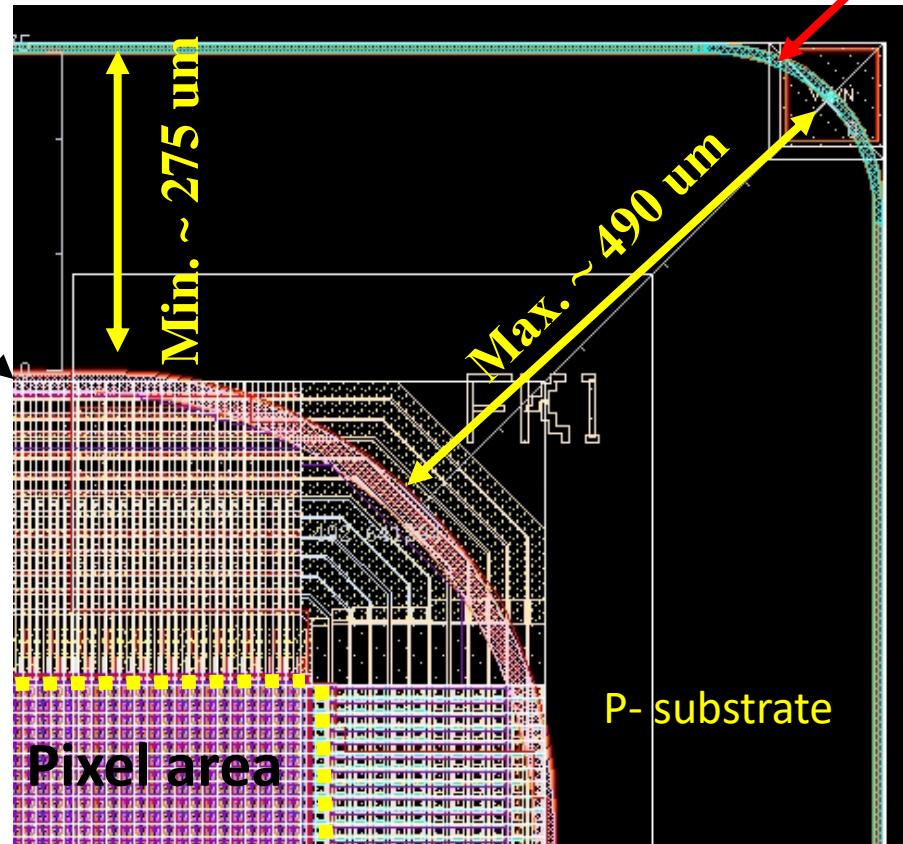
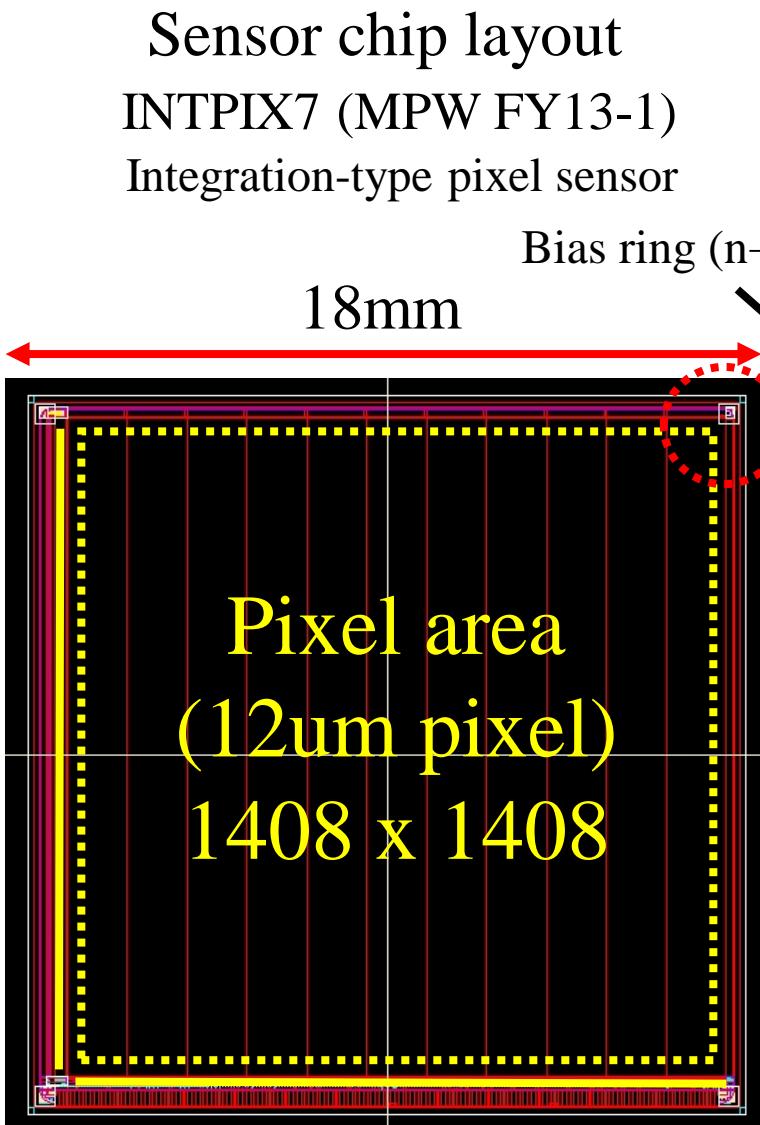


# Suppression of cross-talk

Crosstalk can be reduced by middle SOI



# Improvement of breakdown voltage in DSOI



Edge of the chip (side view)

The corner shape is the same in INTPIX7&8

# Breakdown voltage study (INTPIX8, SSOI)

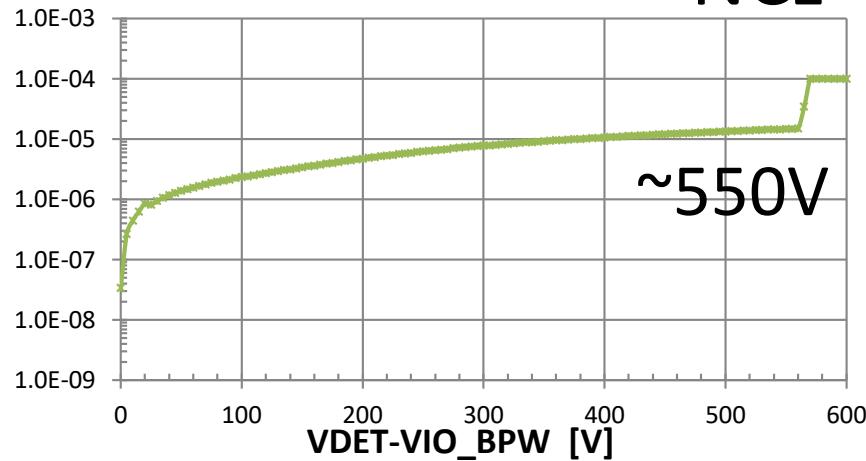
@25deg.

KEITHLEY2410

VDET-VIO\_BPW I-V

NCz

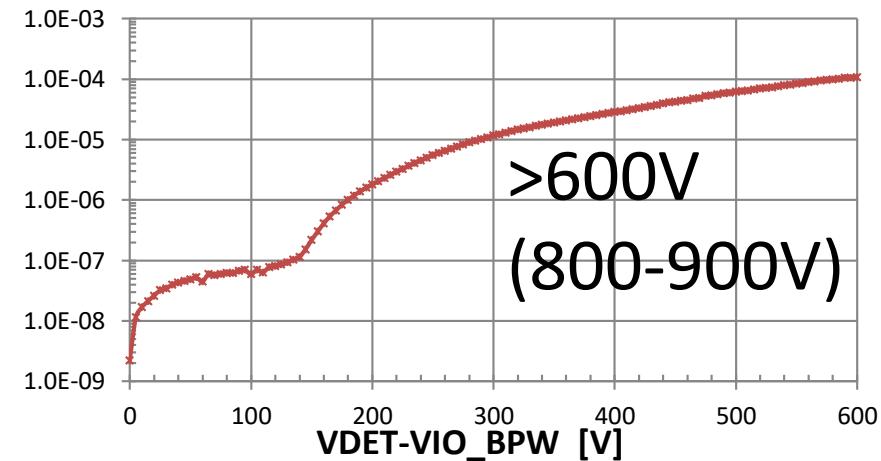
VDET[I]



VDET-VIO\_BPW I-V Curve

NFZ

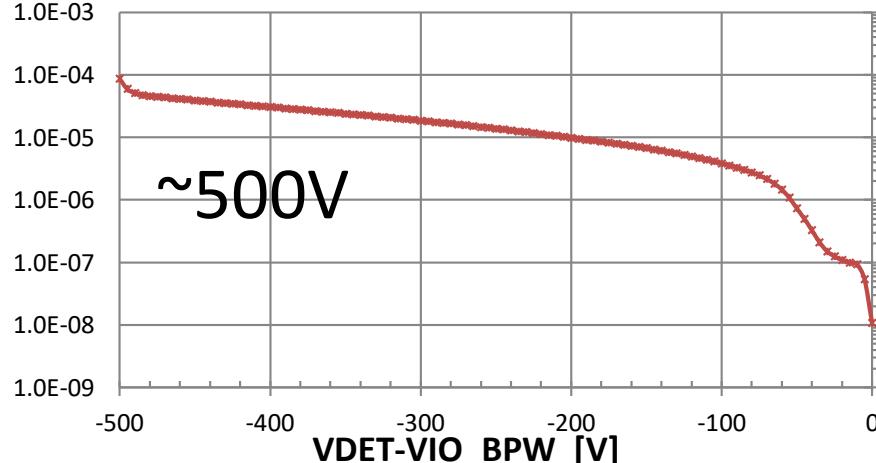
VDET[I]



VDET-VIO\_BPW I-V

PFZ

VDET[I]



Full depletion voltage

NCz 0.7 Ohm cm → ≈ 400V@300um

NFZ 4 kOhm cm → ≈ 200V@500um

PFZ 25 kOhm cm → ≈ 200V@500um

\*DSOI(p) 1kOhm cm → > 500V@300um!

(calculation)

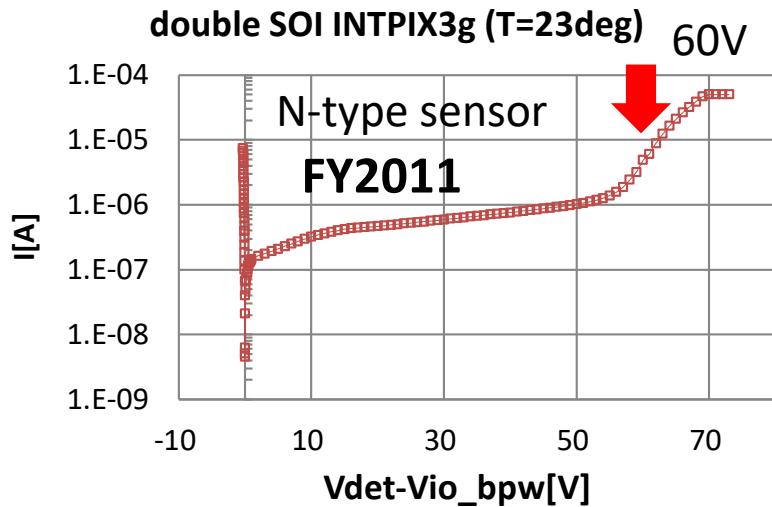
→ Thinned to 70um → <200V

# Breakdown voltage: double SOI sensor I-V measurement

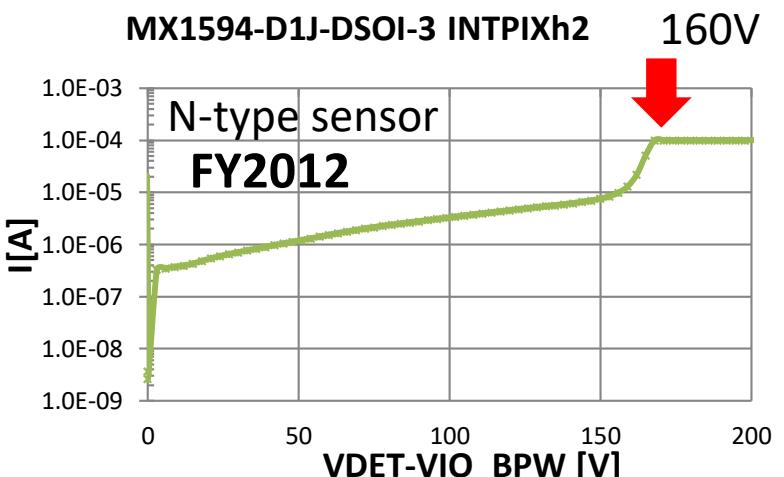
(Development history)

At room temp.

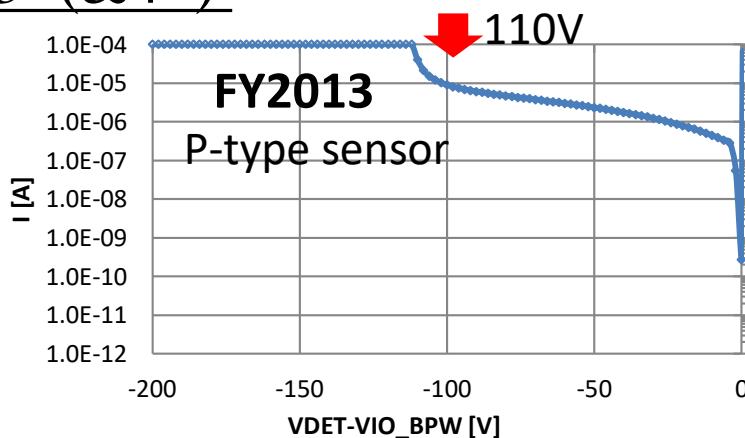
## Double SOI 1<sup>st</sup> trial



## Double SOI 2<sup>nd</sup> trial



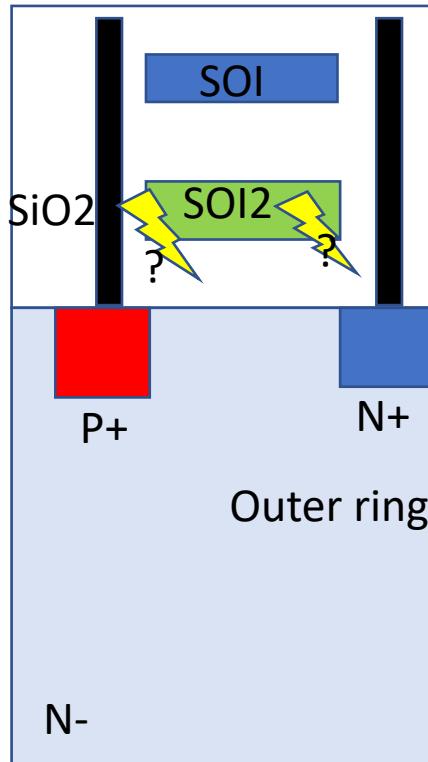
## 3<sup>rd</sup>(&4<sup>th</sup>) MX1655D-1J-DSOI INTPIX7



**Process improvement was required.**

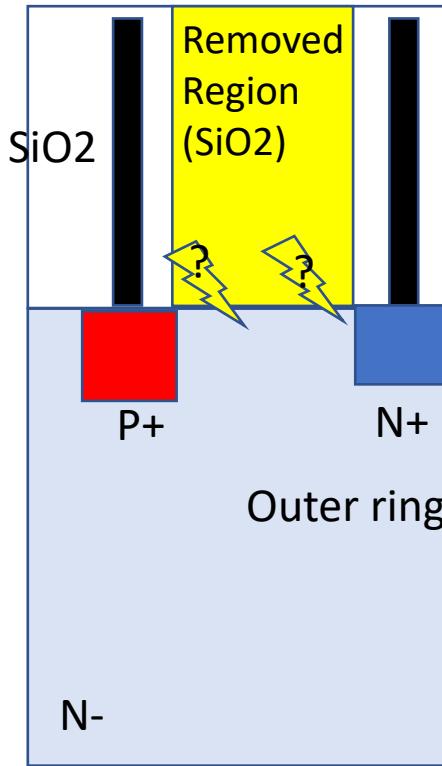
# Improvement of SOI process for DSOI

First ver.

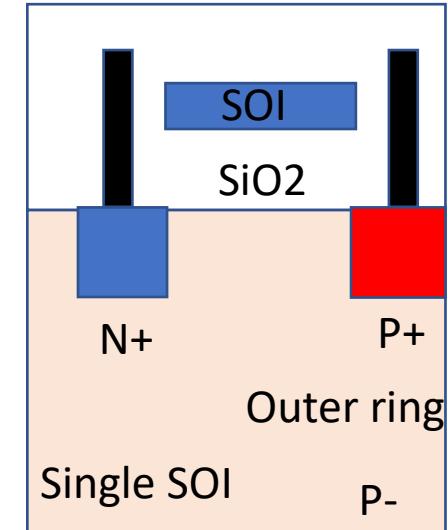


Floating SOI2 might  
be problem

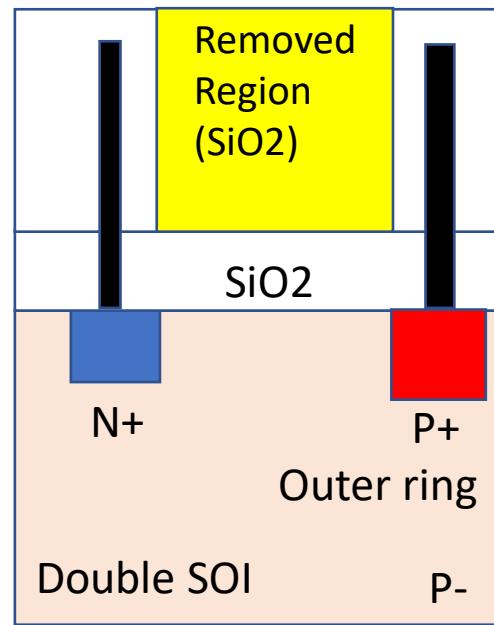
Second ver.  
Remove SOI2  
and the bottom SiO<sub>2</sub>



Si/SiO<sub>2</sub> interface  
has problem?



Current ver.

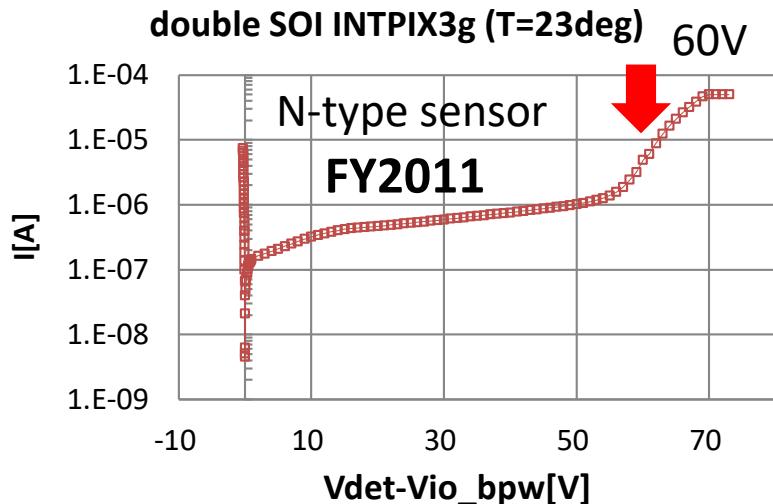


Remove SOI2 & keep Si/SiO<sub>2</sub>  
at the bottom

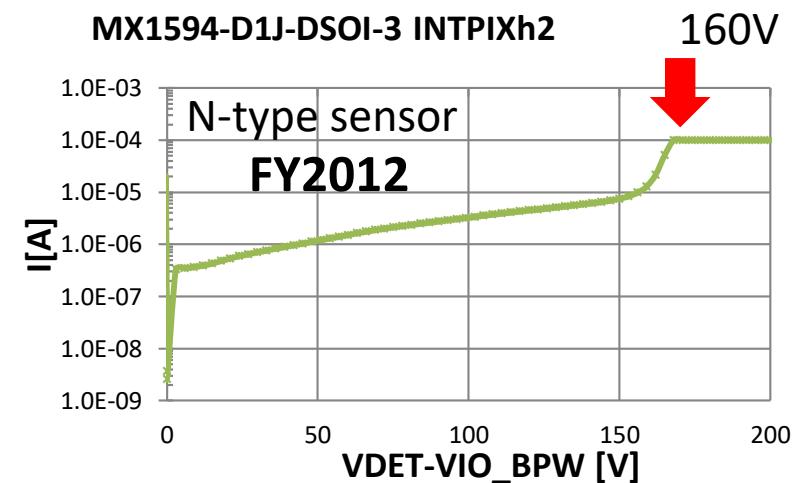
# Breakdown voltage: double SOI sensor process (improved)

At room temp.

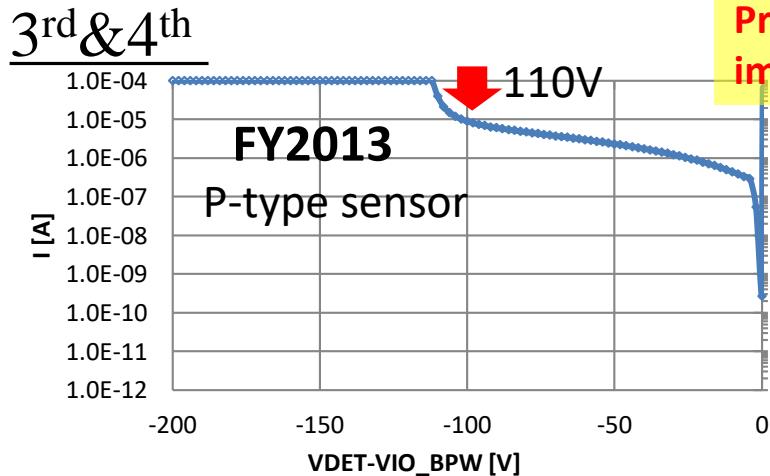
## Double SOI 1<sup>st</sup> trial



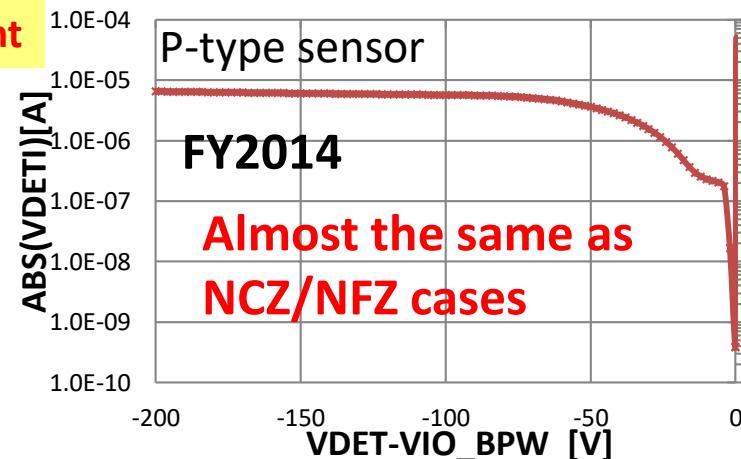
## Double SOI 2<sup>nd</sup> trial



MX1655D-1J-DSOI INTPIX7



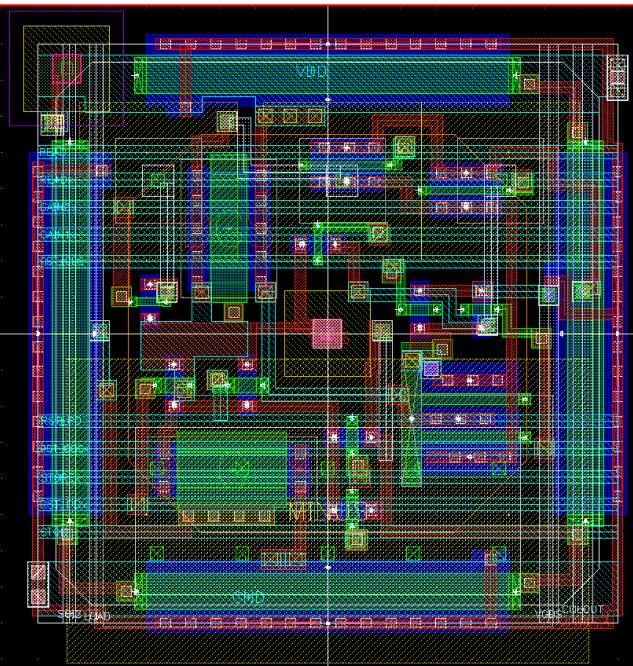
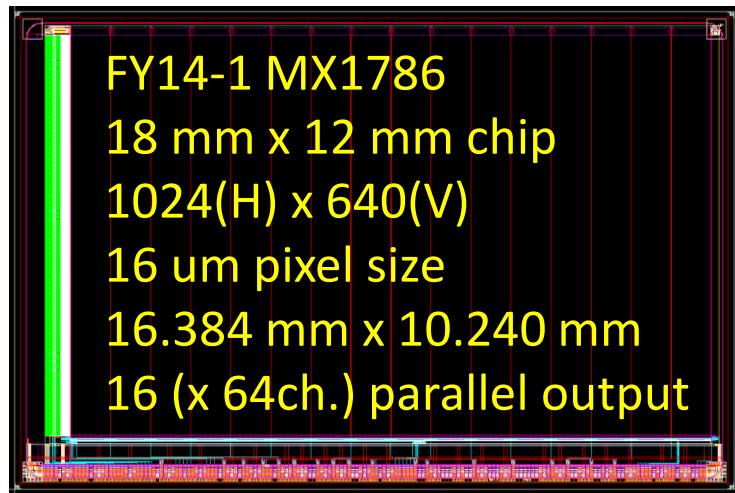
5<sup>th</sup> MX1786D-1J-DSOI INTPIX8



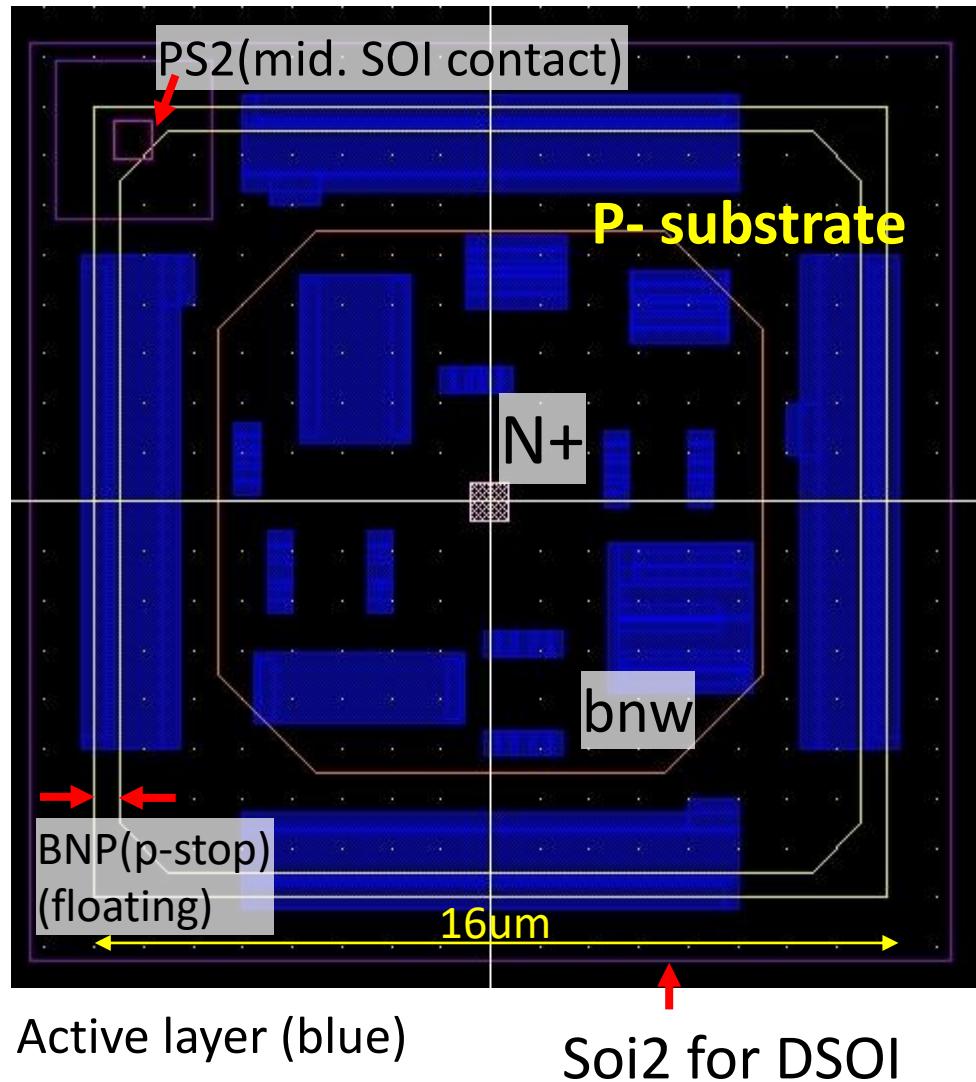
Recover breakdown voltages: comparable to the single SOI case

Evaluation test – Sensor gain, pixel leak current, Energy resolution, readout noise

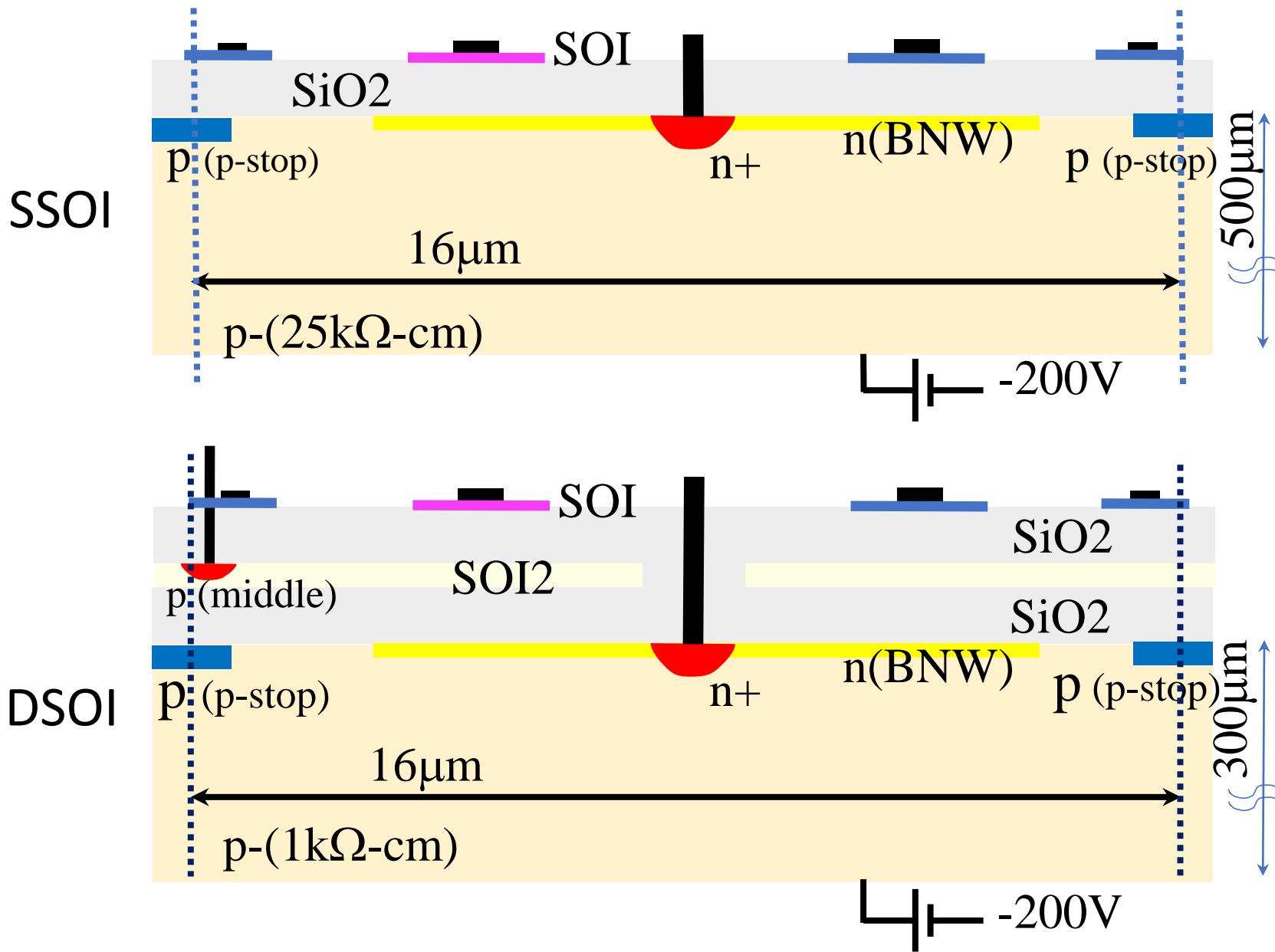
### Integration-type p-type SSOI/DSOI sensor - INTPIX8 (FY14-1)



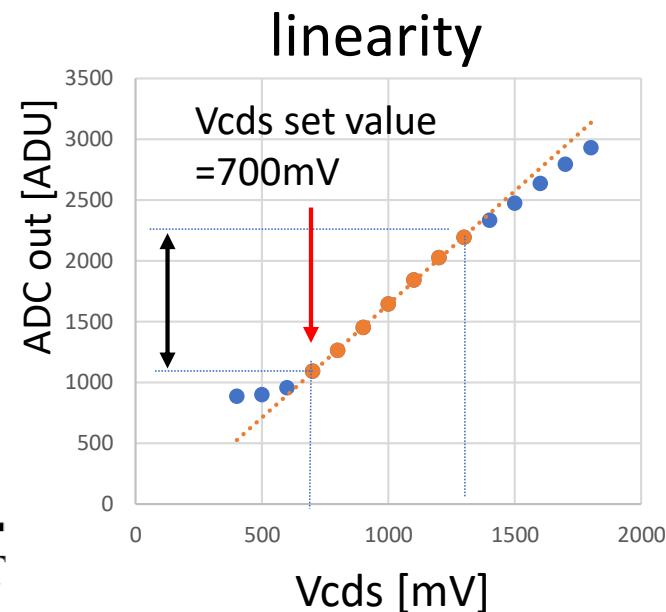
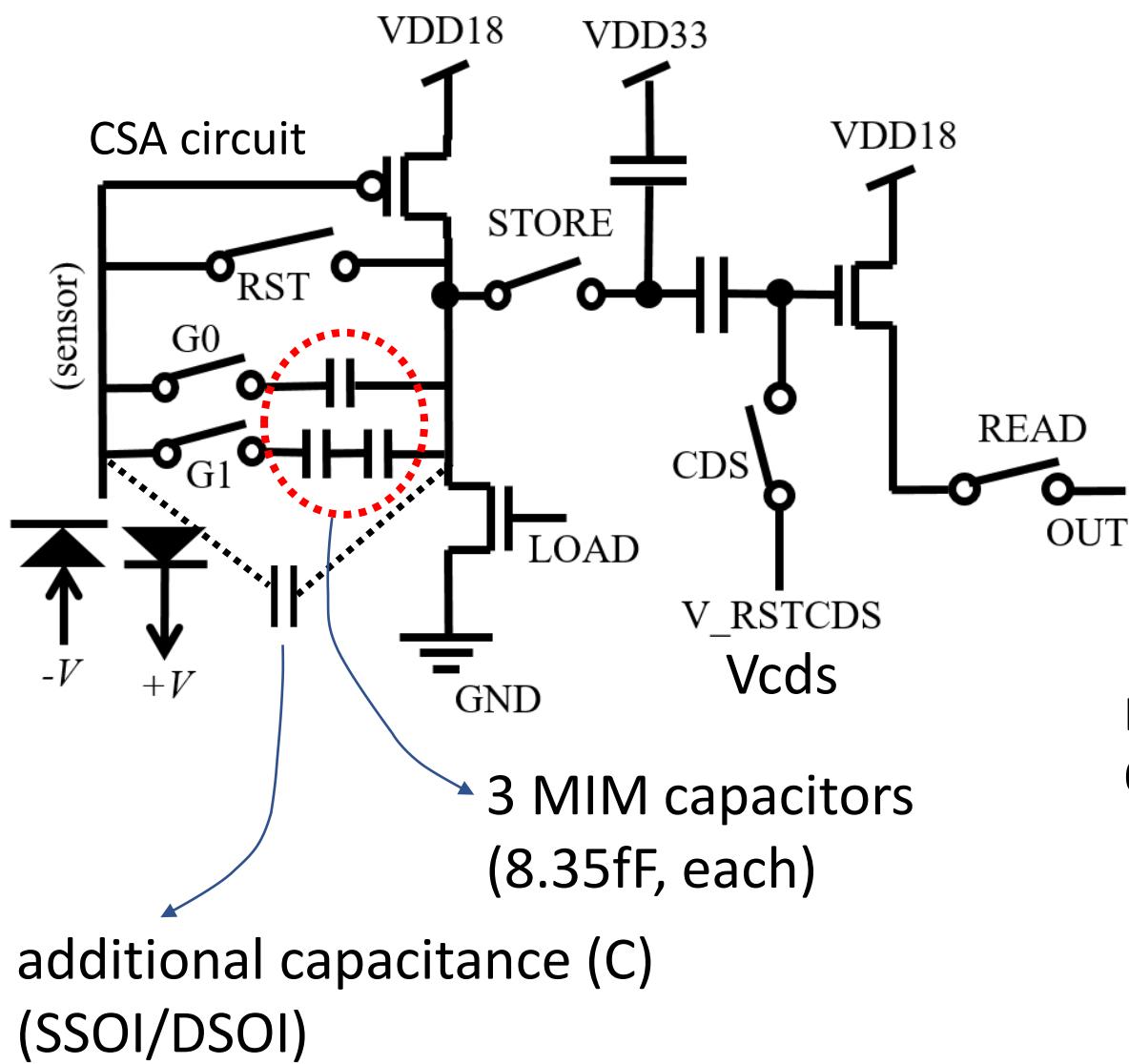
Pixel layout 16 x 16 um



# Side view of INTPIX8 pixel layout

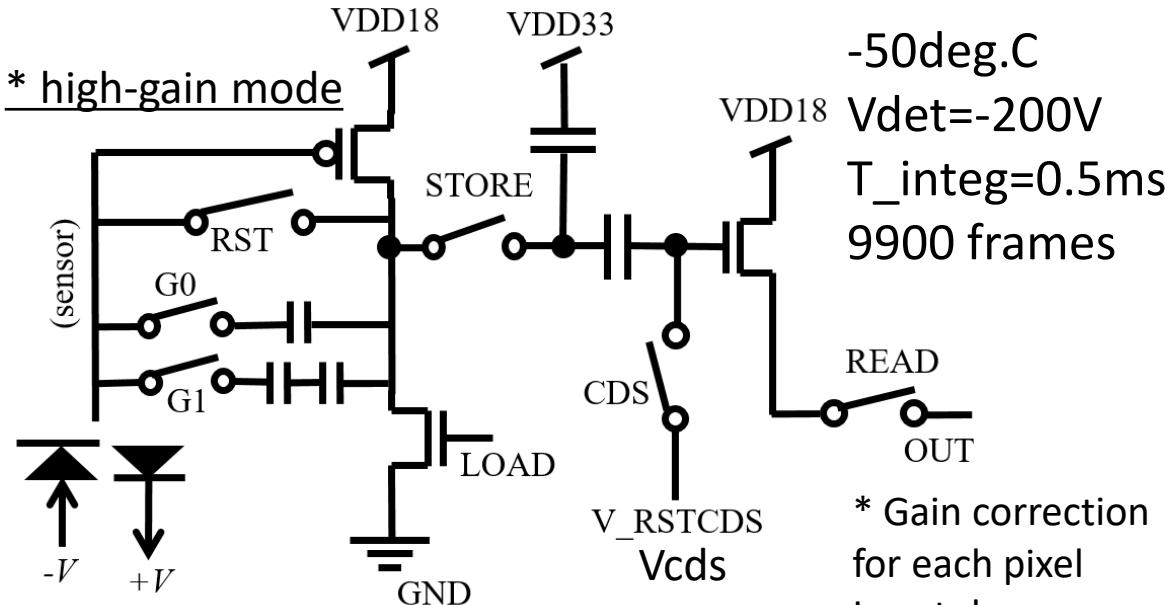


# Pixel circuit of p-type SSOI/DSOI INTPIX8



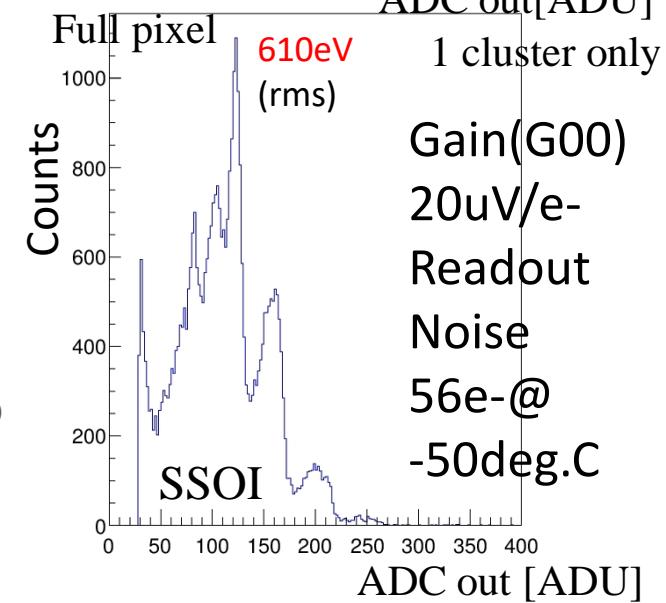
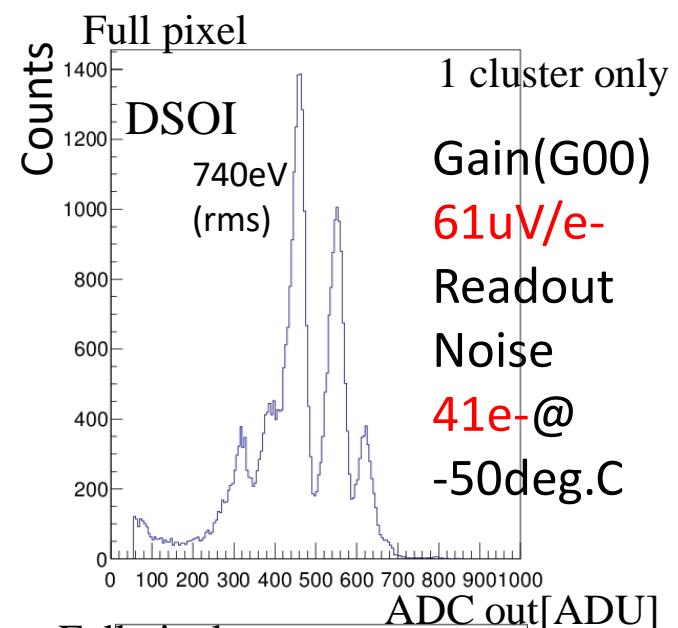
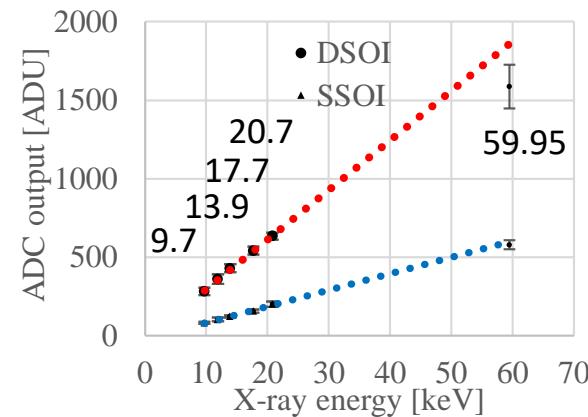
Linear range (dynamic range)  
600mV: 1100 ADU

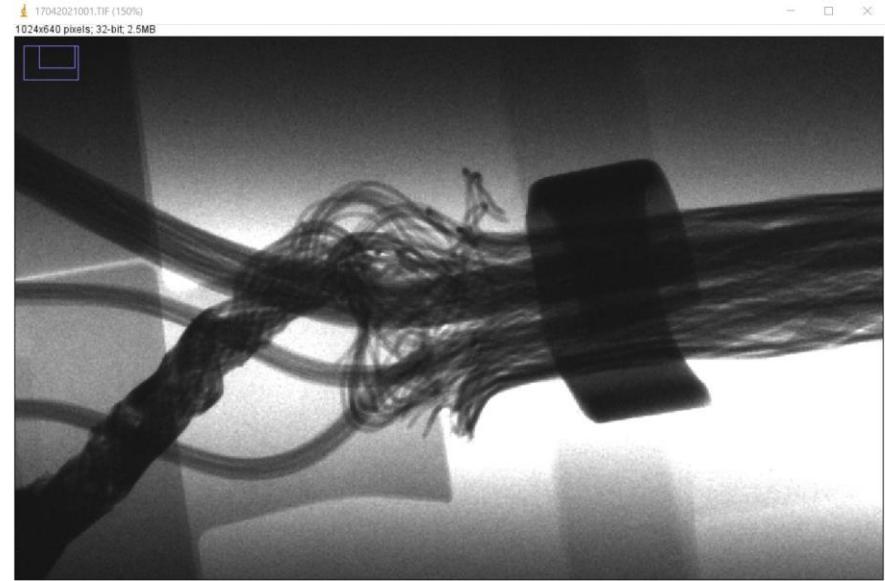
# Am-241 spectra by p-type SSOI/DSOI INTPIX8



Gain setting	Sensor gain [ $\mu\text{V/e}$ ]	Coupling capacitance, C [fF]
G01 in DSOI	10.2	1.67
G10 in DSOI	18.9	1.87
G11 in DSOI	7.58	1.78
G01 in SSOI	7.36	4.81
G10 in SSOI	12.2	6.43
G11 in SSOI	6.07	5.40

G00: all open, G11: all connected

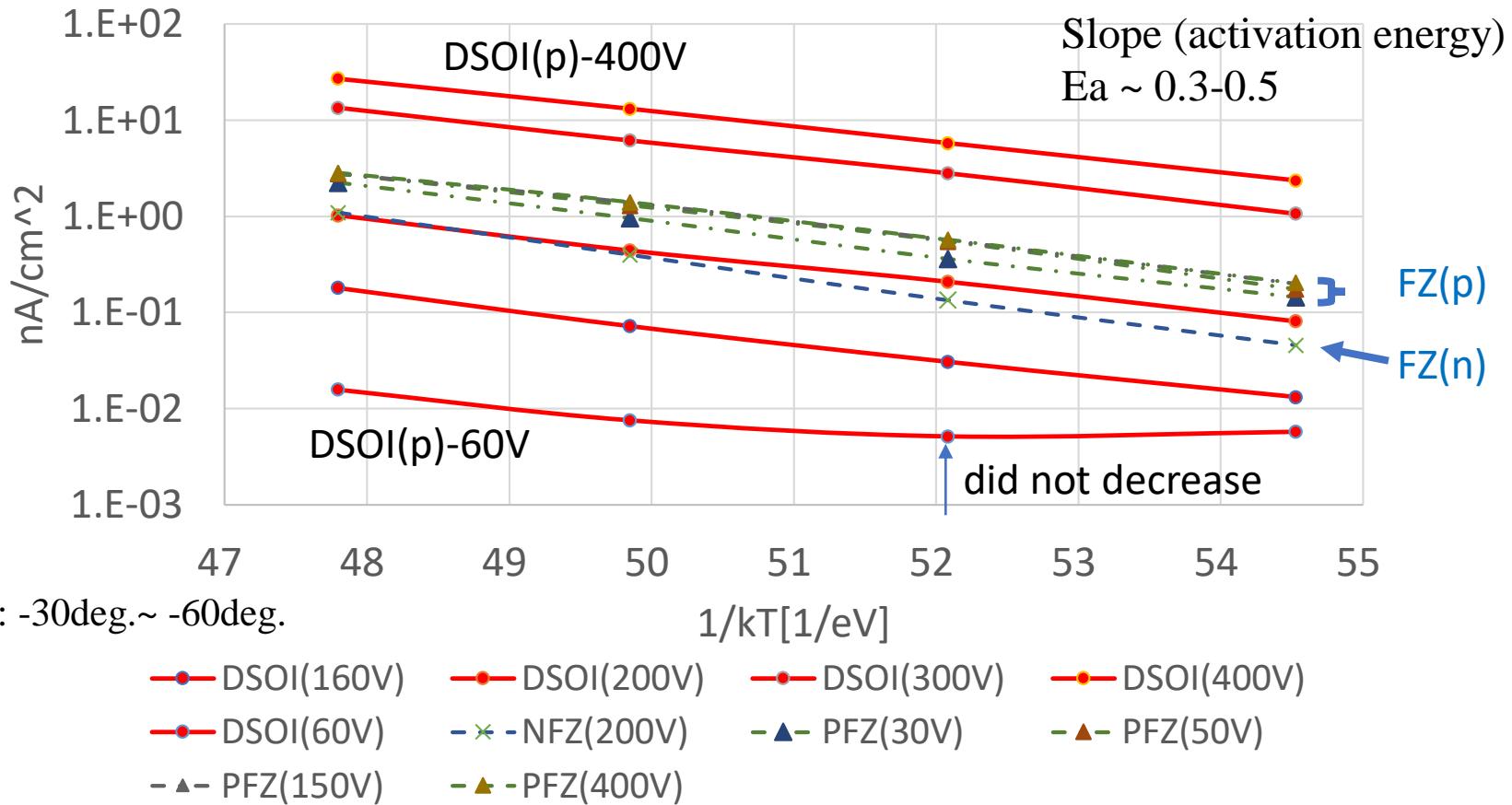




## Pixel leak current of integration-type pixel sensors



# Pixel leak current of FZ(n), FZ(p), and DSOI(p) INTPIX8

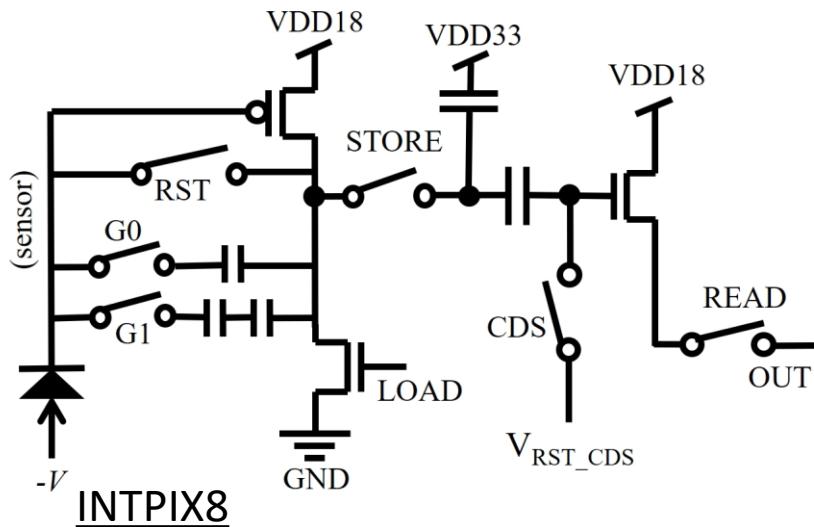
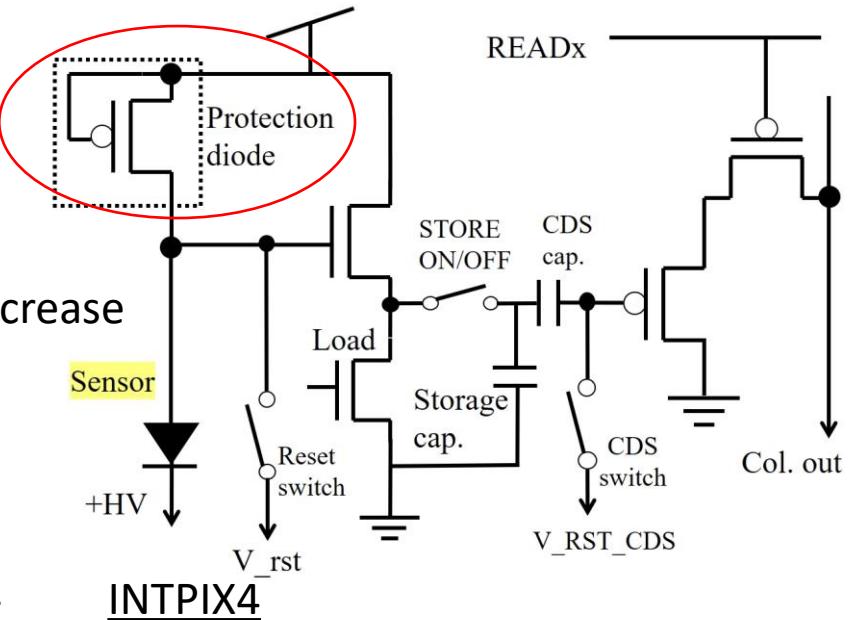
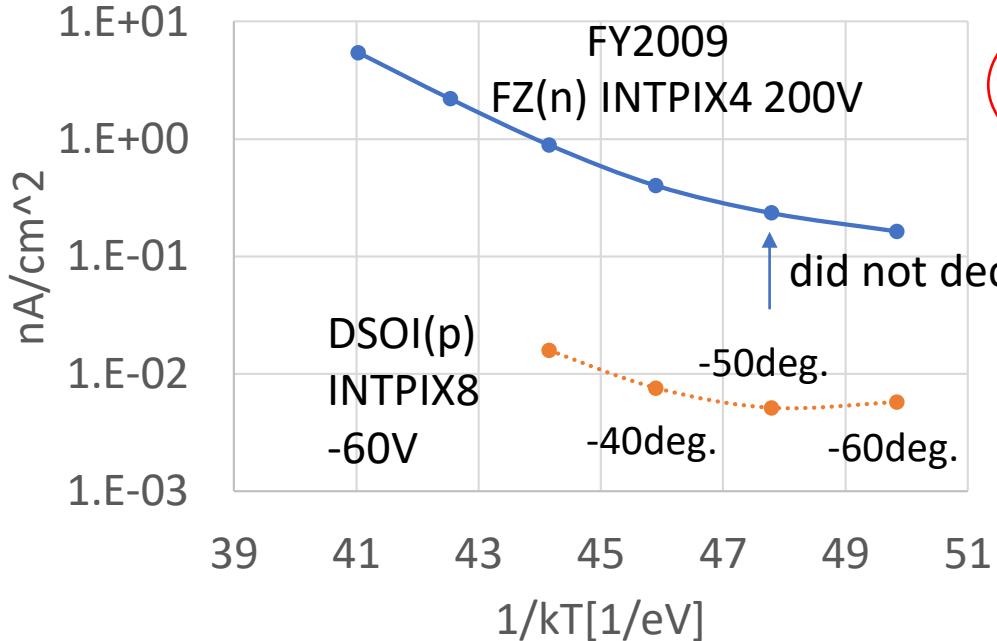


Back bias voltage dependence

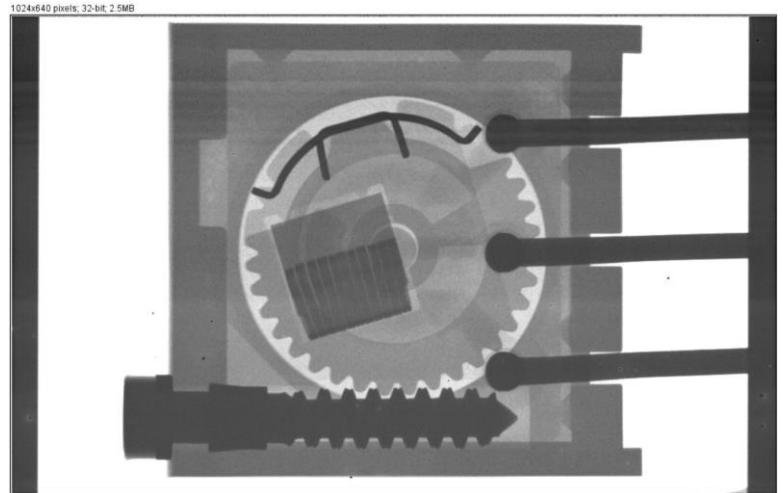
FZ(n,p) : small, larger current

DSOI(p) : large, smaller current with lower voltage

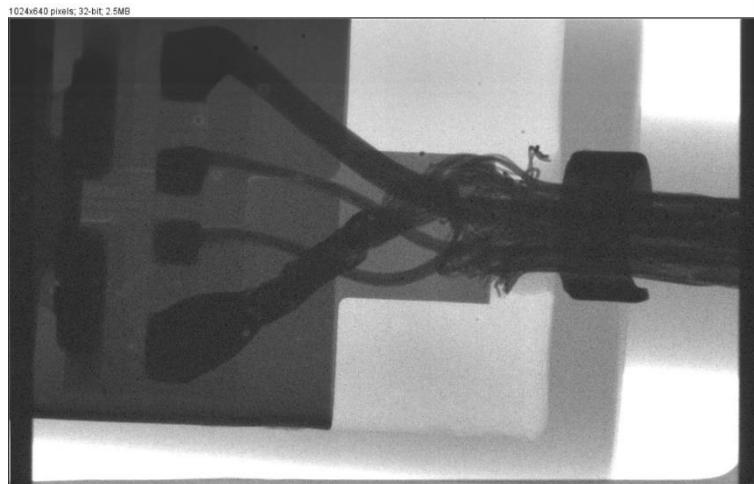
# Pixel leak current of NFZ-INTPIX4 and DSOI-INTPIX8



- Source-follower pixel circuit (INTPIX4)  
Higher leakage current  
Probably because of diode leak (to be confirmed)
- CSA pixel circuit (INTPIX8)  
Lower leakage current but reach the minimum



## Energy resolution and noise (back bias voltage dependence)



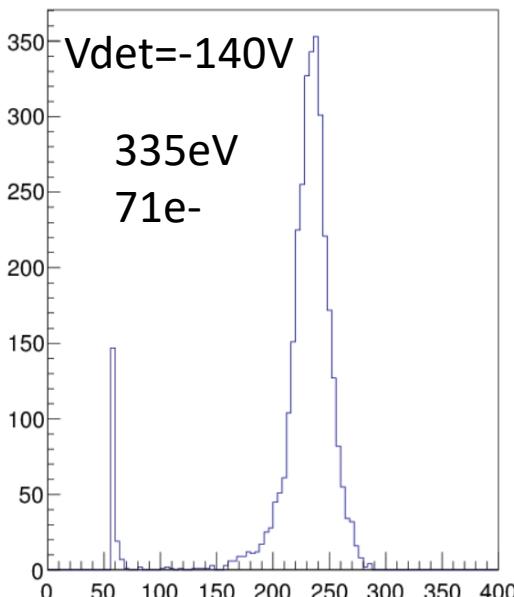
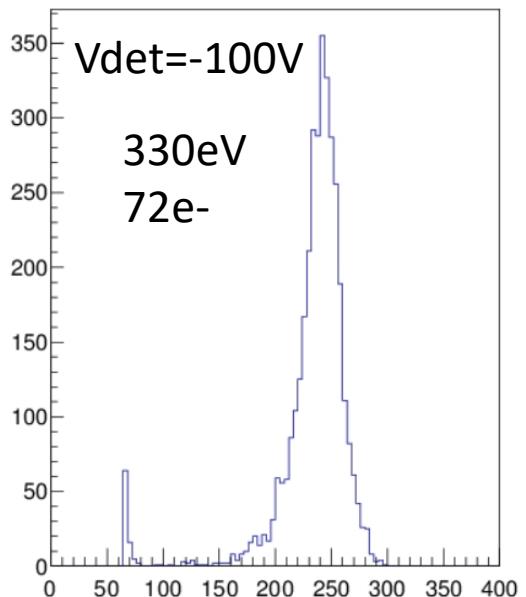
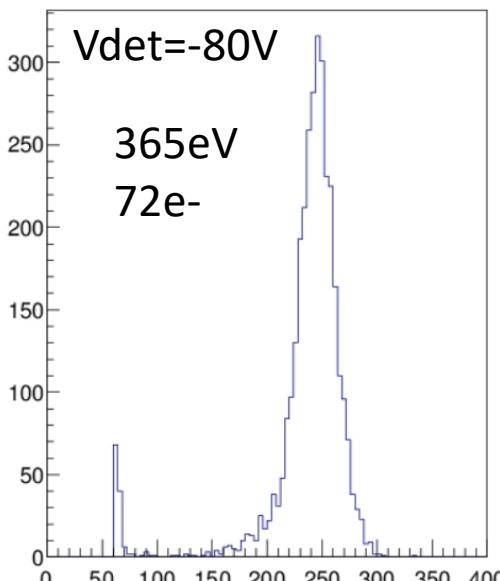
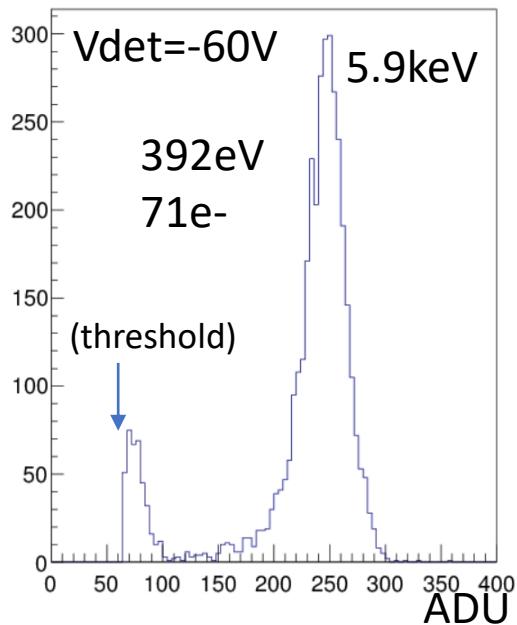
# Energy resolution and readout noise (DSOI-INTPIX8)

02 07

09 13

## Fe-55 spectra

(Preliminary)



1 cluster only  
-50deg.  
Tinteg=1ms  
x10000 frames  
Vcds=800mV

Energy resolution(rms)  
Readout noise(rms)

Statistics increases with  
increasing the back bias  
voltages

Contribution to energy  
resolution from leakage  
current is smaller than  
other (unknown) noise  
sources

\* Champ. data? → see XRPIXs posters

# Summary and future plan

Double SOI pixel sensor is almost ready to use application study

Utilization of double SOI sensor:

- The back-gate effect is suppressed
- Crosstalk is reduced

DSOI compared with SSOI

Sensor gain (CSA pixel): higher (crosstalk suppression)

Noise: comparable

Energy resolution: comparable

Breakdown voltage: comparable

Pixel leakage current: larger back bias dependence (Wafer-related issues)

Full depletion: incomplete (300 um-thick)

Process using new DSOI wafer ( $> 3\text{k}\Omega\text{cm}$ ) is ongoing

It will be tested in 2018