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Development and performance of double SOI pixel sensors

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Double Silicon-on-Insulator (SOI) pixel sensors have been developed using fully-depleted (FD) SOI pixel process technology in recent years. It consists two thin SOI layers and a thick silicon substrate. The top SOI later uses as CMOS circuit and another SOI (middle SOI) layer is used to reduce sensor and circuit crosstalk and the back-gate effect. The middle SOI layer is also effective for enhancement of radiation hardness. The silicon substrate is p-type and the negative back bias is applied. In 2014, a high-resolution, integrated SOI pixel sensor, called INTPIX8, was developed with single and double SOI wafers. It has gain switch to operate the sensor with 4 gain settings. X-ray spectra were obtained using radiation sources to determine the sensor gain and the coupling capacitance between the sensor and the circuit was evaluated. We also performed X-ray imaging tests with wide X-ray ranges. The resistivity of 300 um-thick substrate in the double SOI wafer is about 1 kOhm-cm and the sensor can not be fully-depleted below 500V. Therefore we performed back side thinning up to 75 um and it might be fully-depleted below 100V. We have tested several integration-type pixel sensors with double SOI wafer and various properties such as pixel leakage current, noise, sensor gain and full depletion voltage were investigated. In the presentation, the test results and application examples will be shown.

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