Development of a monolithic pixel sensor based on SOI technology for the ILC vertex detector

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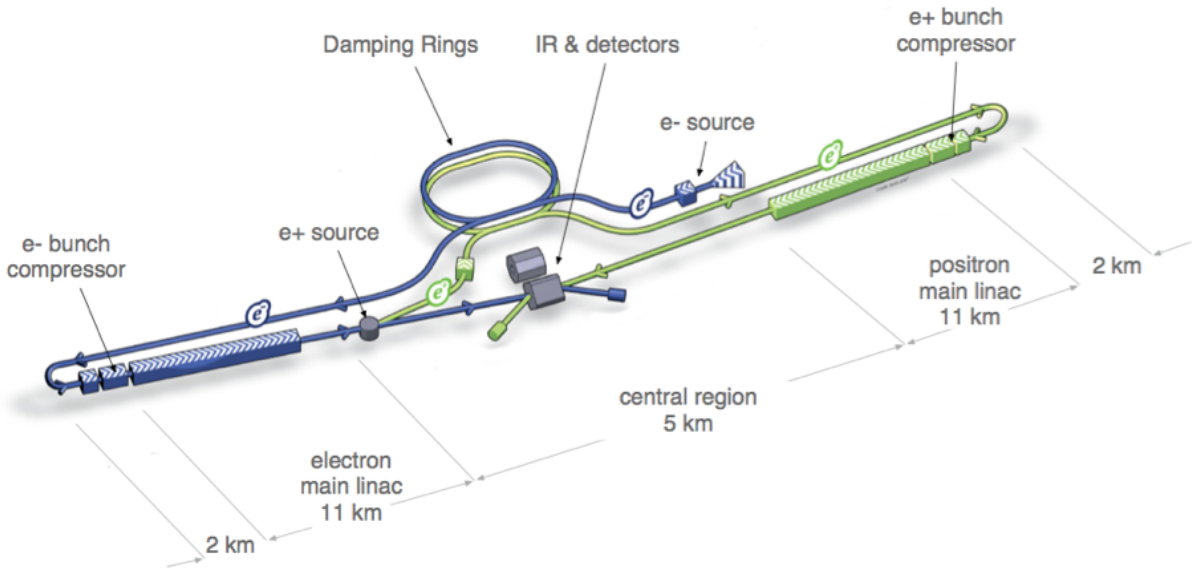
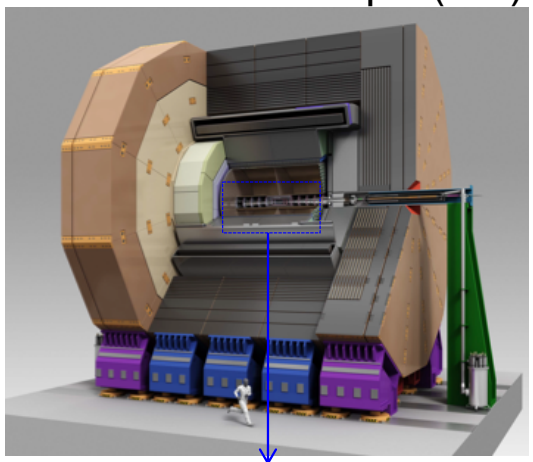
International linear collider

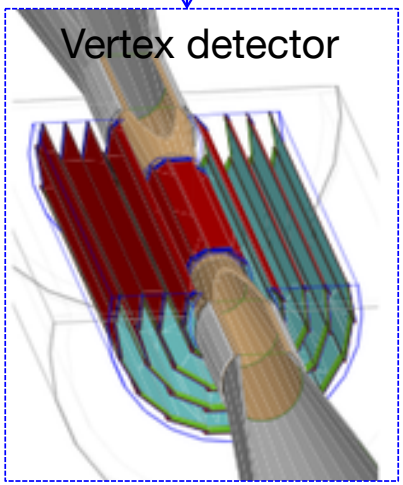
ILC experiment

- e+e- linear collider
- Center of mass energy: 250-500 GeV



ILC detector concept (ILD)

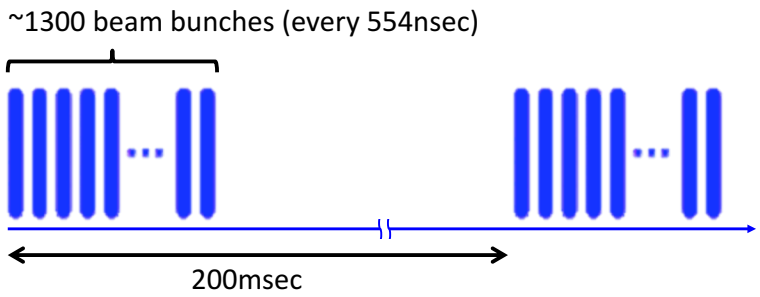




ILC Vertex detector system

- Single point resolution: < 3um
  - Small pixel size: < 25 μm pitch

- Occupancy reduction: < 2%
- Time resolution: 554ns interval
  - Bunch identification during beam train



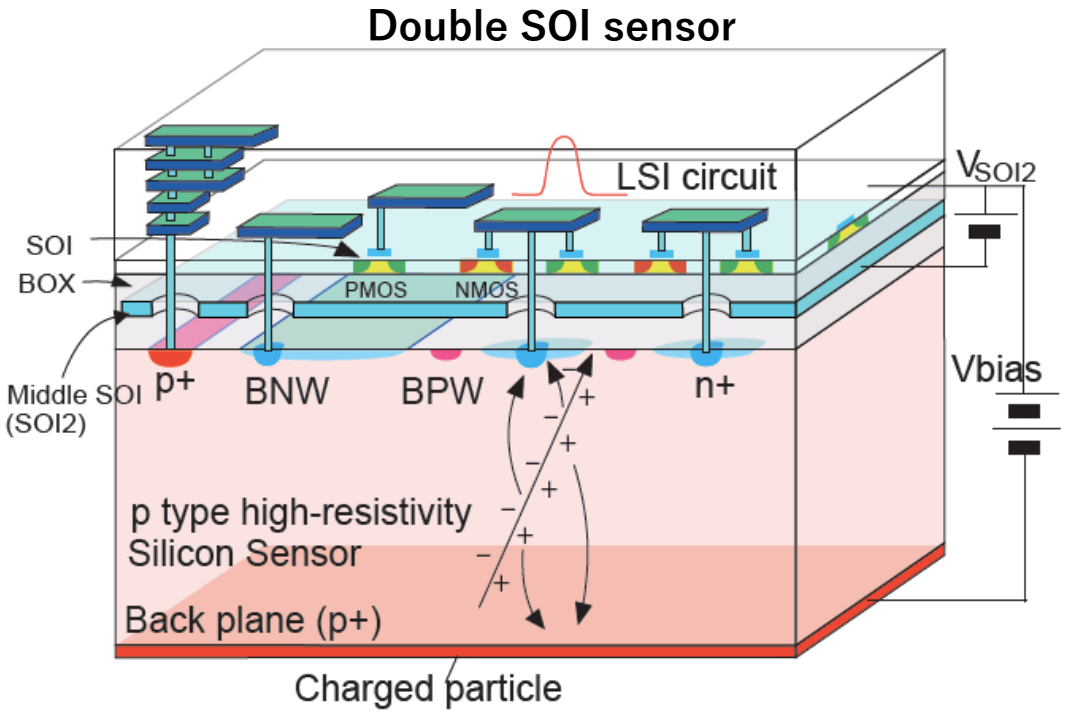
- Low material budget: ~0.1%/X0
  - corresponds to ~ 100 μm Si thickness
  - Low power consumption (50mW/cm^2)+ gas flow cooling.

- Radiation hardness
  - TID: 1 kGy/year
  - NIEL: 10^{11} 1MeVneq/cm2/year

SOI Pixel Detector (SOIPIX)

- SOI pixel detector
  - Small pixel size
  - Complex functions in pixel
  - Low material budget
  - High speed, Low power circuit

- Double SOI structure
  - Radiation hardness: > 100kGy (TID)

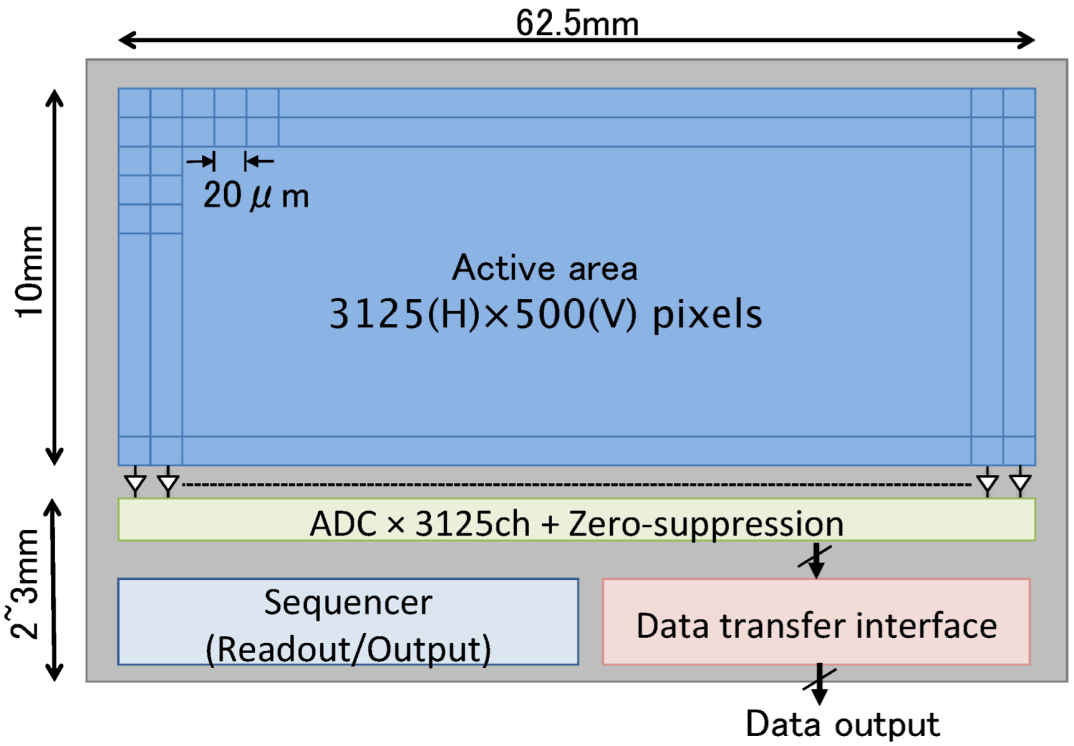


SOI detector for ILC: SOFIST

- SOI sensor for Fine measurement of Space and Time
  - Conceptual design of SOI pixel sensor for the ILC vertex detector

Target:

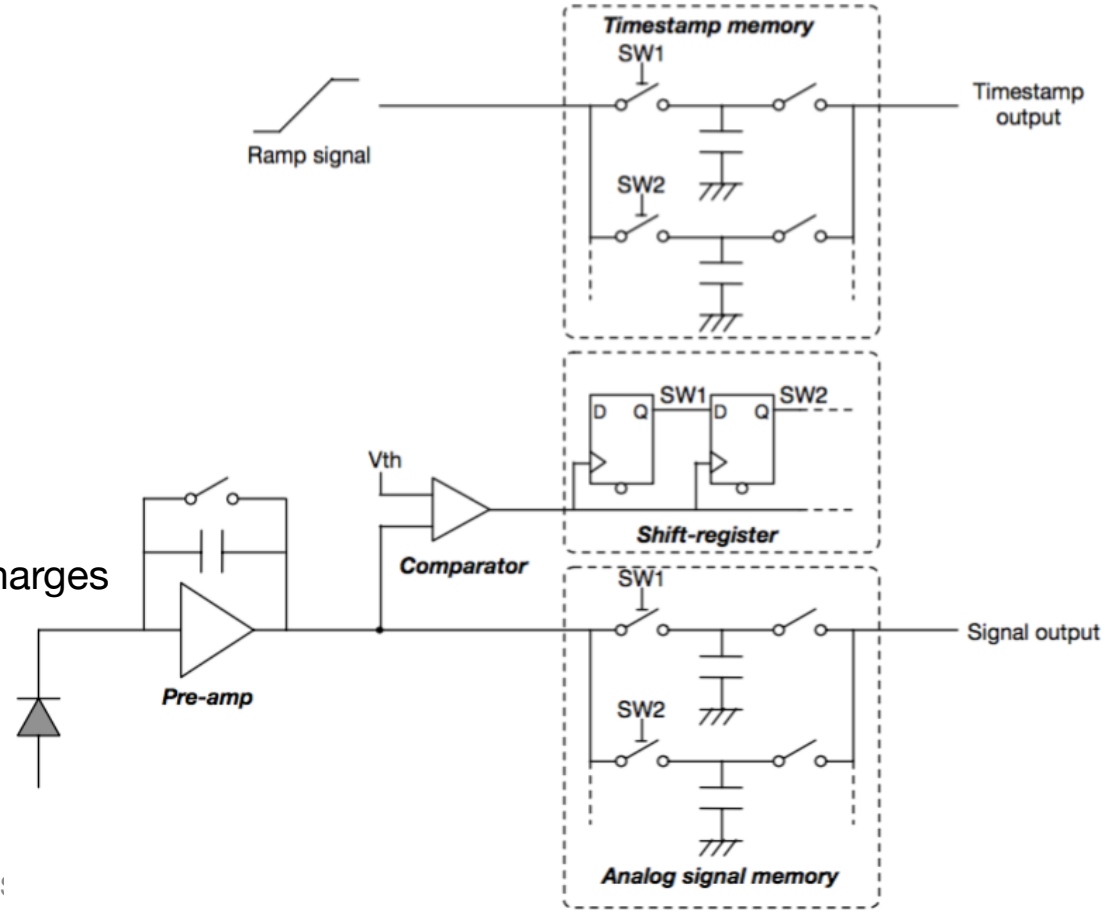
- Single point resolution: < 3 μm
  - Pixel size: 20~25 μm pitch
- Time resolution: 554 ns interval
  - In-pixel timestamp circuit



SOFIST: Pixel architecture

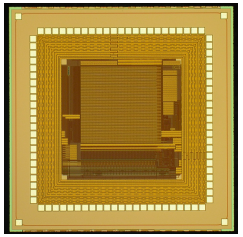
- Pixel circuit
  - Pre-amplifier
  - Comparator
    - Hit-signal discrimination
  - Shift-register
    - Latch hit signal

  - Analog memory
    - Store charge signal
    - Calculate weighted center of charges
  - Timestamp memory
    - Store hit timing
  - Multiple memories



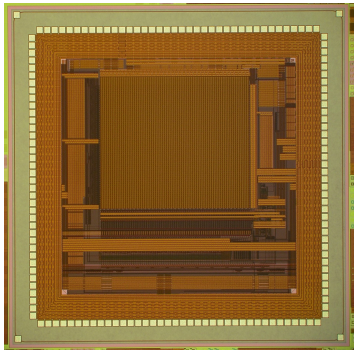
SOFIST: Prototype sensor

- **Ver.1:**
  - Pixel: Analog signal readout
    - Pre-amplifier
    - Analog signal memory



2.9 mm

- **Ver.2:**
  - Pixel: Hit detection, Timestamp
    - Pre-amplifier
    - Comparator + Shift register
    - Analog signal memory / Time stamp memory



4.45 mm

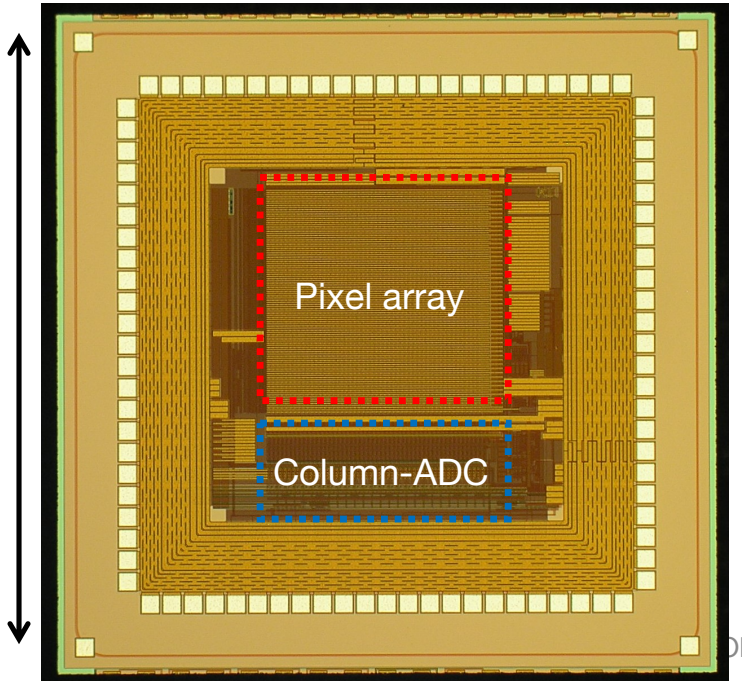
- Ver.3/Ver.4**:** in production
  - Ver.3: Both analog signal and timestamp readout
  - Ver.4: SOI sensor with 3D stacking (Poster by T. Tsuboyama)

SOFIST Ver.1

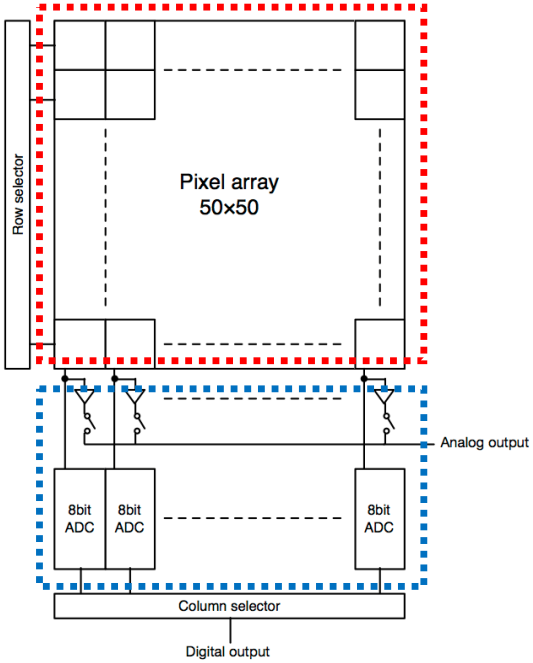
SOFIST Ver.1 sensor

- Pixel circuit
  - Pixel array: 50x50, active area: 1x1 mm^2
  - Sensor thickness: 500 μm

2.9 mm

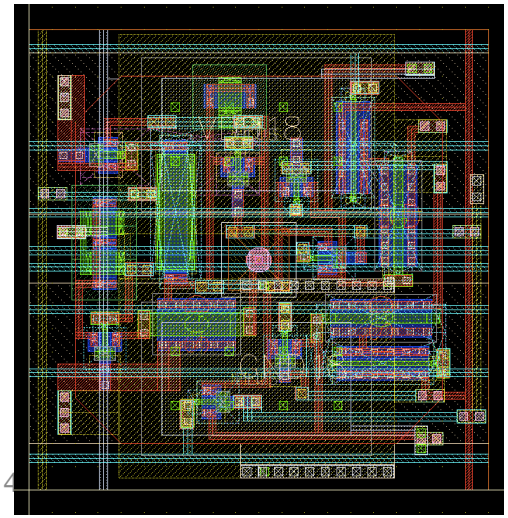


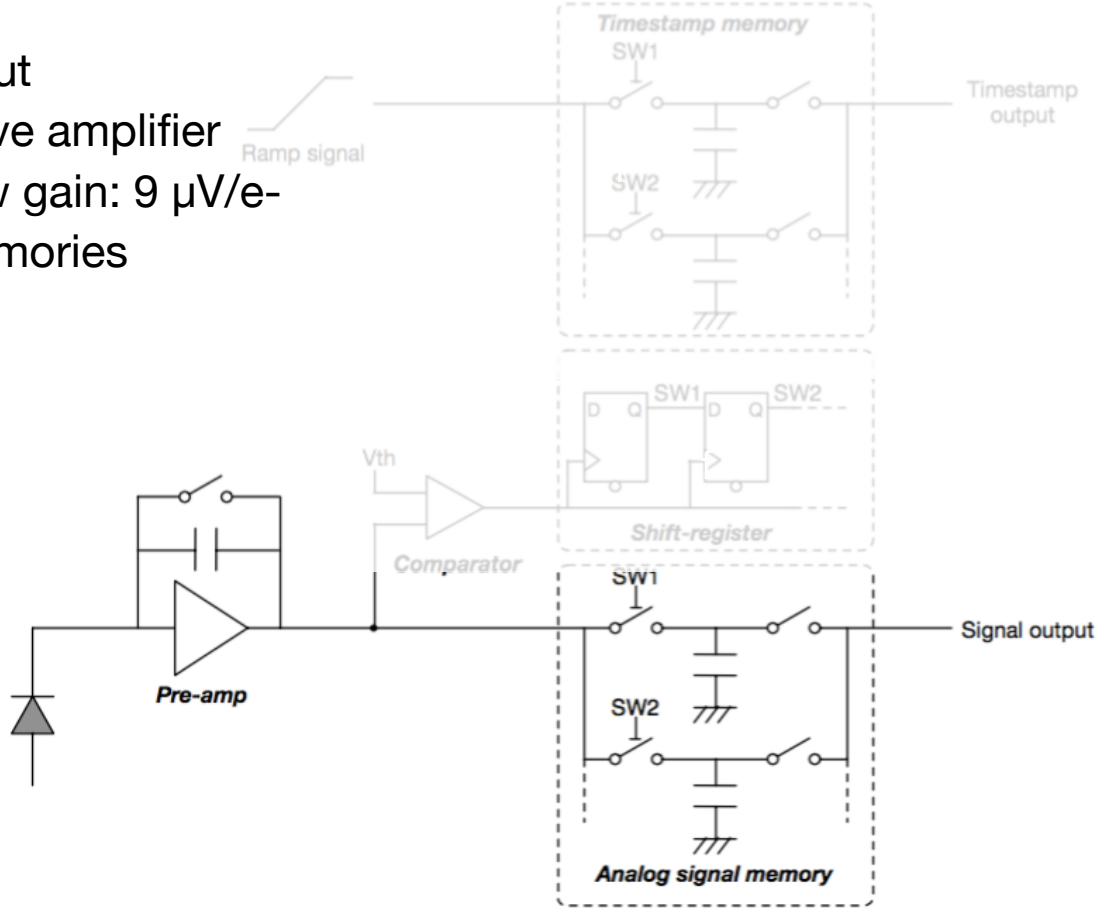
- Signal readout
  - Analog output or Column ADC readout



SOFIST Ver.1 sensor: Pixel circuit

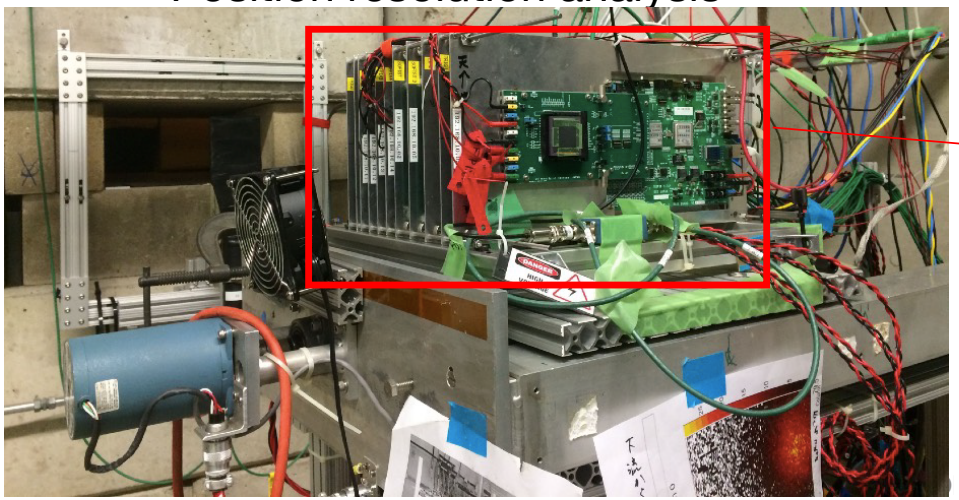
- Pixel circuit: Analog signal readout
  - Pre-amplifier: Charge sensitive amplifier
    - High gain : 32 μV/e-, Low gain: 9 μV/e-
  - Analog signal memory: 2 memories
  - Pixel size: 20x20 μm^2

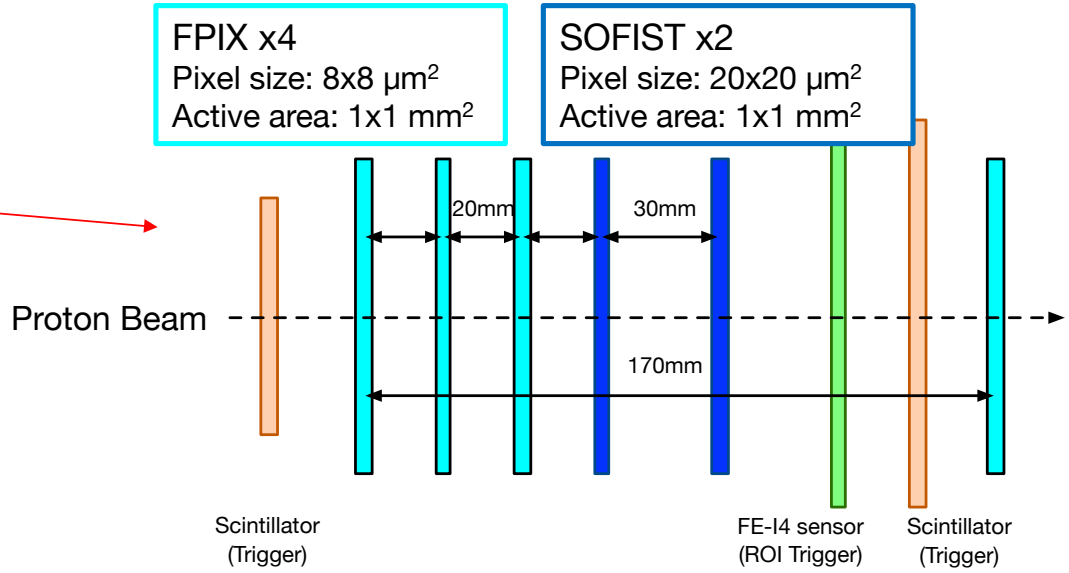




SOFIST Ver.1 sensor: Beam test

- Beam test with SOFIST Ver.1 + FPIX (Talk by K. Hara)
  - Fermilab Test beam Facility (Jan. 2017)
  - Proton beam: 120 GeV
- Sensor evaluation
  - Particle track reconstruction
  - Position resolution analysis



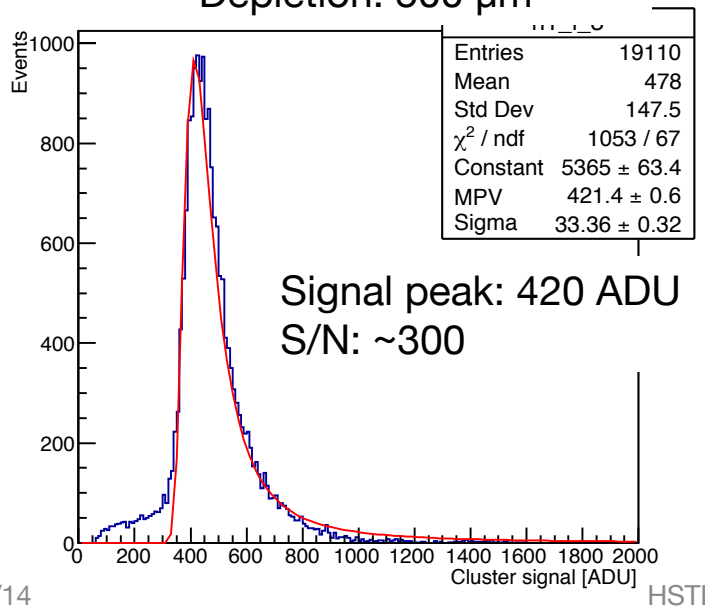


Cluster signal spectrum

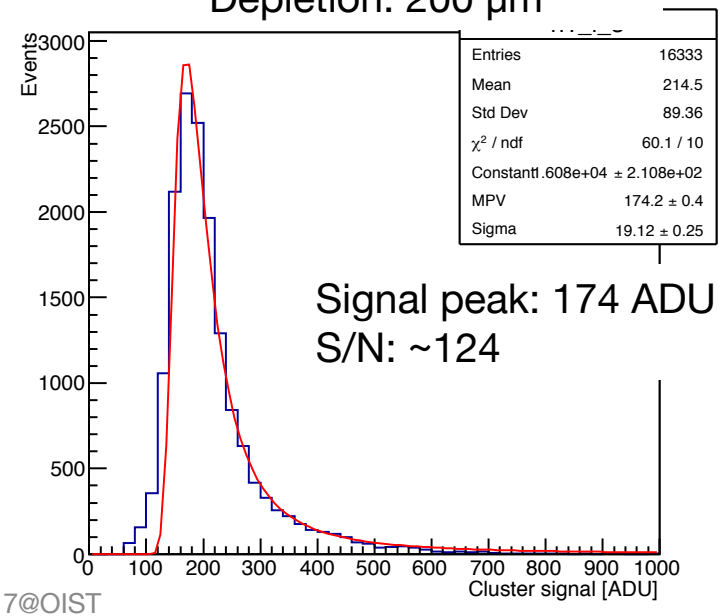
- Sensor setup
  - Bias voltage: 130 V, 15 V
  - (Depletion width: 500 μm, 200 μm)

- Cluster signal reconstruction
  - Summing 5x5 pixels around hit
- Readout by External ADC (12 bit)
  - Pixel Noise: ~1.4 ADU

Depletion: 500 μm

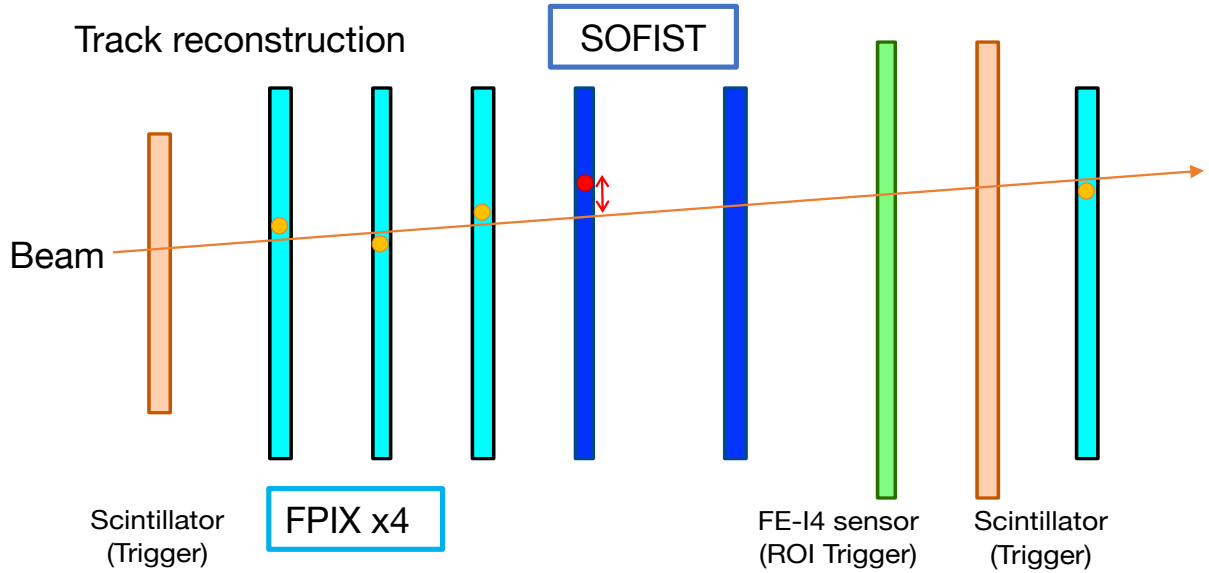


Depletion: 200 μm



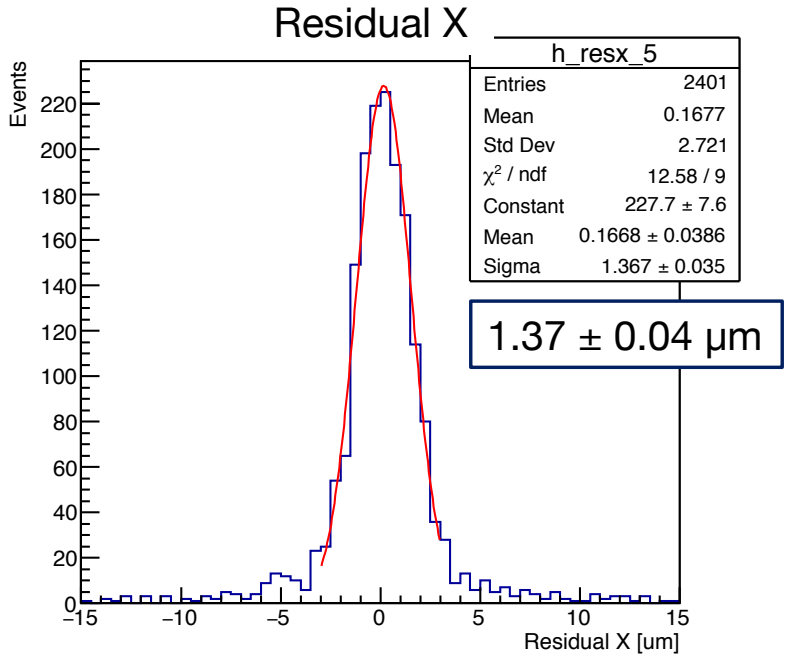
Tracking and residual analysis

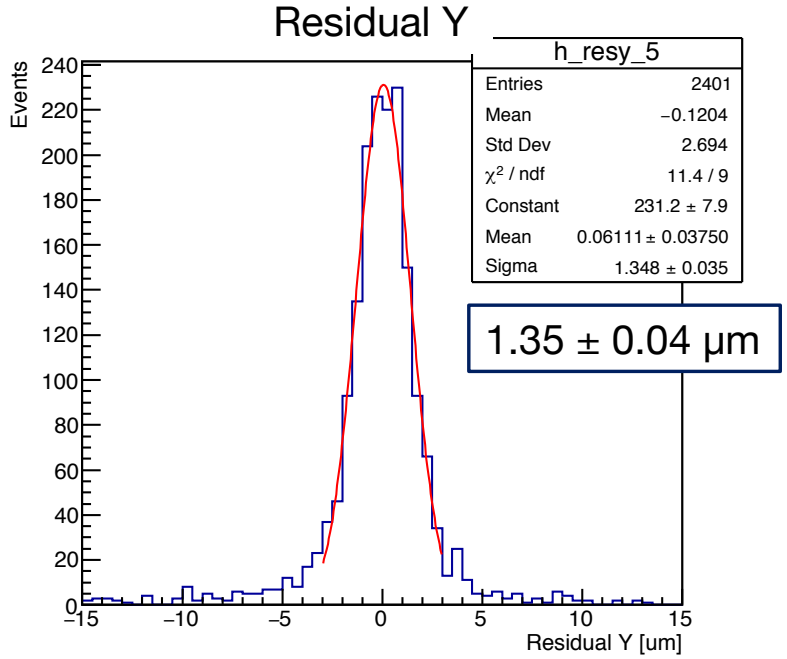
- **Track reconstruction**
  - Find track candidates from 4 FPIX hits (FPIX resolution: 0.6~0.7 μm)
- **Residual calculation**
  - Difference between reconstructed track and detected hit on the SOFIST



Residual distribution: 500 μm thickness

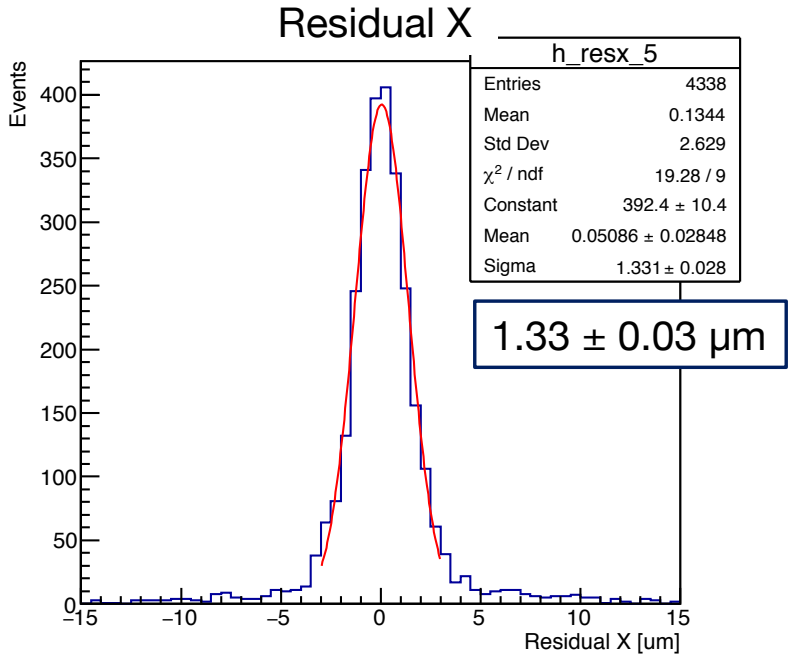
- Sensor setup:
  - Depletion width: ~500 μm (HV = 130V)
  - Readout by External ADC (12bit)

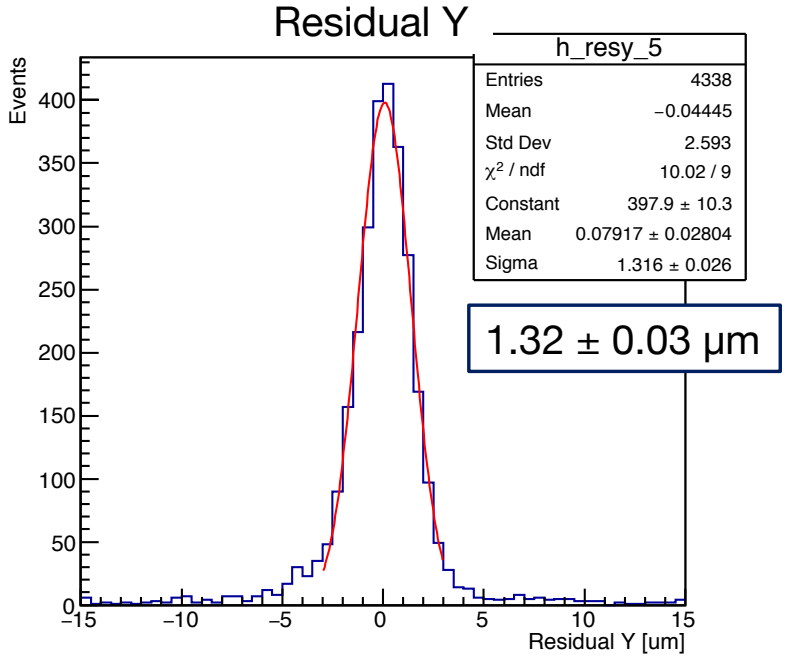




Residual distribution: 200 μm thickness

- Sensor setup:
  - Depletion width: ~200 μm (HV = 20V)
  - Readout by External ADC (12bit)



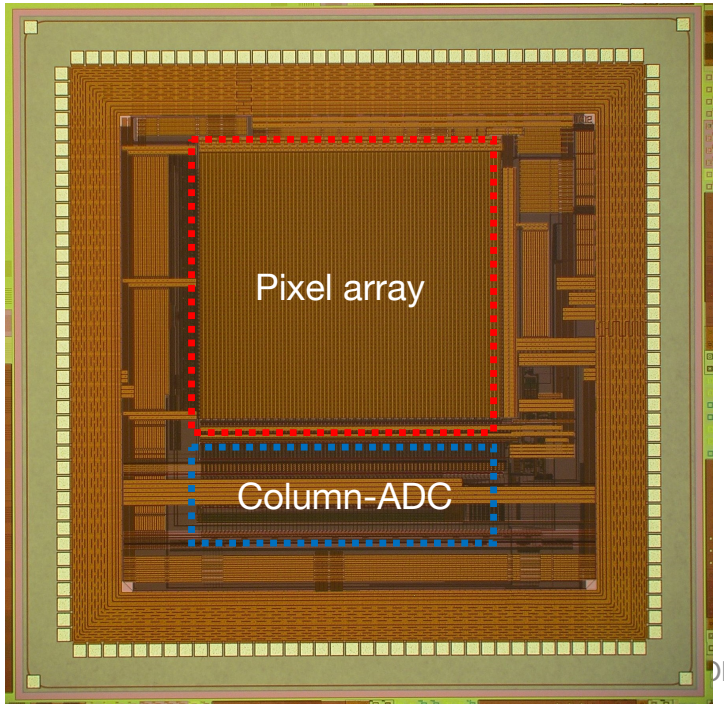


SOFIST Ver.2

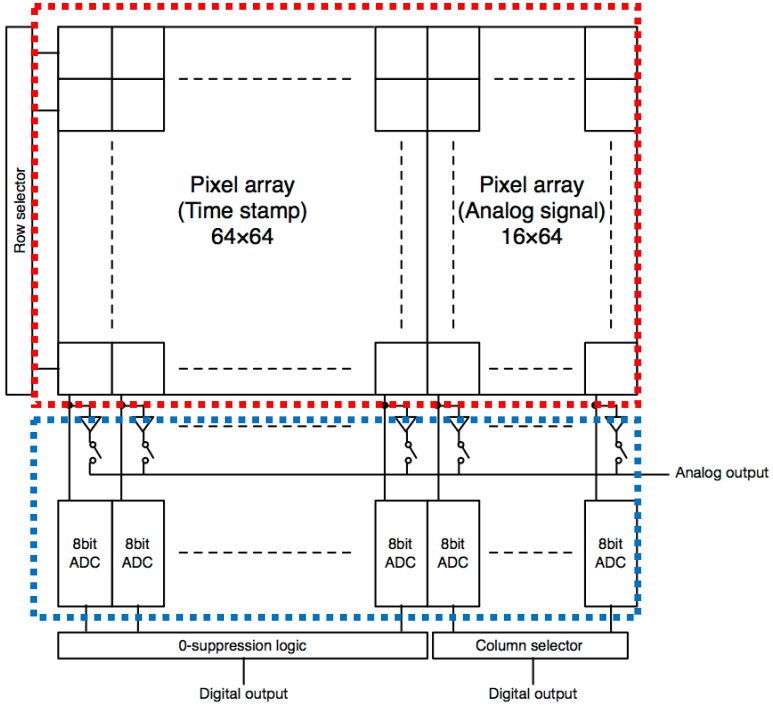
SOFIST Ver.2 sensor

- Pixel circuit
  - Pixel array: 80x64, Active area: 2x1.6mm^2
  - Sensor thickness: 300 μm (Thinning to 75 μm)

4.45 mm

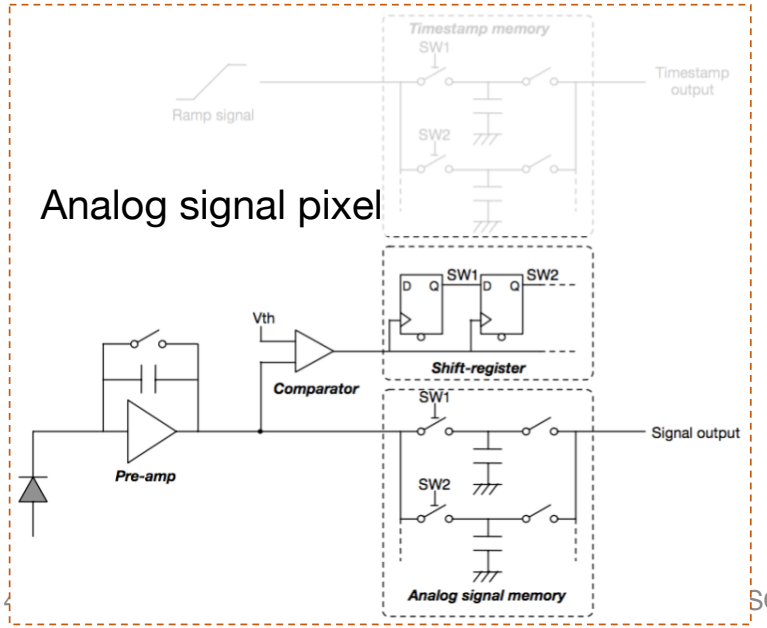


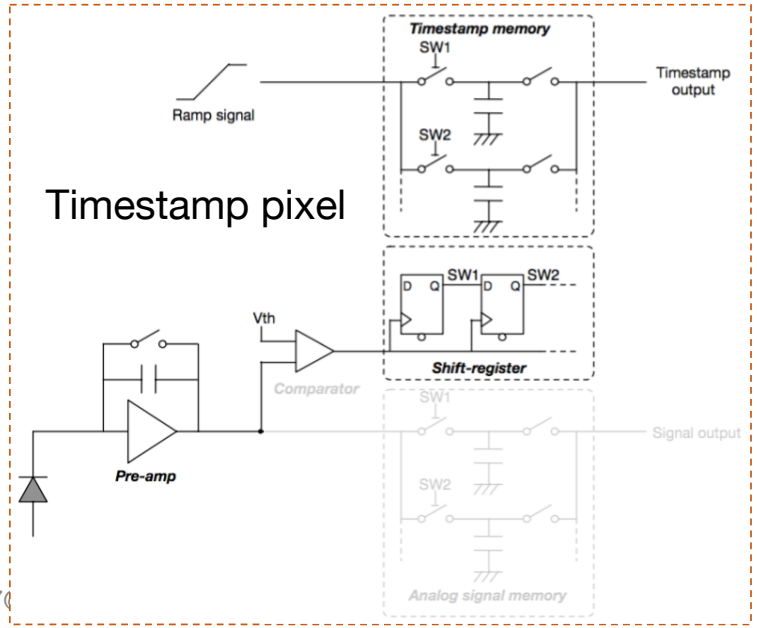
- Pixel type
  - Analog signal pixel
  - Timestamp pixel



SOFIST Ver.2 sensor: Pixel circuit

- Pixel circuit: Hit detection, Timestamp
  - Pixel size: 25x25 μm^2
  - Comparator + Shift register (2 stage D-FF)
  - Analog signal memory or Time stamp memory (2 Memories)

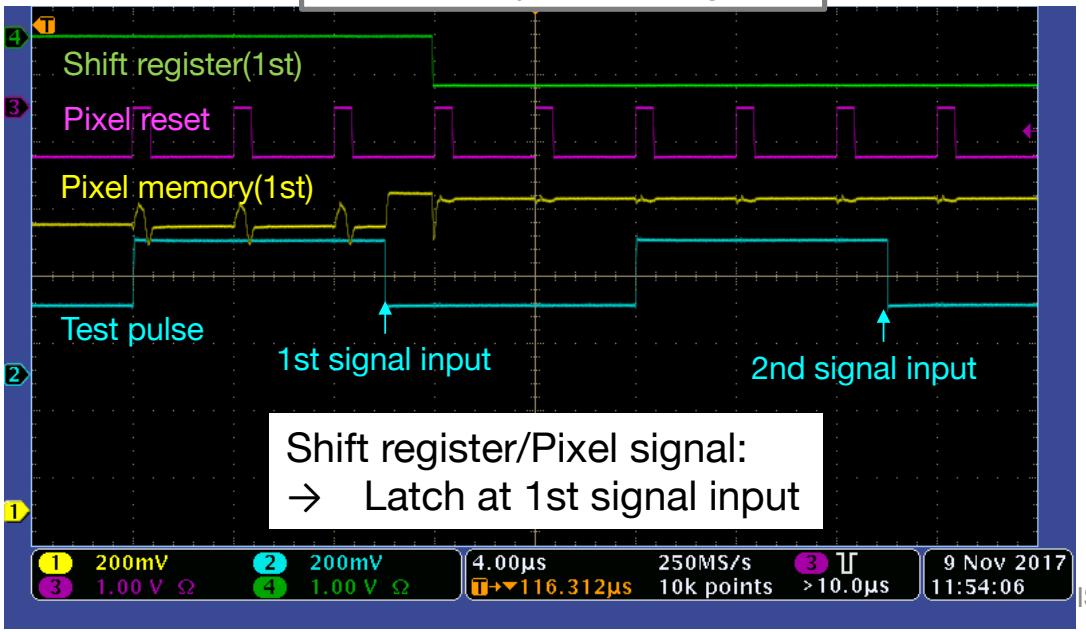




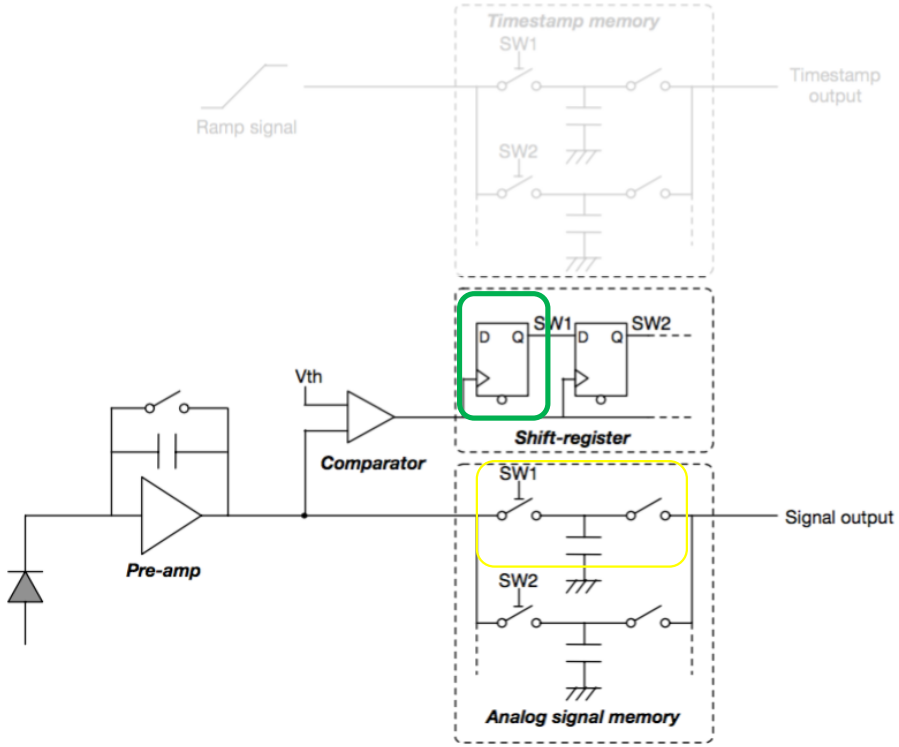
SOFIST Ver.2 sensor: Analog signal pixel

- Analog signal pixel
  - Pixel response by test pulse: 200 mV
  - Threshold voltage: 100 mV

1st Memory / Shift register

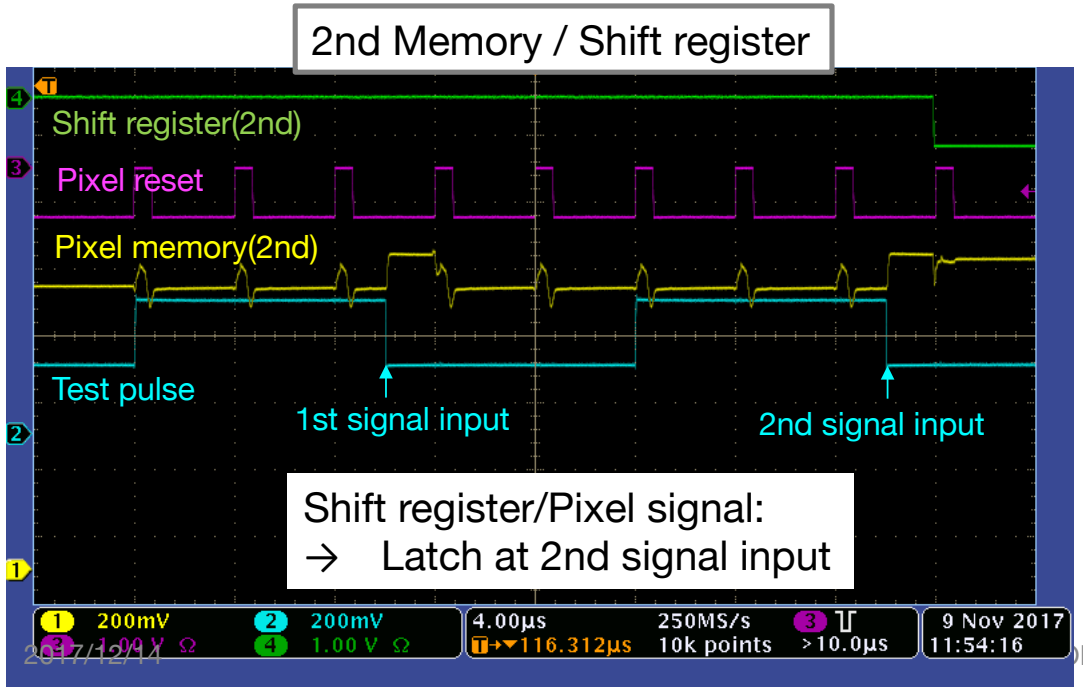


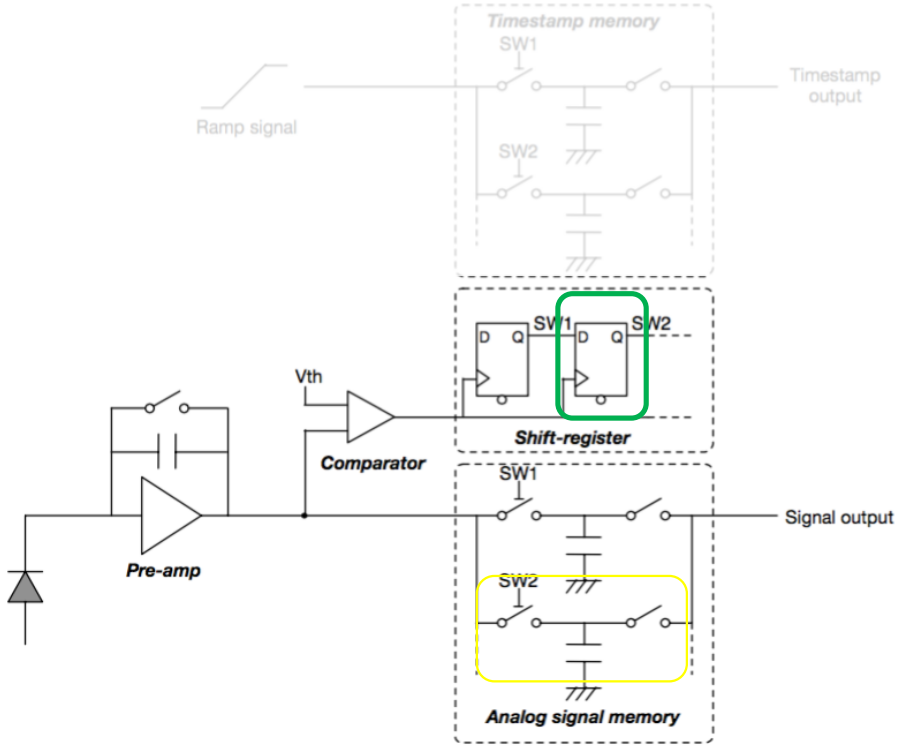
Shift register/Pixel signal:
→ Latch at 1st signal input



SOFIST Ver.2 sensor: Analog signal pixel

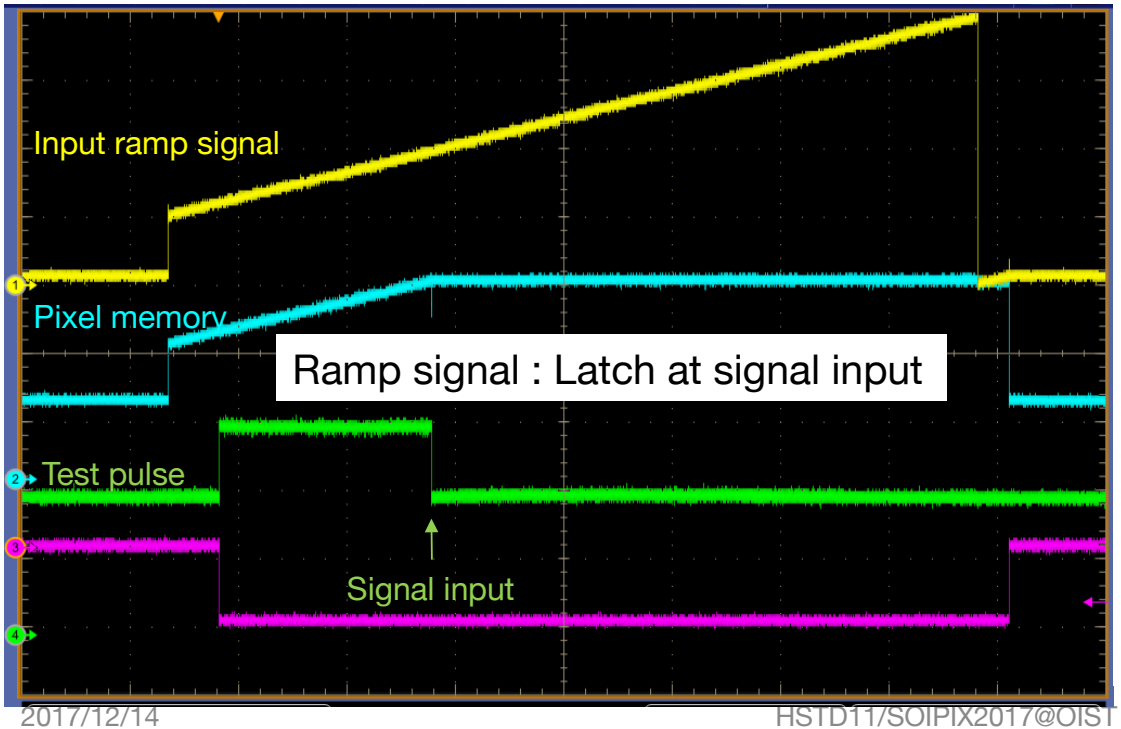
- Analog signal pixel
  - Pixel response by test pulse: 200 mV
  - Threshold voltage: 100 mV

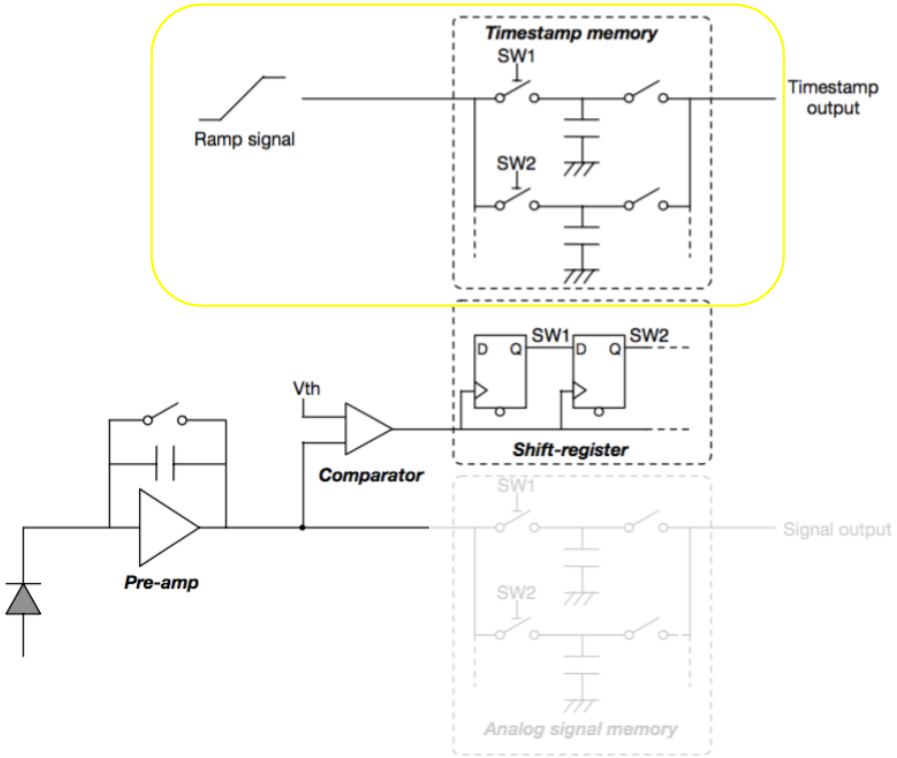




SOFIST Ver.2 sensor: Timestamp pixel

- Timestamp pixel
  - Pixel response by test pulse:





Summary

- SOI pixel sensor for ILC vertex detector: SOFIST
  - Pixel: Store both hit signal and timing

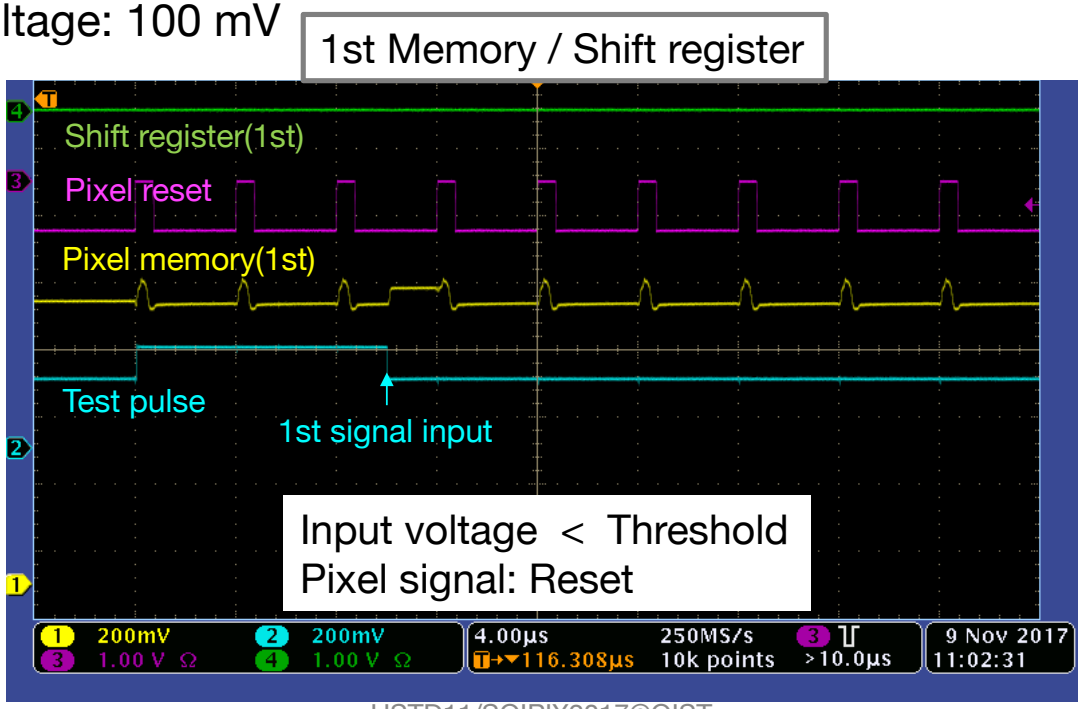
- SOFIST Ver.1: Pixel for analog signal readout
  - Particle tracking and positon resolution analysis
  - Residual width: 1.33 ± 0.04 μm @200 μm

- SOFIST Ver.2: Pixel for hit detection, timestamp
  - Confirmed pixel operation.
  - Beam test : scheduled in Feb. 2018

Backup

SOFIST Ver.2 sensor: Analog signal pixel

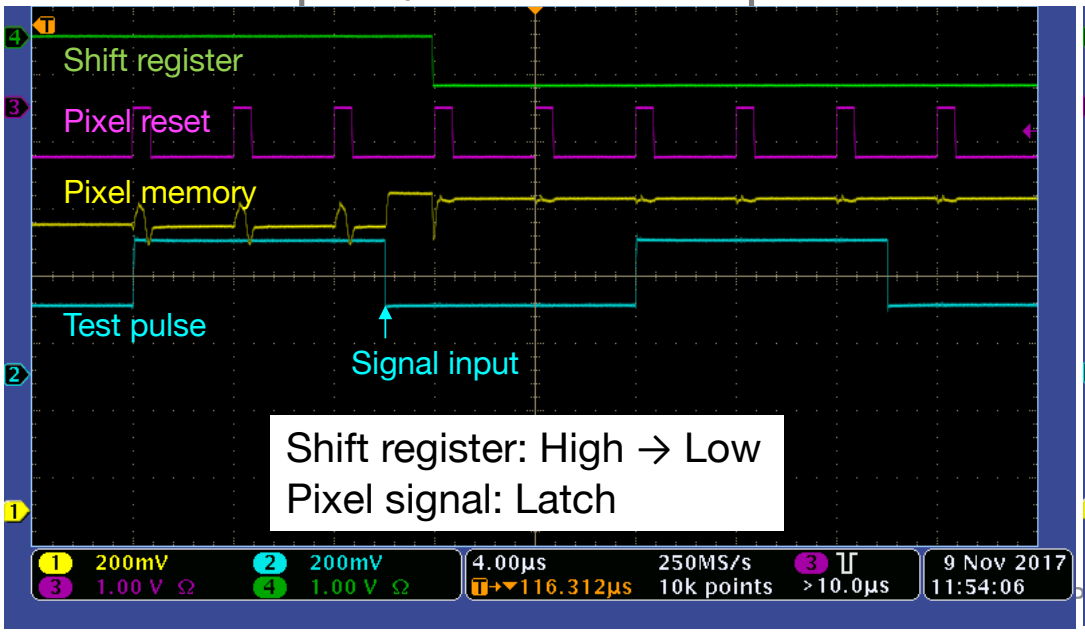
- Analog signal pixel
  - Pixel response by test pulse: < 100 mV
  - Threshold voltage: 100 mV



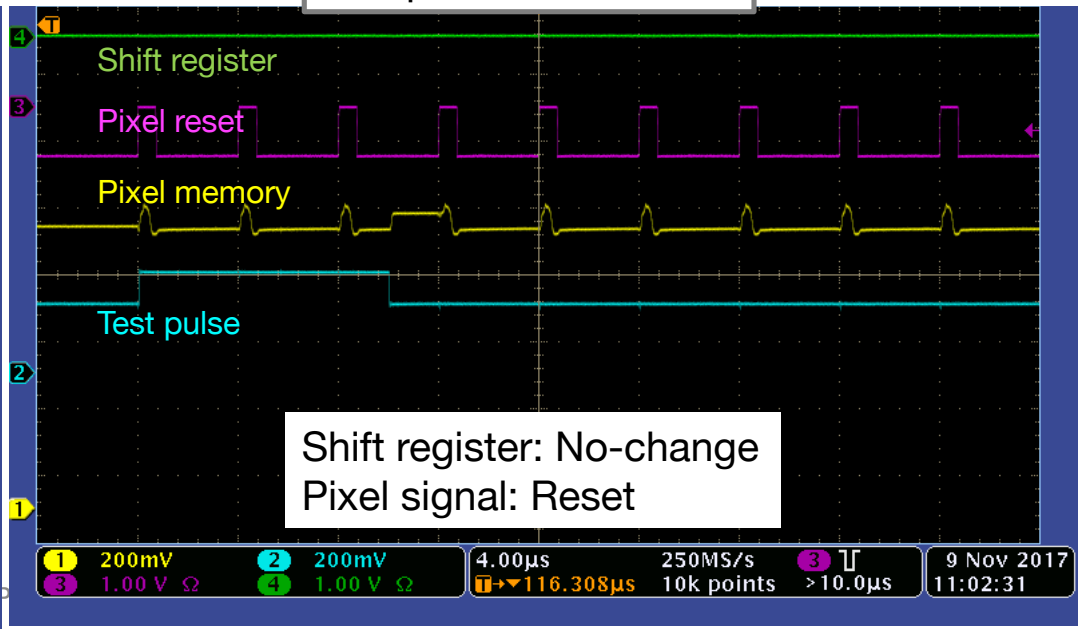
SOFIST Ver.2 sensor: Analog signal pixel

- Analog signal pixel
  - Pixel response by test pulse: 200 mV, 100 mV
  - Threshold voltage: 100 mV

Test pulse > Threshold



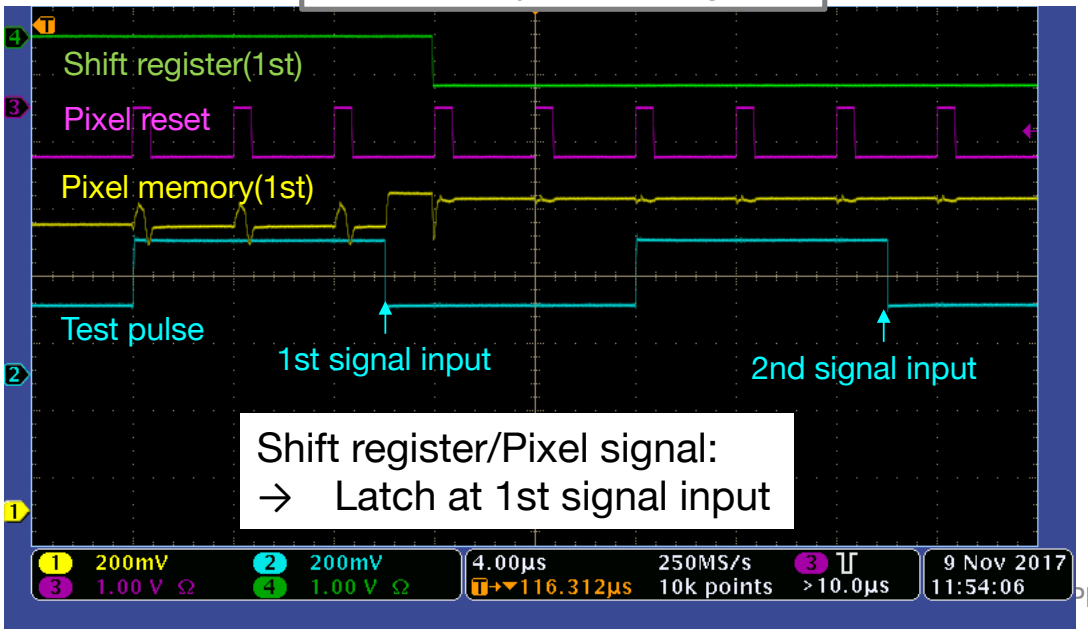
Test pulse < Threshold



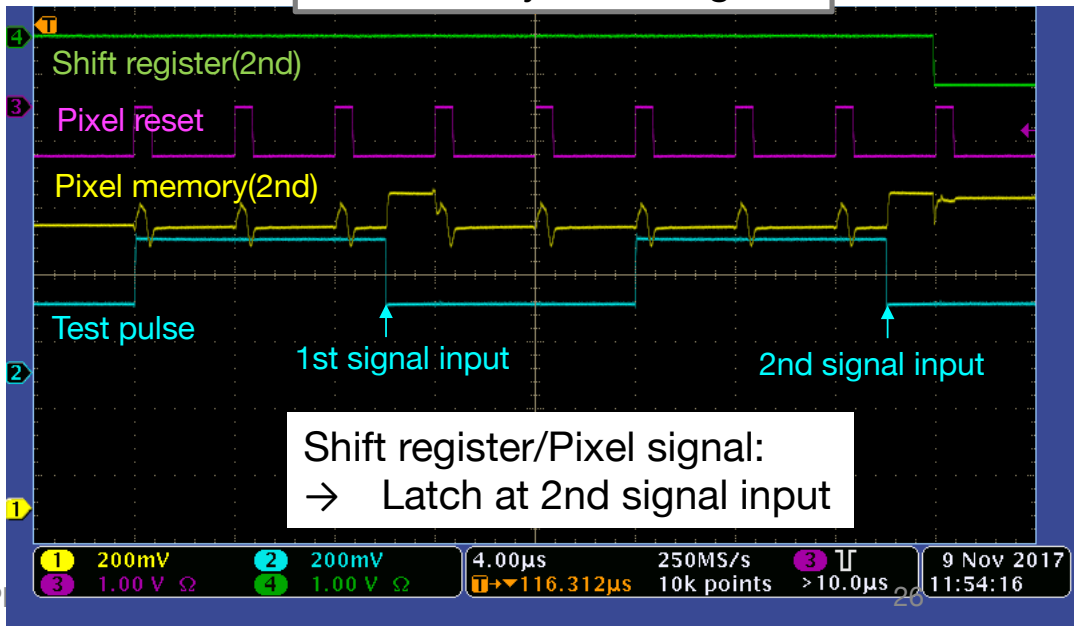
SOFIST Ver.2 sensor: Analog signal pixel

- Analog signal pixel
  - Pixel response by test pulse: 200 mV
  - Threshold voltage: 100 mV

1st Memory / Shift register

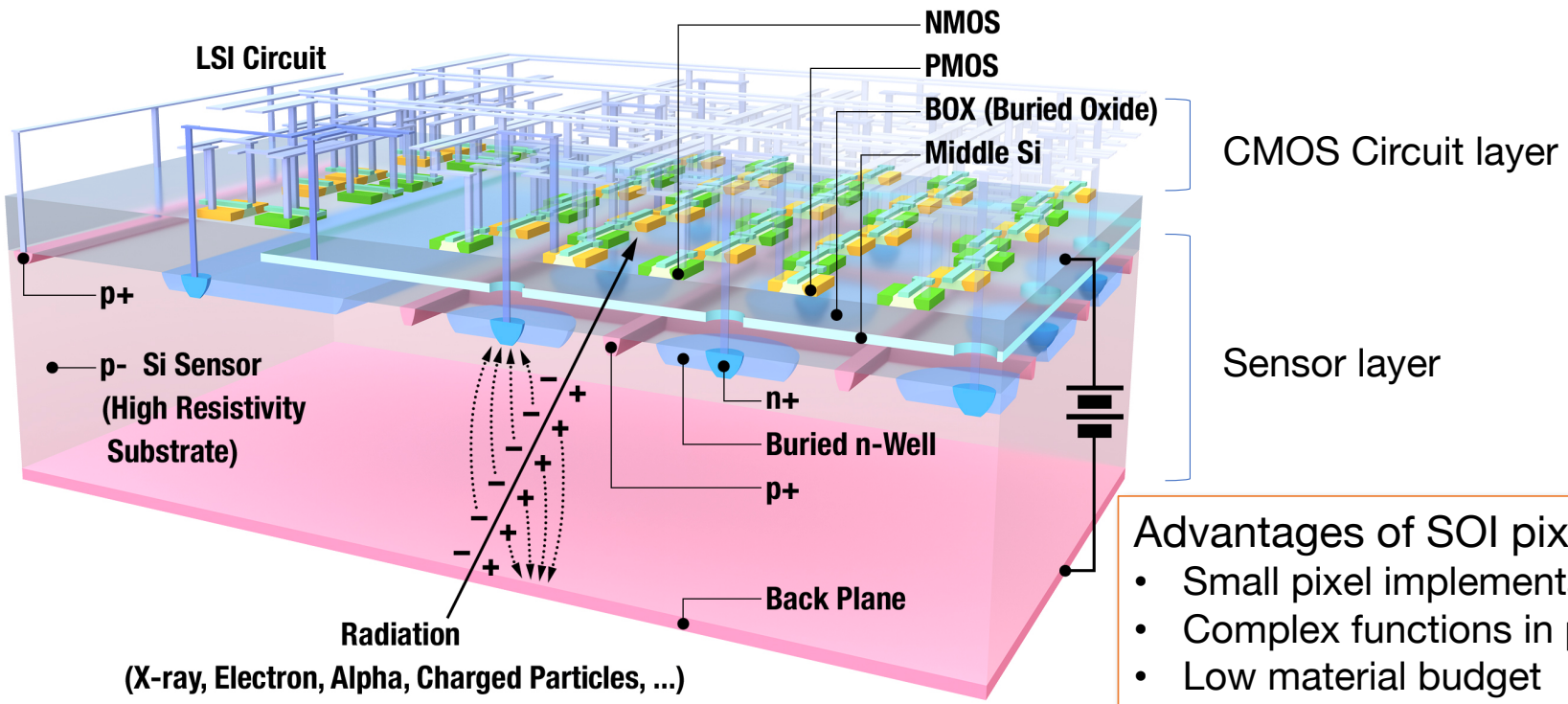


2nd Memory / Shift register



SOI Pixel Detector (SOIPIX)

Detector structure of Double SOI sensor



CMOS Circuit layer

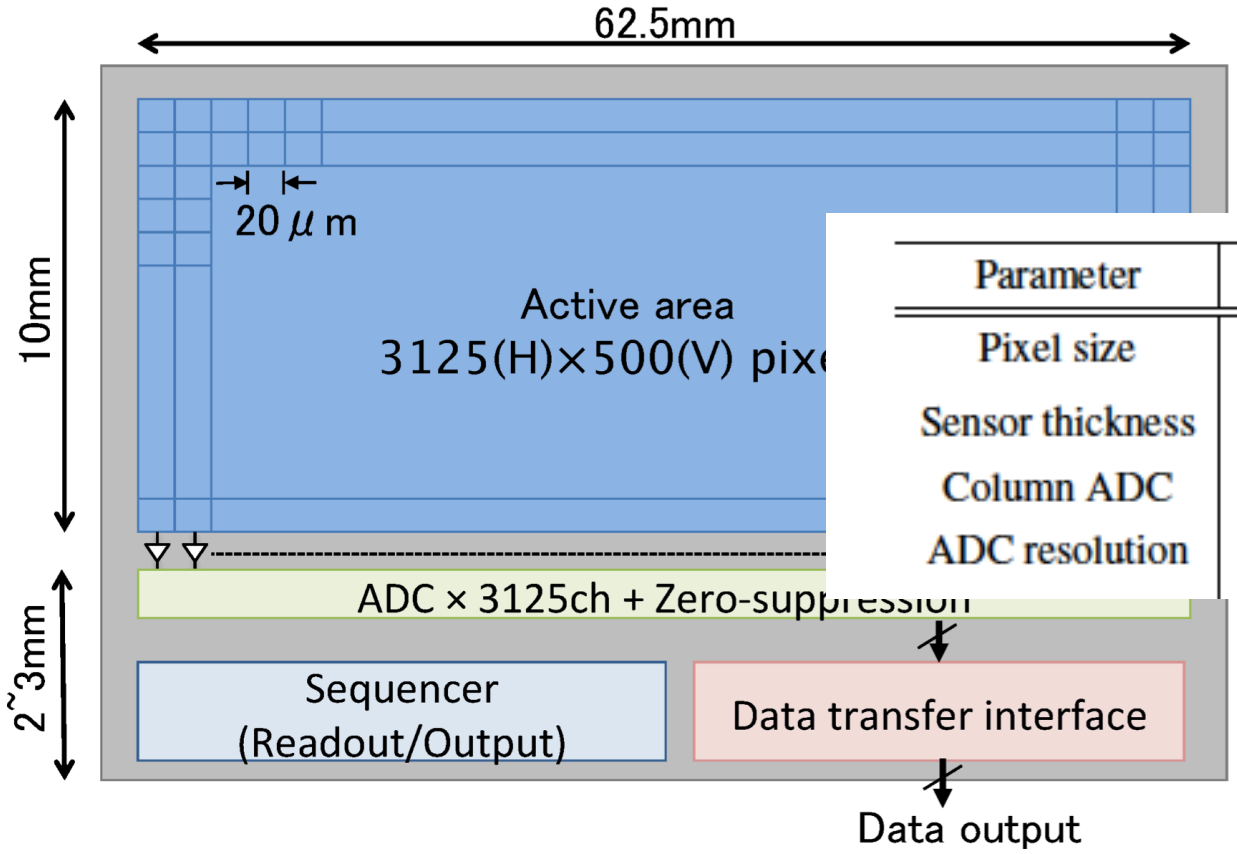
Sensor layer

Advantages of SOI pixel detector

- Small pixel implementation
- Complex functions in pixel circuit
- Low material budget
- High speed, Low power
- Radiation hardness: > 100kGy(TID)

SOI sensor for ILC: SOFIST

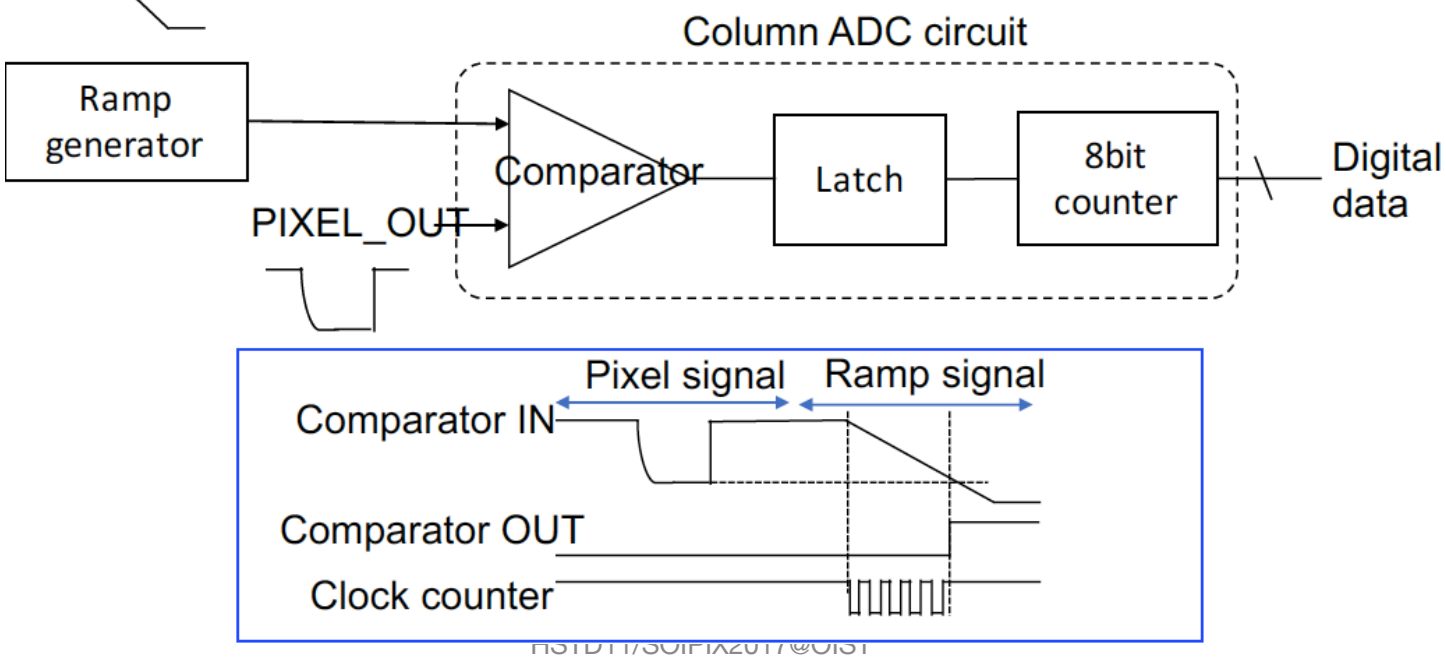
- SOI sensor for Fine measurement of Space and Time



Parameter	
Pixel size	$20\times20\ \mu m^2$
Sensor thickness	$50\ \mu m$
Column ADC	3125 channels
ADC resolution	Analog signal: ≥ 8 bit

SOFIST Ver.1: Column ADC

- Colum ADC circuit
  - Wilkinson-Type ADC
  - Resolution: 8bit / 1V = 3.9mV/bit. Conversion time: 2.56usec



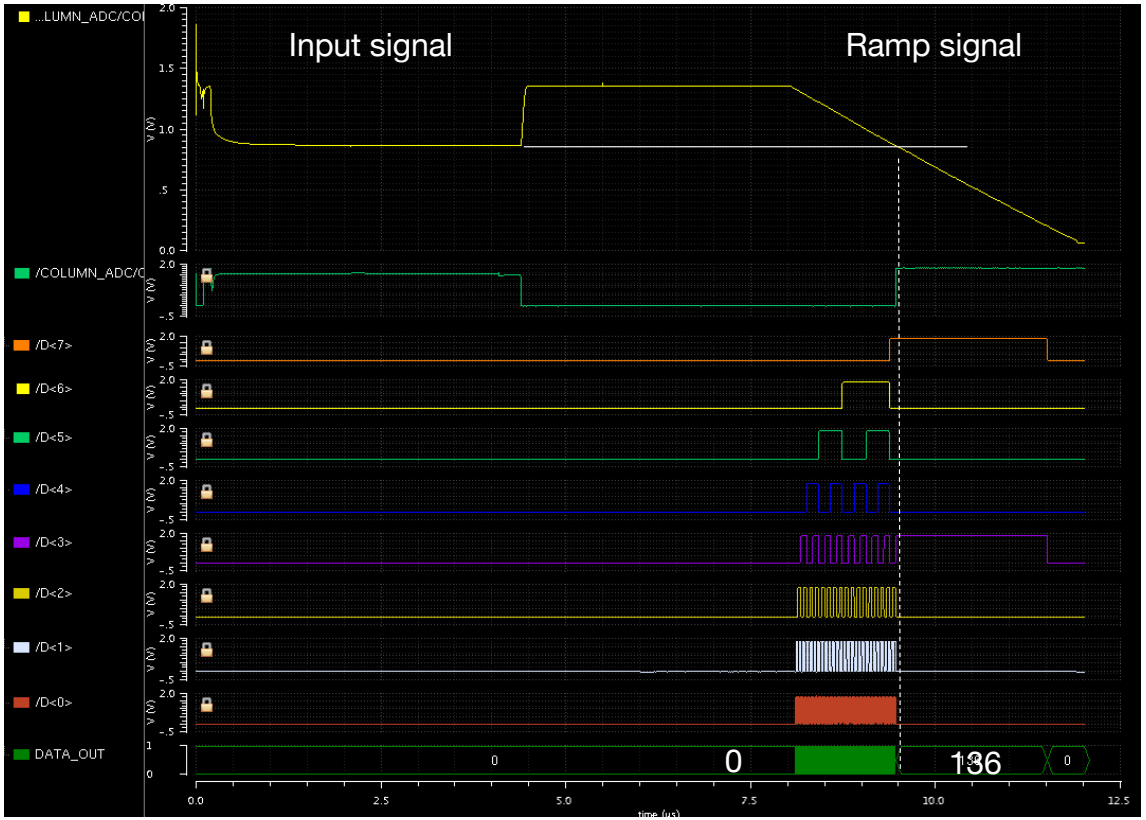
SOFIST Ver.1: Column ADC

- ADC SPICE simulation

Signal/Ramp input

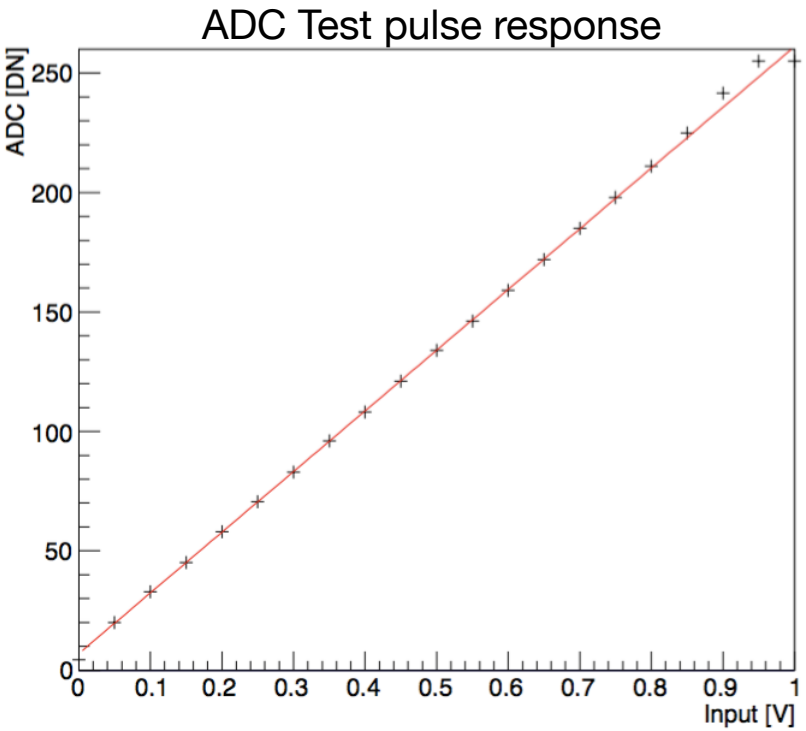
Comparator

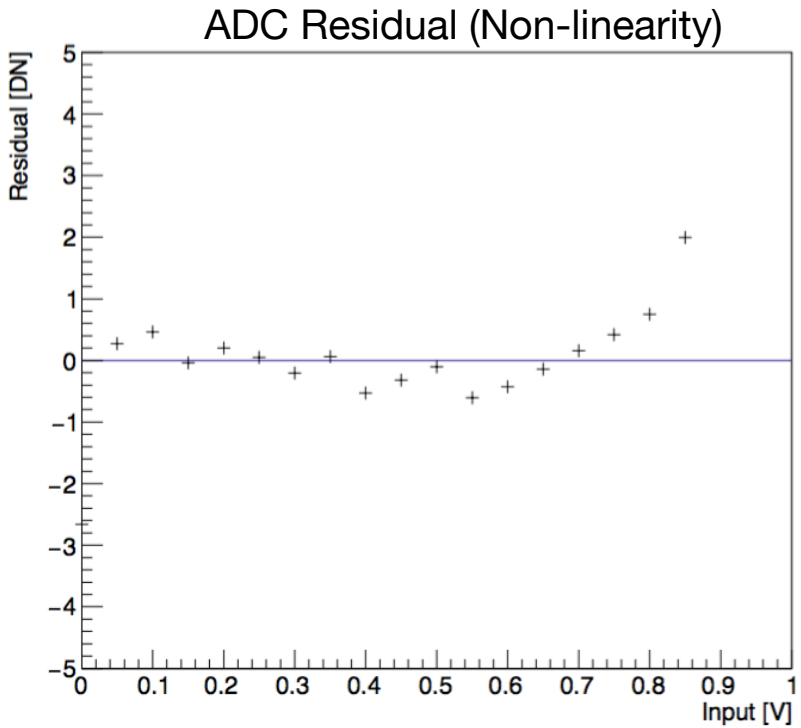
Output (8bit)



SOFIST Ver.1:

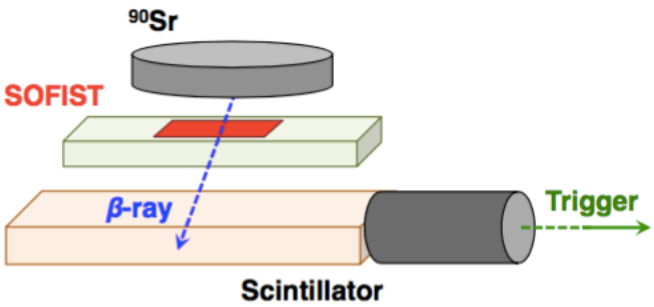
- Column ADC: output linearity
  - ADC response by test pulse input.



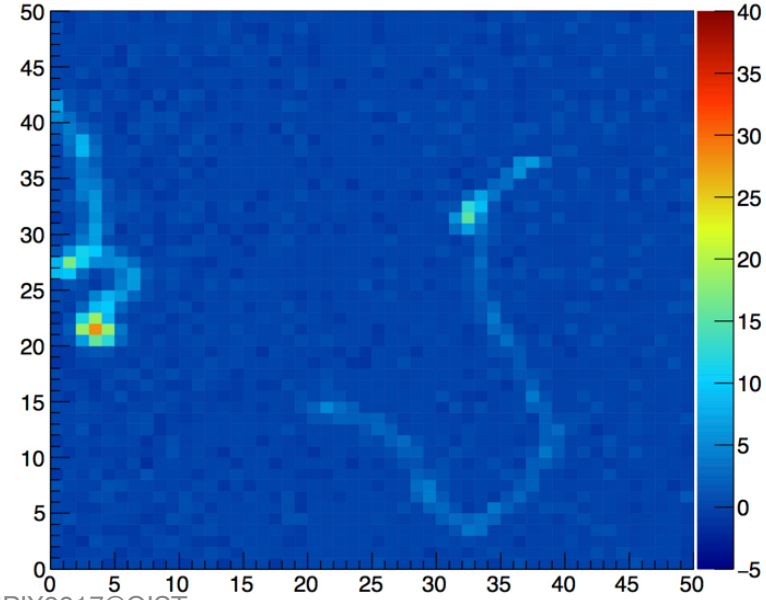


SOFIST Ver.1 chip

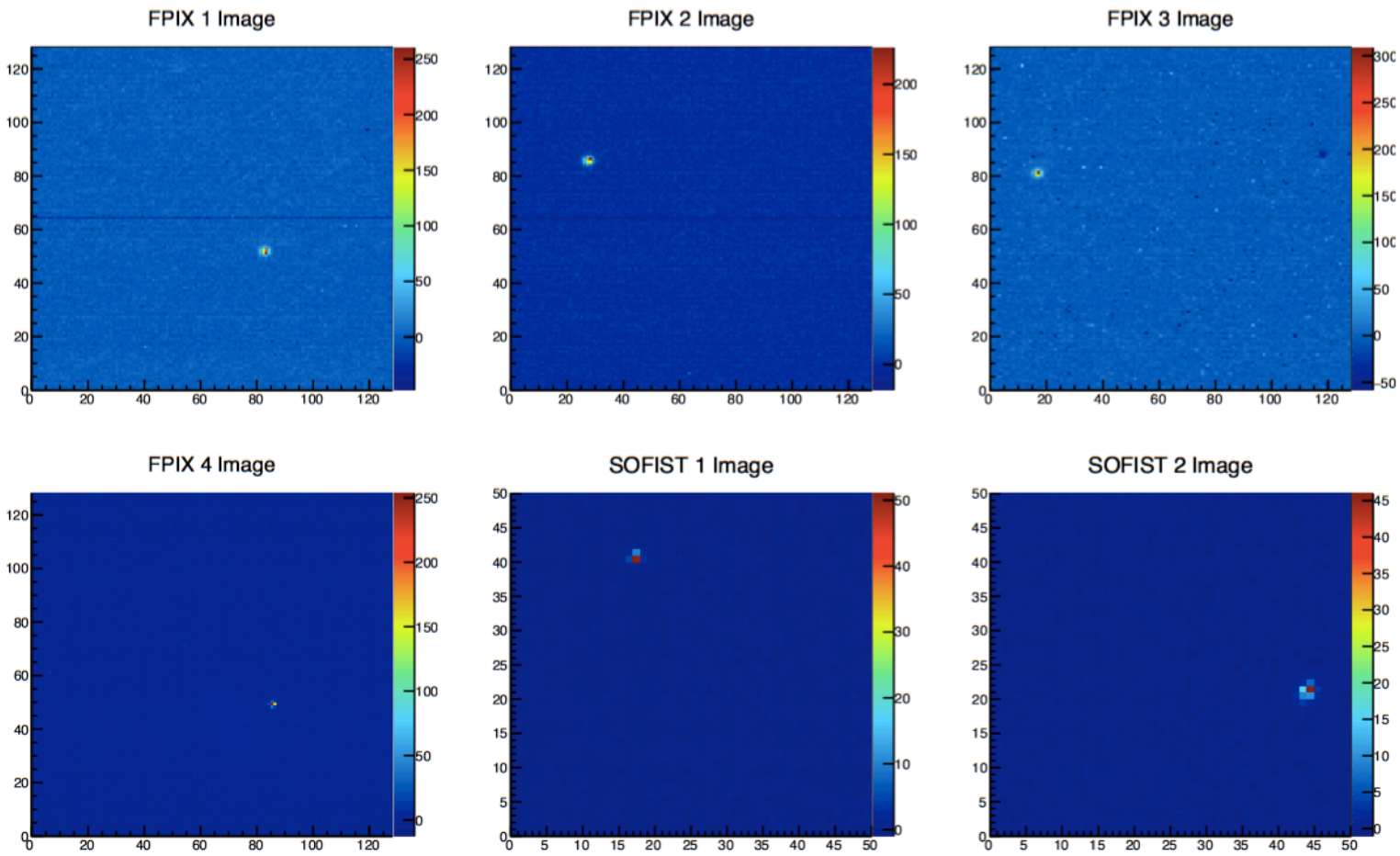
- Sr-90 irradiation
  - SOFIST setup: Bias voltage = 140V, Readout by On-chip ADC



SOFIST output data



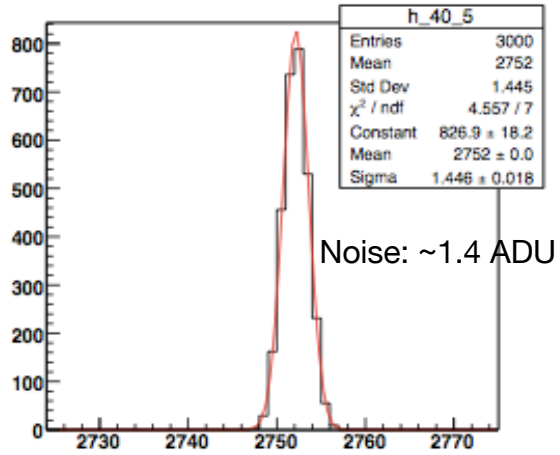
Beam test: Event display



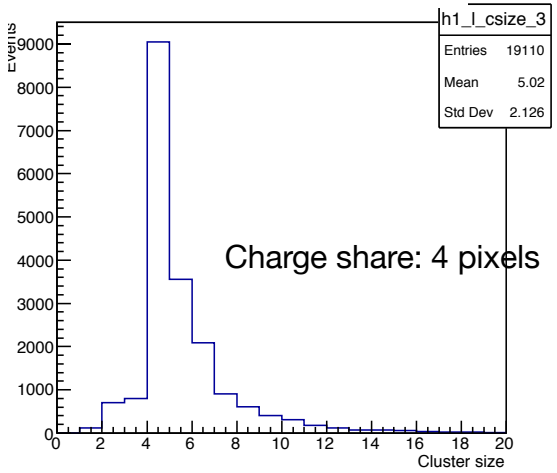
Cluster signal, S/N

- Sensor setup
  - Depletion width: ~500 μm (HV = 130V)
  - Readout by External ADC (12 bit)
- Cluster signal reconstruction
  - Finding hit pixel over threshold
  - Summing 5x5 pixels around hit

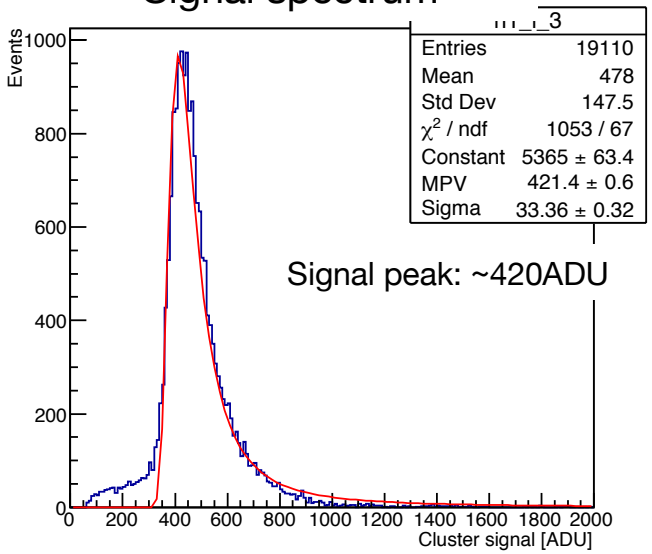
Pixel noise



Cluster size (Pixel)



Signal spectrum



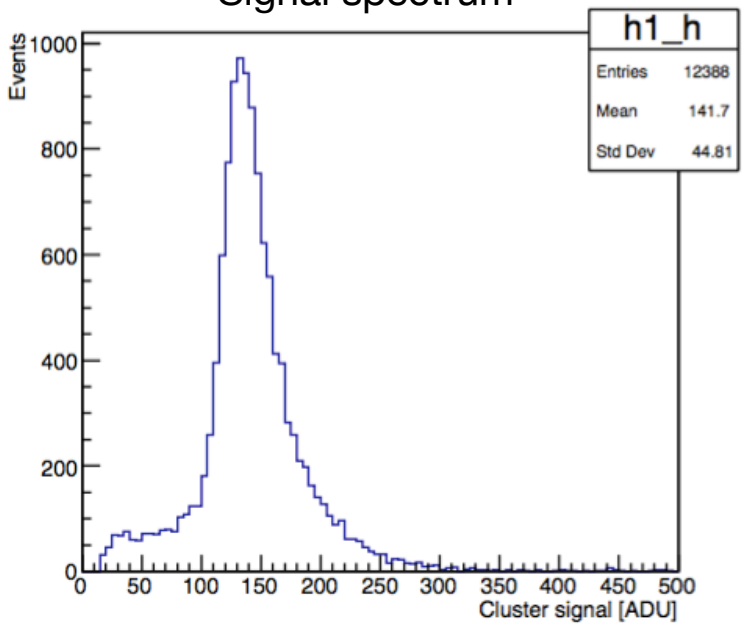
Signal peak: ~420 ADU
Pixel noise: 1.4 ADU/pixel

S_{peak}/N_{pixel} ~300 (@500um thickness)

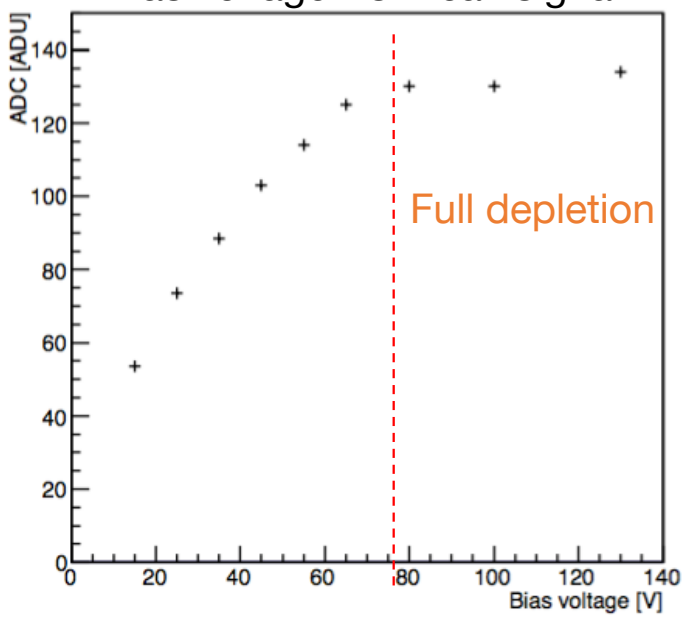
SOFIST Ver.1: HV scan

- Bias voltage dependence of Peak signal
  - Bias voltage: 15 ~ 130V

Signal spectrum



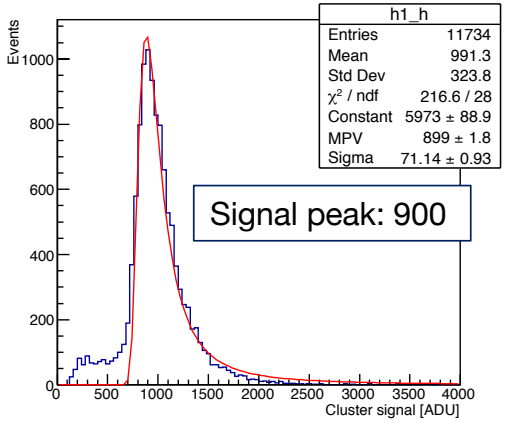
Bias voltage v.s. Peak signal



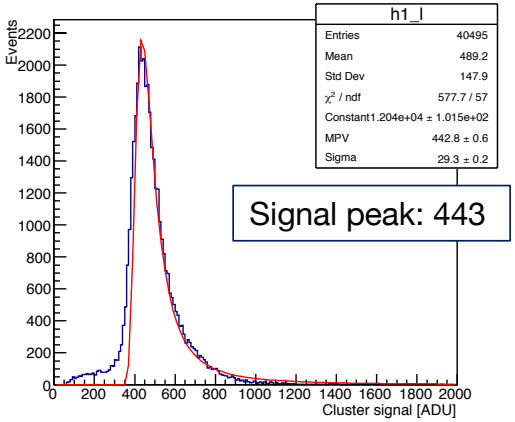
SOFIST Ver.1: Signal spectrum

- Cluster signal spectrum
  - SOFIST setup: External ADC (12 bit), On-chip ADC (8 bit)
  - Bias voltage: 130V (Full depletion), Clustering: 5x5 pixels

External ADC

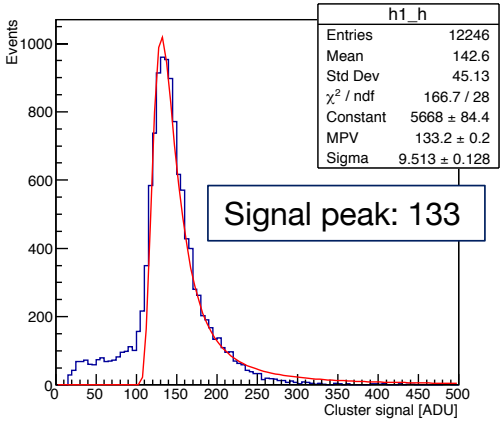


High gain

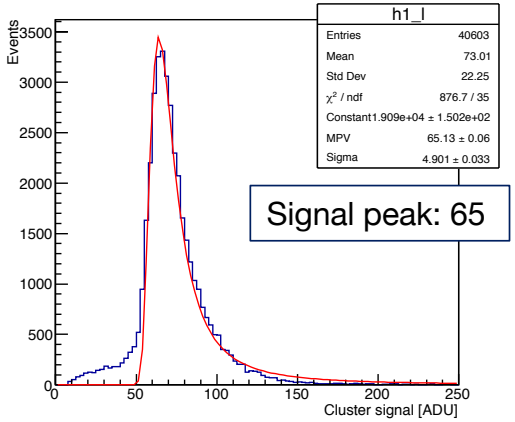


Low gain

On-chip Column ADC



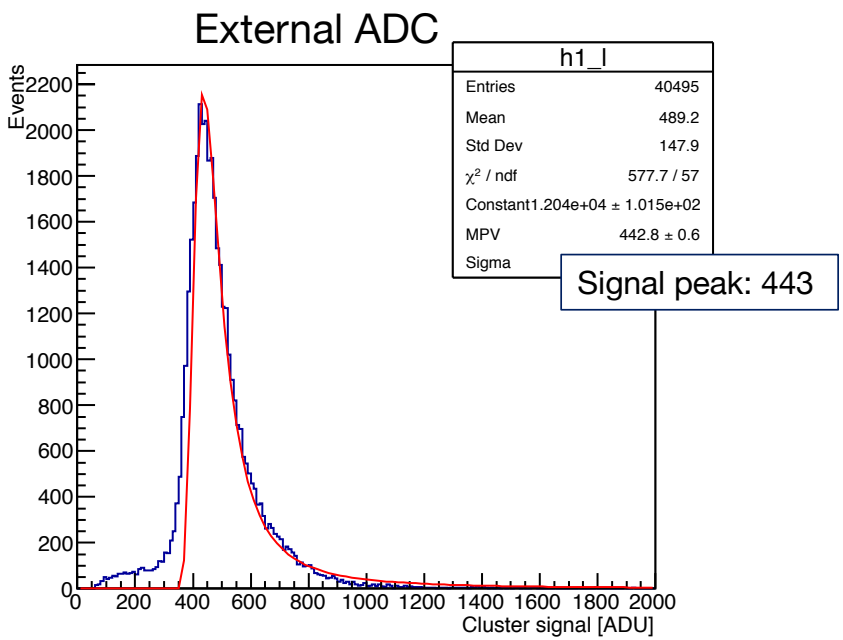
High gain

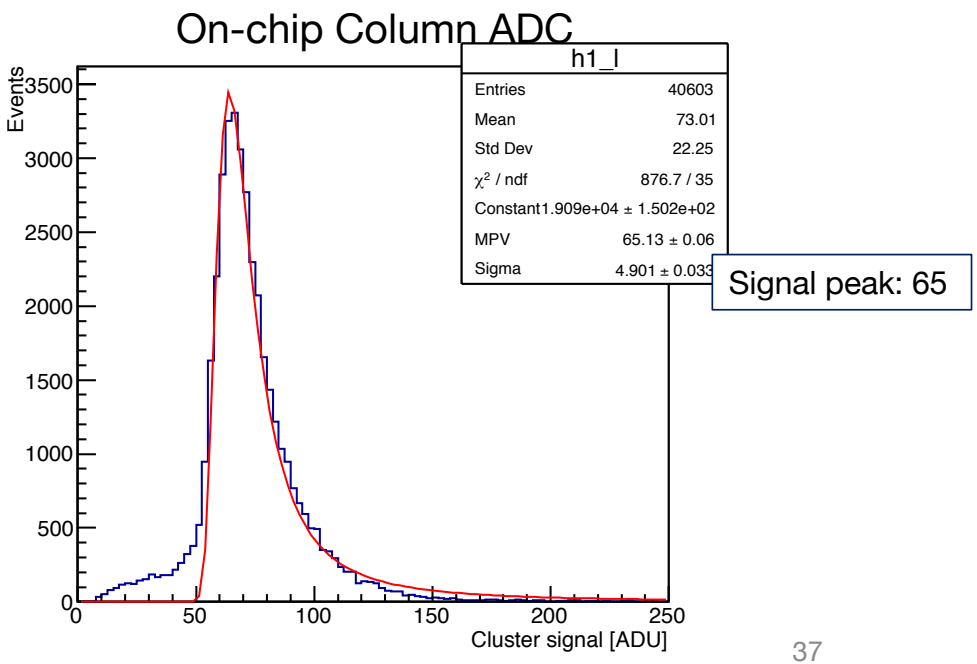


Low gain

SOFIST Ver.1: Signal spectrum

- Cluster signal spectrum
  - SOFIST setup: External ADC (12 bit), On-chip ADC (8 bit)
  - Bias voltage: 130V (Full depletion), Clustering: 5x5 pixels

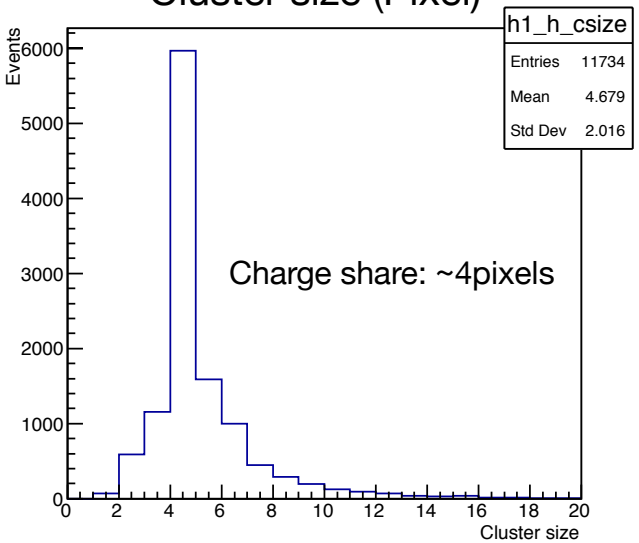




Cluster signal, S/N (High gain)

- Sensor setup
  - Depletion width: ~500 [um] (HV=130V)
  - Readout by External ADC (12bit)

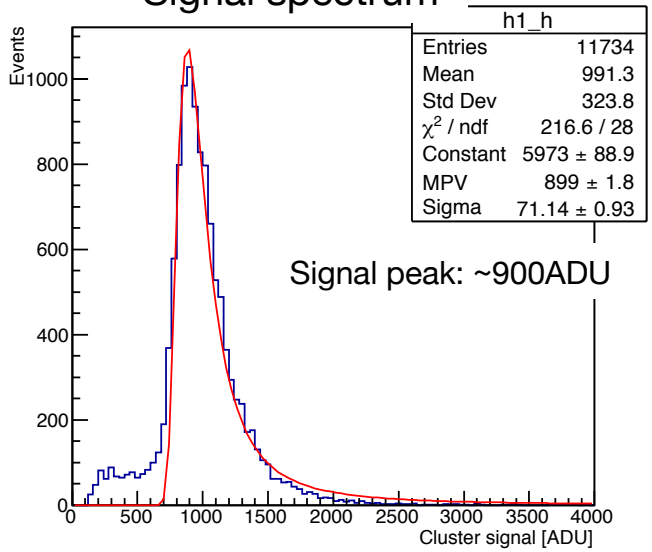
Cluster size (Pixel)



Signal peak: ~900 [ADU]
Pixel noise: 2.2 [ADU/pixel]

- Cluster signal reconstruction
  - Finding hit pixel over threshold
  - Summing 5x5 pixels around hit

Signal spectrum

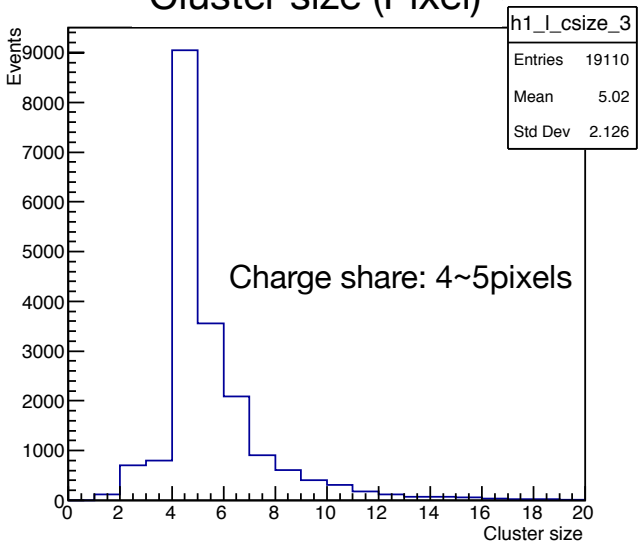


S_{peak}/N_{pixel} ~440 (@500um thickness)

Cluster signal, S/N (Low gain)

- Sensor setup
  - Depletion width: ~500 [um] (HV=130V)
  - Readout by External ADC (12bit)

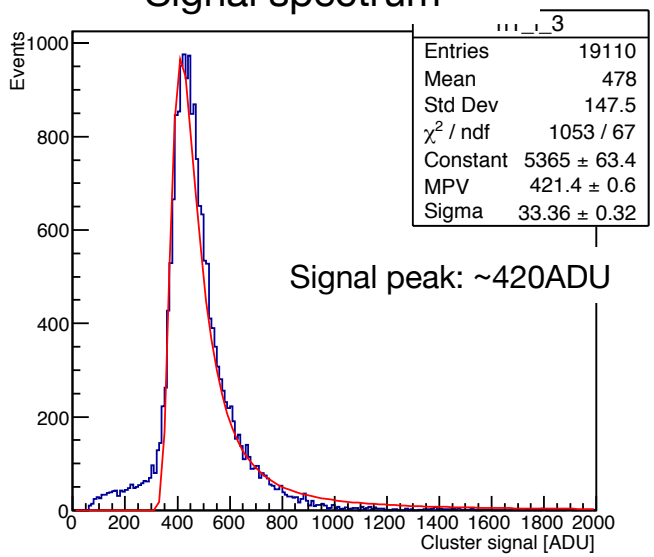
Cluster size (Pixel)



Signal peak: ~420 [ADU]
Pixel noise: 1.4 [ADU/pixel]

- Cluster signal reconstruction
  - Finding hit pixel over threshold
  - Summing 5x5 pixels around hit

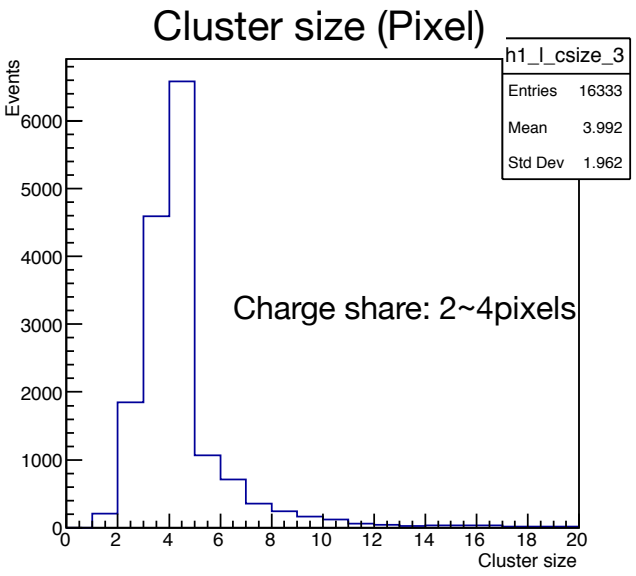
Signal spectrum



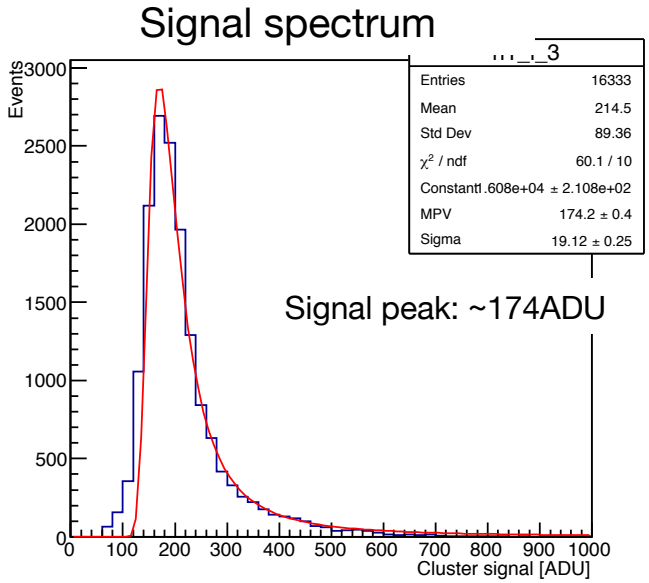
S_{peak}/N_{pixel} ~300 (@500um thickness)

Cluster signal, S/N (Low gain)

- Sensor setup
  - Depletion width: ~200 [um] (HV=20V)
  - Readout by External ADC (12bit)



- Cluster signal reconstruction
  - Finding hit pixel over threshold
  - Summing 5x5 pixels around hit

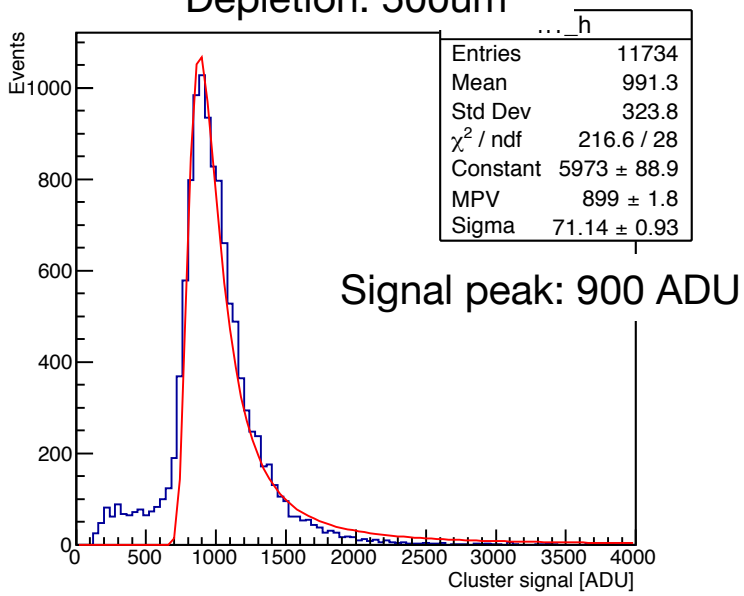


HV scanning:

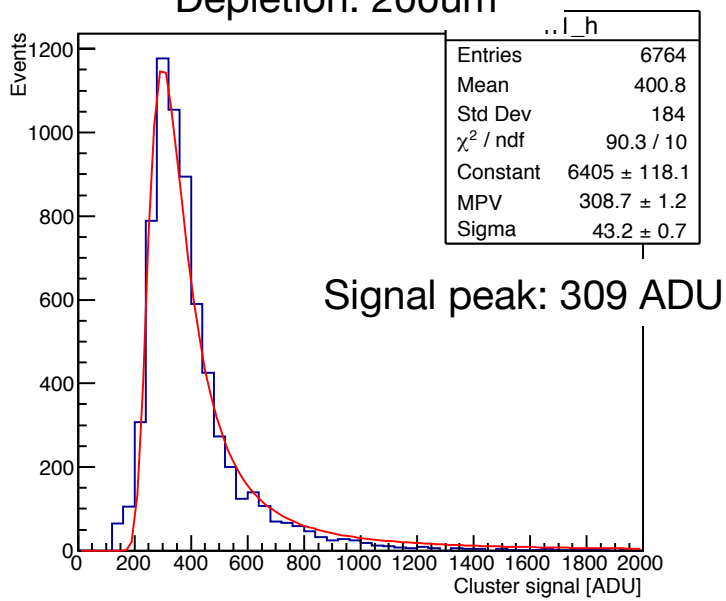
- Evaluation for thinner sensor: High gain
  - HV: 20V, Depletion width: 500um → ~200um

Signal spectrum

Depletion: 500um



Depletion: 200um

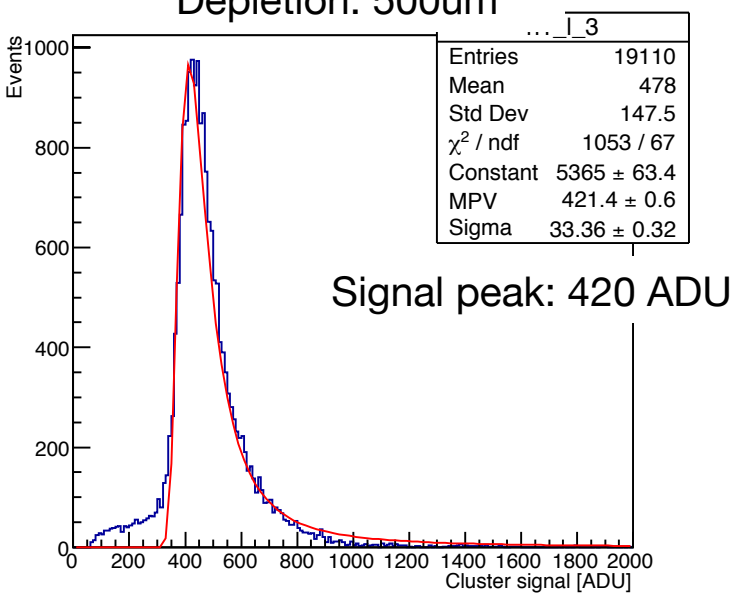


HV scanning:

- Evaluation for thinner sensor: Low gain
  - HV: 20V, Depletion width: 500um → ~200um

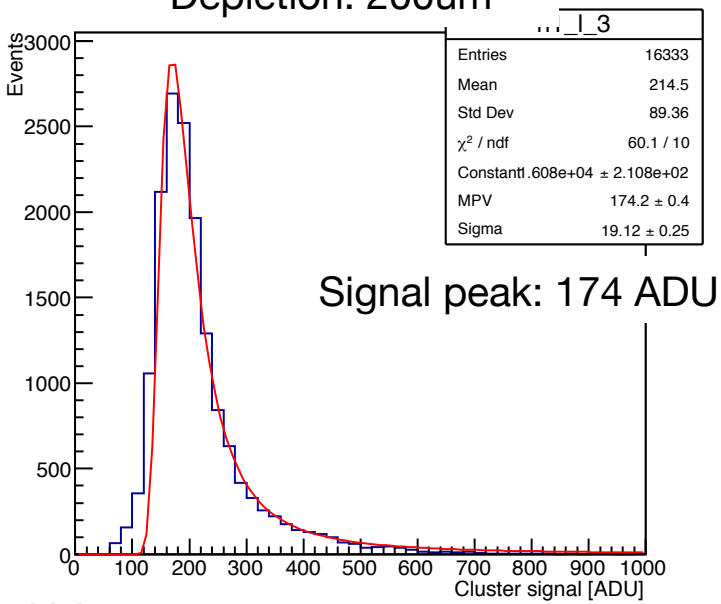
Signal spectrum

Depletion: 500um



Signal peak: 420 ADU

Depletion: 200um



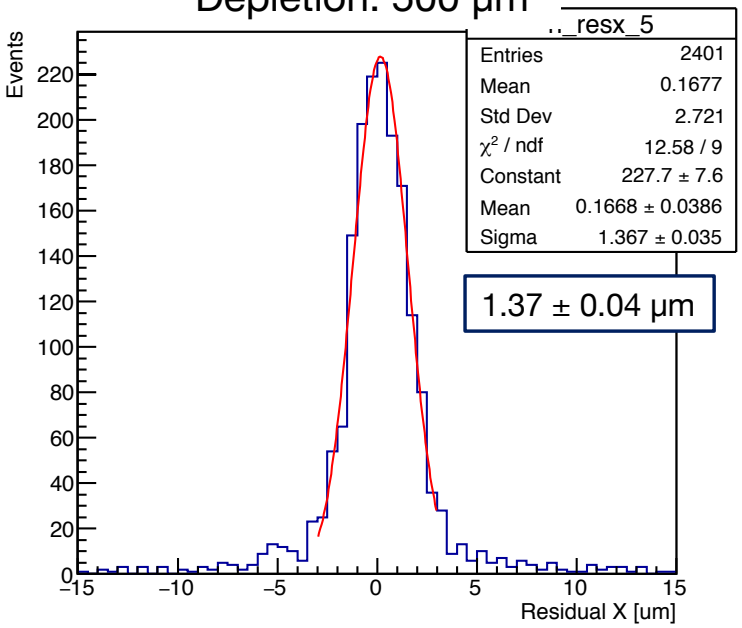
Signal peak: 174 ADU

Residual distribution

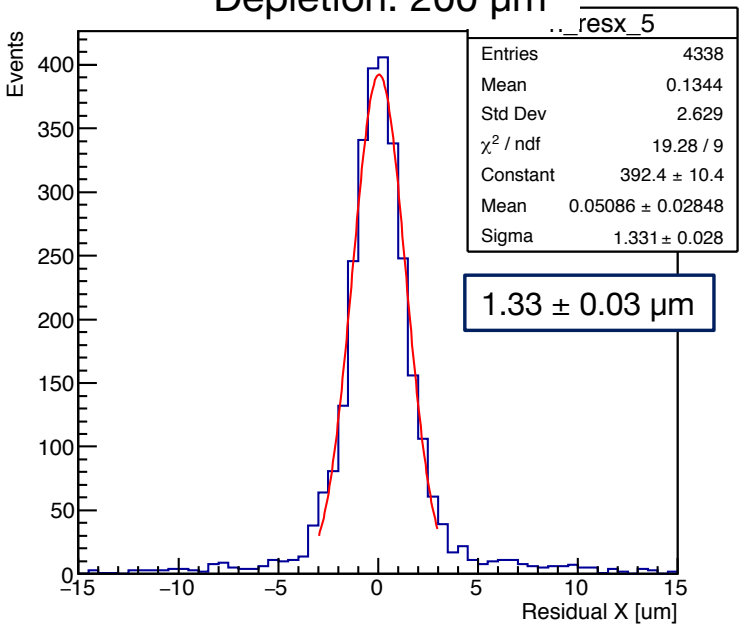
- Evaluation for thinner sensor
  - HV: 20V, Depletion width: 500 μm → ~200 μm

Residual distribution

Depletion: 500 μm

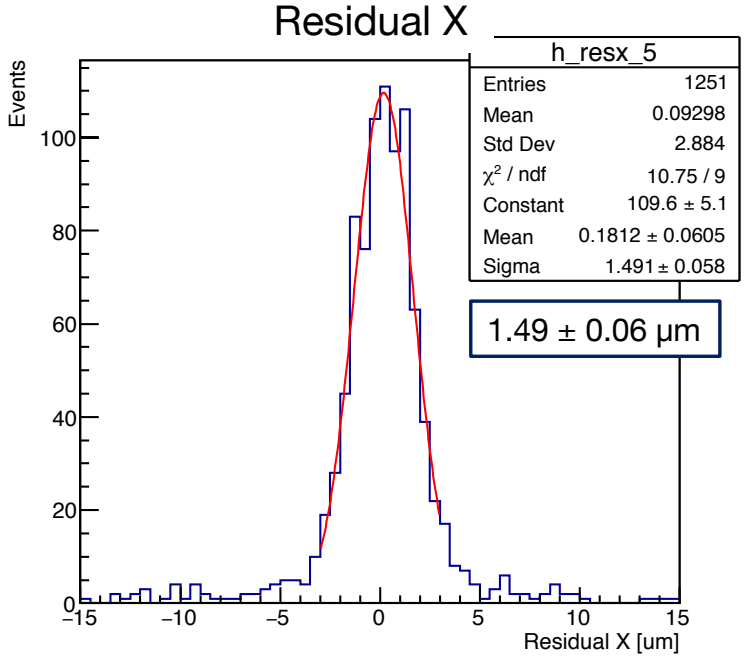


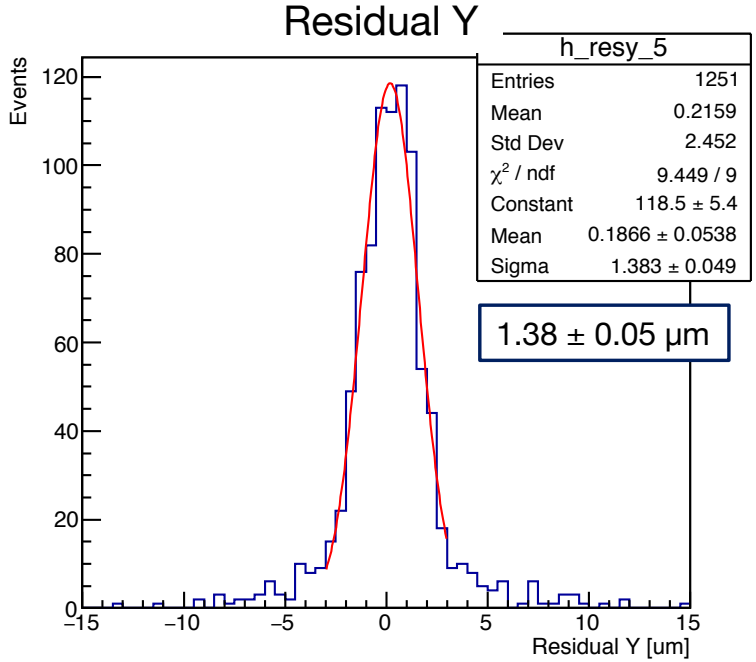
Depletion: 200 μm



Residual distribution

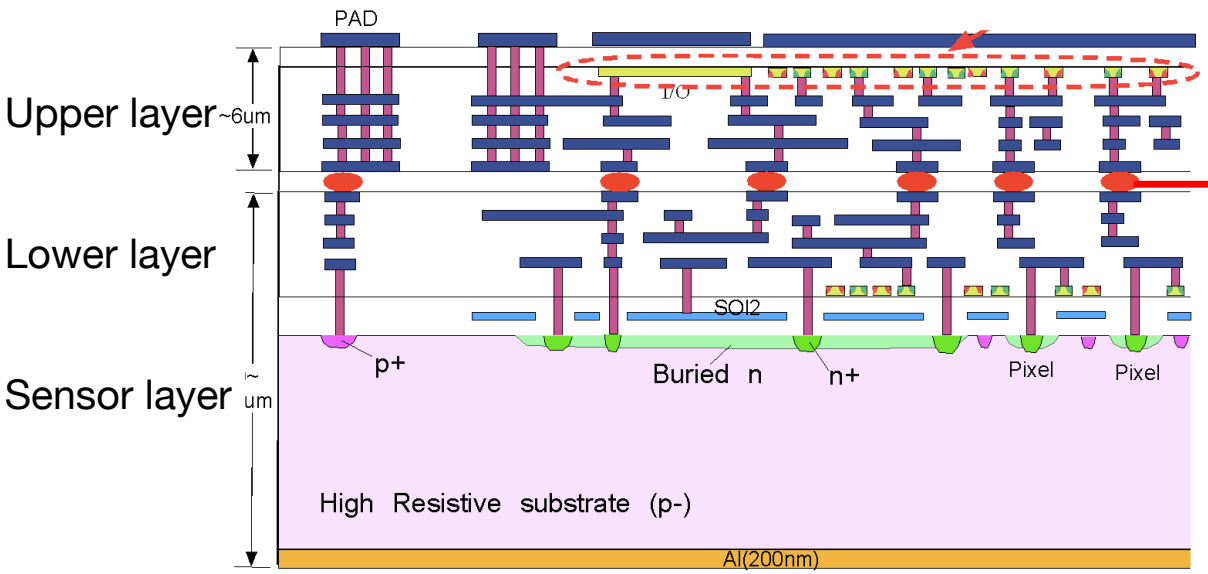
- Sensor setup:
  - Depletion width: ~500 [um] (HV=130V)
  - Readout by On-chip Column ADC (8bit)

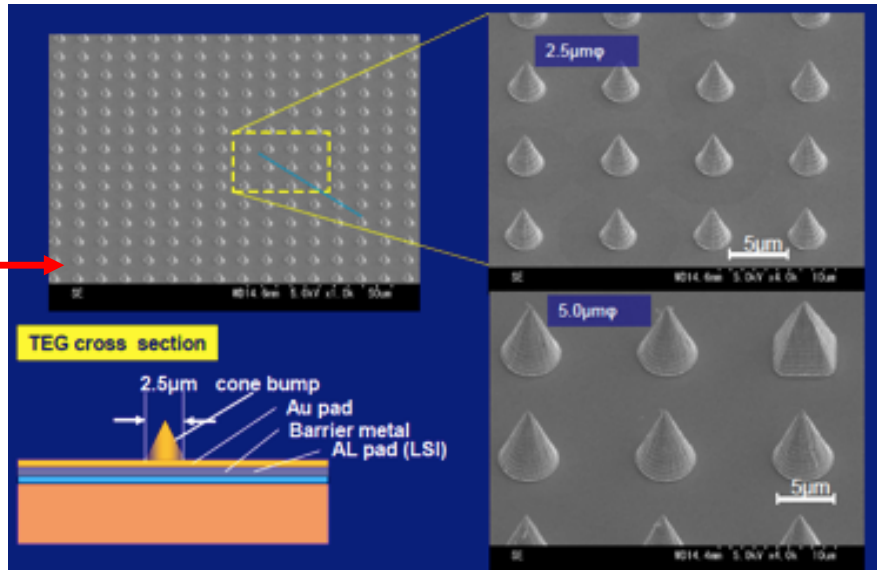




SOI-3D stacking sensor

- Stacking circuit chip on SOI sensor
  - Connecting upper and lower chip by Au cone bump with 5um pitch





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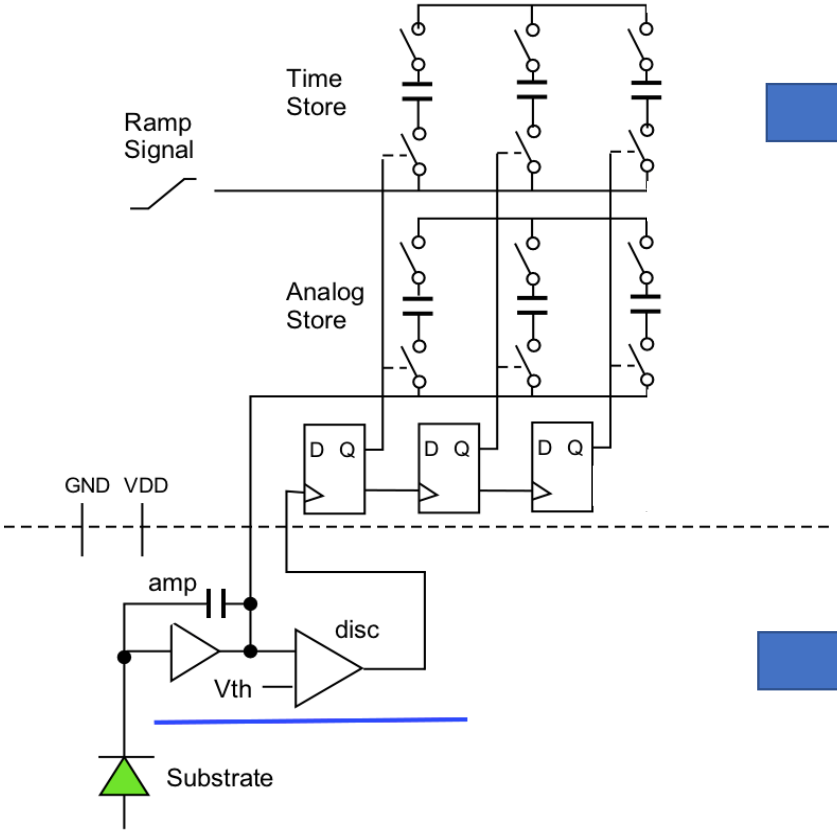
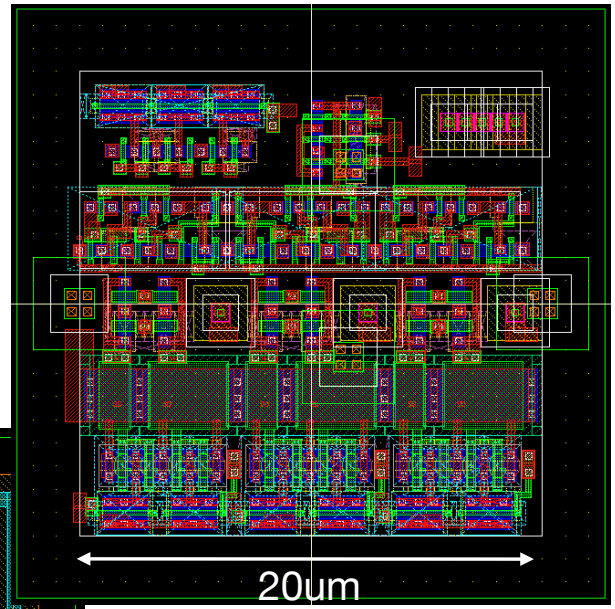
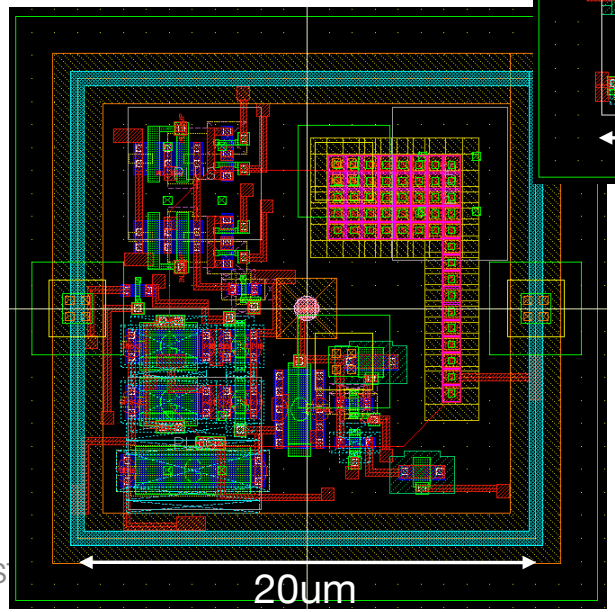
SOI-3D stacking sensor



Upper pixel
- Shift-register
- Analog memory x3
- Timestamp x3

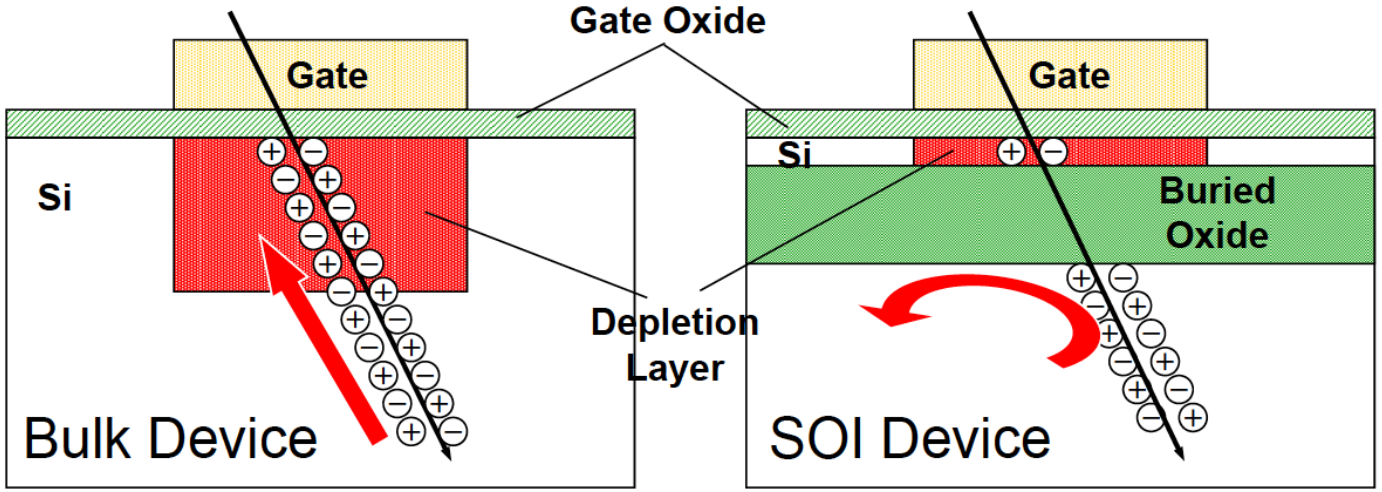




Lower pixel
- Pre-amp
- Comparator

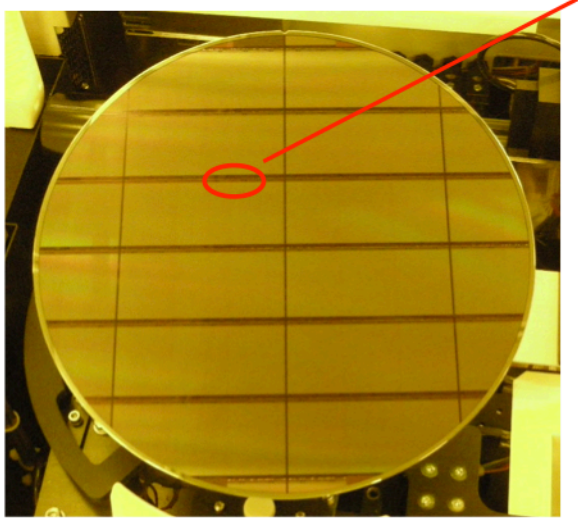
SOI technology

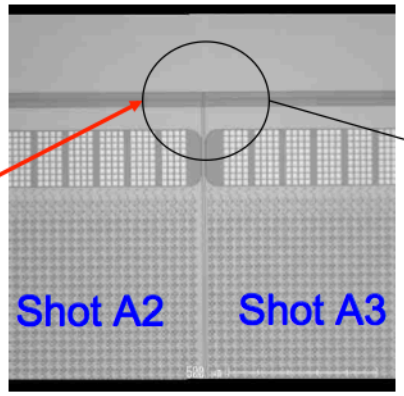
- Suitable for operation in harsh radiation condition
  - Insensitive to Single-event effects because transistors are isolated from the wafer (bulk) silicon.

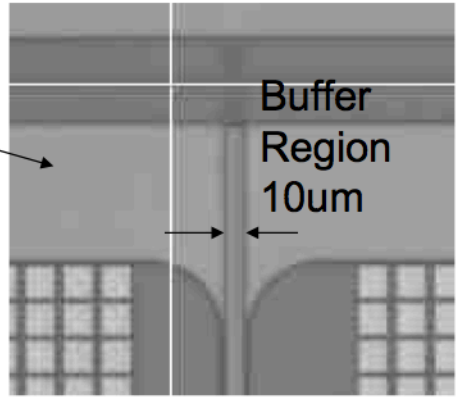


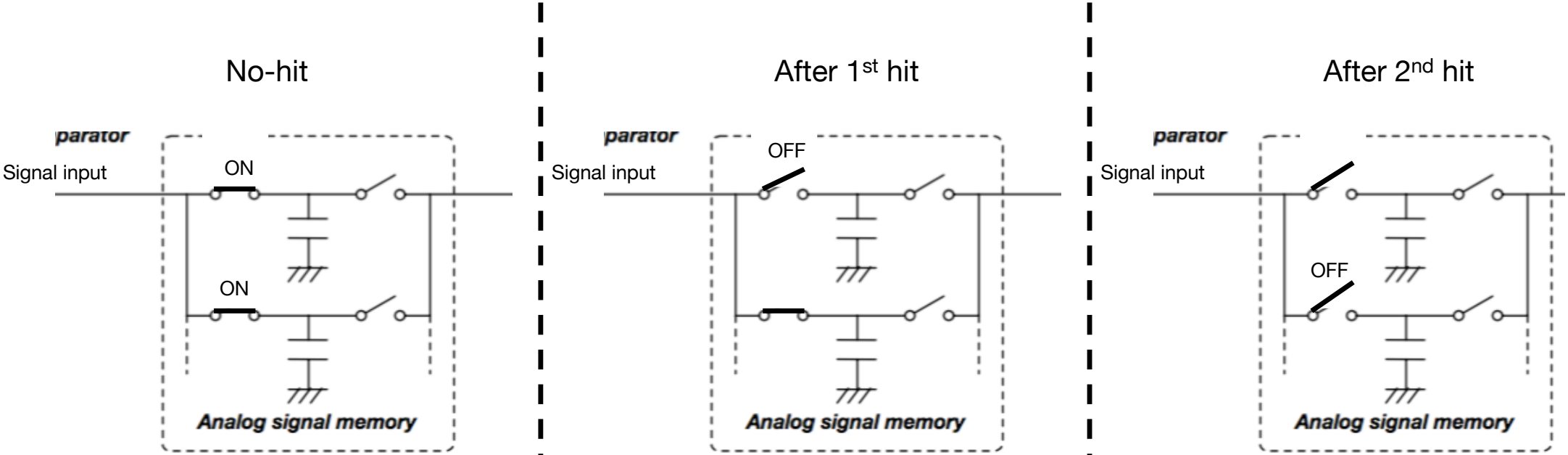
Stitching Exposure for Large Sensor

Produce 26.7 mm x 64 mm Sensing Area (3 Stitching).







- Width of the Buffer Region can be less than 10um.
- Accuracy of Overwrap is better than 0.025um.
- 1-direction stitching at present.

Shift register / Memory