Advances in pixel electronics for experiments with high rate and radiation

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Introduction

• “Pre”cedings: arxiv 1705.10150
• Several topics covered in N. Wermes: “Pixel Detector Overview”
• Other topics have dedicated talks/posters – will point out
• Will focus this talk on readout chip developments:

• High rate and small feature size
• Total dose radiation tolerance and small feature size
• Power delivery
• Data transmission
• Control and operation considerations, including SEU
• Practical IC design model
• Outlook: what needs rethinking?
Obligatory Pileup Slide

LHC Collision Snapshot
Exposure Time = 25ns

~10cm

Raw $\Delta E_T \sim 2$ TeV
14 jets with $E_T > 40$
Estimated PU $\sim 50$
Rate

Particles / Hits

LHC

HL-LHC

* Store full time sequence of drops until trigger (not collect in a bucket)
* Can quantify rate as memory bits / area / time
  (note: no mention of pixel size)
Readout Chip Evolution

- **analog**
  - digital memory & control

- 15 yrs ago: <1 Gbps/cm^2

- 5 yrs ago: 5 Gbps/cm^2

- HL-LHC: 40 Gbps/cm^2

- digital control

An alternate way to say memory per unit area: Logic Density.
Getting to Higher Logic Density

From Hiroshima 09

Future Directions

- Still higher rate capability
- Need smaller, faster pixel
- Yet need more memory per pixel to buffer higher rate
- Two directions to explore: 3D and 65nm
  - FE-I4 region placed on 2 130nm tiers would have 60% pixel size and 50% more logic/memory

<table>
<thead>
<tr>
<th>Pixel Size</th>
<th>Bits</th>
</tr>
</thead>
<tbody>
<tr>
<td>FE-I3</td>
<td>3.2</td>
</tr>
<tr>
<td>FE-I4</td>
<td>25</td>
</tr>
<tr>
<td></td>
<td>~35</td>
</tr>
</tbody>
</table>

Aug 31, 2009

FE-I4 Chip -- Hiroshima 09 -- Garcia-Sciveres
Chip Concept from Pixel 2012

Event processing and system

Digital

HL-LHC

(looks more like commercial chip)
One RD53A Chip Core

One flat synthesized circuit
Each pixel is different!

Whole block is stepped and repeated

~ 200k transistors
Size chosen so it CAN be SPICE simulated

(routing dominated re: metal stack)
Hit Storage Architectures

**T**=Transfer  **W**=Wait

**Move all hits immediately to a big common buffer.**
Wait for trigger there.

**W**=“End of Column Buffer”

**Keep hits in a local buffer.**
Transfer only those triggered.

**W**=“Region”
Hit Storage Architectures 2

- Really two extremes of the same problem
- (*) See poster “A Novel Pixel Region Architecture for Pixel detector at HL-LHC…”

Can imagine this is a core (not how it is in RD53)
Radiation

F. Faccio:  CMOS technologies and power distribution components for HL-LHC: radiation strikes back Wednesday, 13 December 2017 09:00 (30)

Will only talk about how radiation effects have been taken into account in this talk
Rad Hard Logic Density Scaling

28nm ?

65nm
Not quite min. size due to pesky radiation damage. But still 2-3x higher logic density than 130nm.

130nm

0.25um
ELT
There are many dimensions to the radiation damage problem. They all have to be taken into account.

But if you do, you can make a pixel chip that works up to 1Grad.

Analog circuits no problem. Several test chips irradiated this high and work fine.

Digital (small transistors): Operate cold and don’t heat it up under power (just like sensors!), Low dose rate caveat (see tomorrow’s talk).

We will soon have RD53A chips working after 1Grad.

We only guaranteed specs up to 500Mrad, because that’s what we could simulate, and this was using pessimistic models.

Radiation damage simulation in the digital design process is now a necessity. Development of more accurate models is an ongoing process.
Data-Simulation Comparison

- Comparison of models used in RD53A chip with test chip data.
- Ring oscillator frequency is sensitive to TID effects
- Different logic cells can be used to make ring oscillator test structures
- Models were built from single transistor data under DC worst case bias.
- A switching transistor is less vulnerable. We see 2x less damage.

Ring Oscillator frequencies 9T_NVT
Power distribution

- On-module power conversion needed as detectors get larger
- But not yet used in any running detector
- Will be a feature in HL-LHC ATLAS and CMS trackers

- In the case of pixels this will be done with serial power
- In-chip DC-DC was the alternative- but was not developed to maturity
- Off-chip DC-DC not suitable for pixel modules: too massive

- Successful demonstrations of serial power since many years
- Will not review. Will show the scheme adopted by RD53
Resistive Serial Chain 101

Should $R = \frac{V_{\text{chip}}}{I_{\text{chip}}}$?

- Narrow operating current range
- Significant power overhead
- Low open-fault tolerance
- $V$ transients can be dangerous

\[ \text{dV} = +\frac{IR(n-m)}{nm} \]

\[ \text{dV} = -\frac{IR}{n} \]
Zenner-like using V-offset

- $R \ll \frac{V_{\text{chip}}}{I_{\text{chip}}}$
- Wide operating current range
- Reduced power overhead
- Tolerates multiple faults per module
- Vo matching important
- No different for shorted module

$\Delta V \ll \text{module } V$
(same formula, smaller $R$)
RD53A chip regulator schematic
Data Transmission

- On-module power conversion reduces the power cable plant
- At the same time, output bandwidth goes up a lot (pileup x trigger rate)
  - ATLAS IBL chip output = 160 Mbps
  - HL-LHC ATLAS/CMS inner layer chip output = 5.12 Gbps
- Direct chip to optical fiber, Grad rad hard, low power, miniature technology not available
- Data cables become the dominant services mass problem

- Solution: fit as much data as possible onto low mass cables
- Many complications to be overcome
- A very active development area
- Industry very far ahead- learning and catching up to be done
Data Transmission Problems/R&D Areas

- Low mass, high bandwidth cables and connectors
  - Many options at 1Gbps for length ~1m.
  - Few options for 5Gbps for length 1-5m.
- Reliable recovery of signals from lossy transmission lines
  - Pre-emphasis and equalization
  - Transmitters on modern FPGA can recover signals after -28dB loss.
  - With radiation, less advanced circuits, added clock jitter, etc, it will be challenging for us to achieve recovery after -20dB loss.
- High speed serialization on chip
  - next slide
- Data encoding and data compression
  - 8b/10b was considered pretty advanced for HEP a few years ago
  - RD53A has multi-lane 64b/66b output
  - Multi-level, PAM-4, PAM-16 not yet explored
  - Compression algorithms such as Huffman being explored by not yet used
High Speed Serialization on Chip

- Need a high quality clock (<15ps jitter for 5 Gbps, <75ps for 1 Gbps)
  - Problem: no high quality, high speed clock coming in
  - Adding one means adding mass
  - PLL multiplication used, but hard to achieve very low jitter, especially after radiation

- Need a high speed serializer that remains high speed after radiation damage
- Need fast recovery from SEU
- 1 Gbps seems achievable after irradiation, 5 Gbps still a challenge
- This means HL-LHC inner layer chips must have 4 output lanes
- LHCb Velopix uses 4x 5Gbps lanes, but less radiation, good incoming clock, and high quality output cables.
- LpGBT can run at 10Gbps, but high speed low jitter incoming reference signal, and less radiation.
Control

- Take advantage of high logic density to implement smarter control functions
- Chip becomes fairly intelligent and “user friendly” to control
- Learn from present operational issues and design a control protocol where they do not arise
  - See earlier ATLAS and CMS pixel operation talks
- In general, SEU’s cause all kinds of exceptions that the DAQ protocol does not easily recover from.
  - Will never manage to prevent SEU- it will only get worse in the future
  - Solution: design protocols that are compatible with SEU’s
  - No long-term memory in the chip: refresh configuration all the time from outside during data taking
    - “Trickle configuration” already supported in RD53A
  - Make no use of counter absolute values- only differences matter so upsets fix themselves when counters loop.
    - “Tagged trigger” protocol already supported in RD53A
New concerns: Low dose rate is not so low

1 Mrad per run at HL-LHC! But dose rate here was ~5x higher than at HL-LHC

Threshold Dispersion vs. Dose

Automated, continual threshold self-tuning would address this
Shift in Design Approach

analog

digital memory & control

analog digital analog digital analog digital digital

digital control

looks more like commercial chip

FE-I4

Participating institutes:

CPPM: D. Fougeron, M. Menouni.
Genova: R. Beccherle, G. Darbo.
Nikhef: V. Gromov, R. Kluit, J.D. Schipper

Nov. 2017 RD53 meeting, CERN

Commercial style design and validation 10^9 transistor Chips work the first time
Where next?

Still a couple of years to go for RD53 to make production chips for ATLAS & CMS

And after that?

- Higher logic density (28nm)
- Higher radiation dose
- Smaller pixels
- More functionality

- R&D into smaller features
- Followed by another collaboration to make next gen. chip

What for?

Replacement of HL-LHC inner layers, FCC
Smaller pixels and resolution

- Refer back to W. Snoey’s talk...

- Single pixel gets “easier” due to smaller capacitance (eg. no timewalk)
- But total power budget gets more challenging (capacitance per unit area goes up- scales with perimeter, not area)
- At what point should we go binary?
  - See poster: “Ultimate position resolution of pixel clusters with binary readout...”
- High bandwidth data transmission. Data compression.
Conclusions

- High rate (*) needs high logic density (hybrid>monolithic forever)
- Digital design flow and tools needed to make $10^9$ transistor chips that work the first time
- Design collaboration model probably here to stay
- High radiation needs high radiation tolerance-
  - Some tension with high density- see F. Faccio’s talk
- High logic density comes with huge functionality potential- have to keep thinking of what to do with it
- (*) readout bandwidth limited. Will likely stay that way