High Resolution SOI Pixel Detector
~ overview ~

Dec. 11, 2017, HSTD11 & SOIPIX2017@OIST

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on behalf of SOIPIX Collaboration

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& Okinawa Institute of Science and Technology (OIST)

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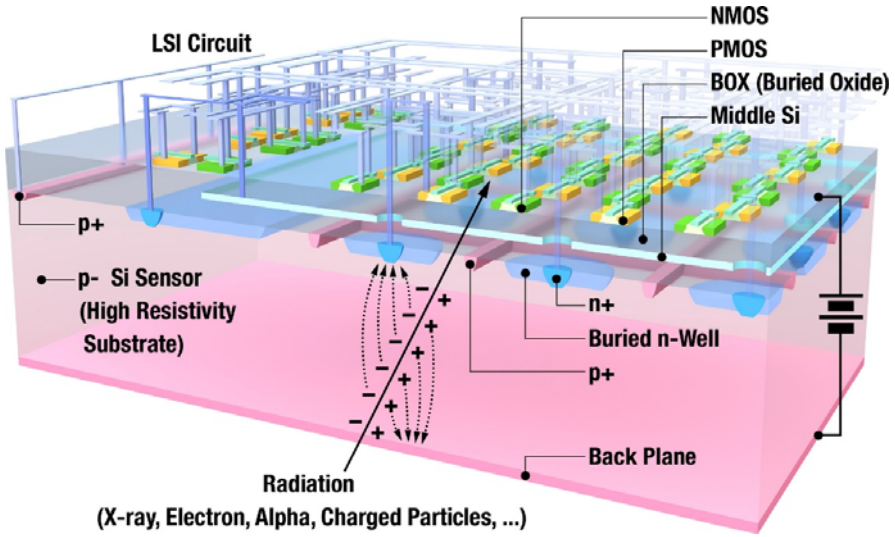
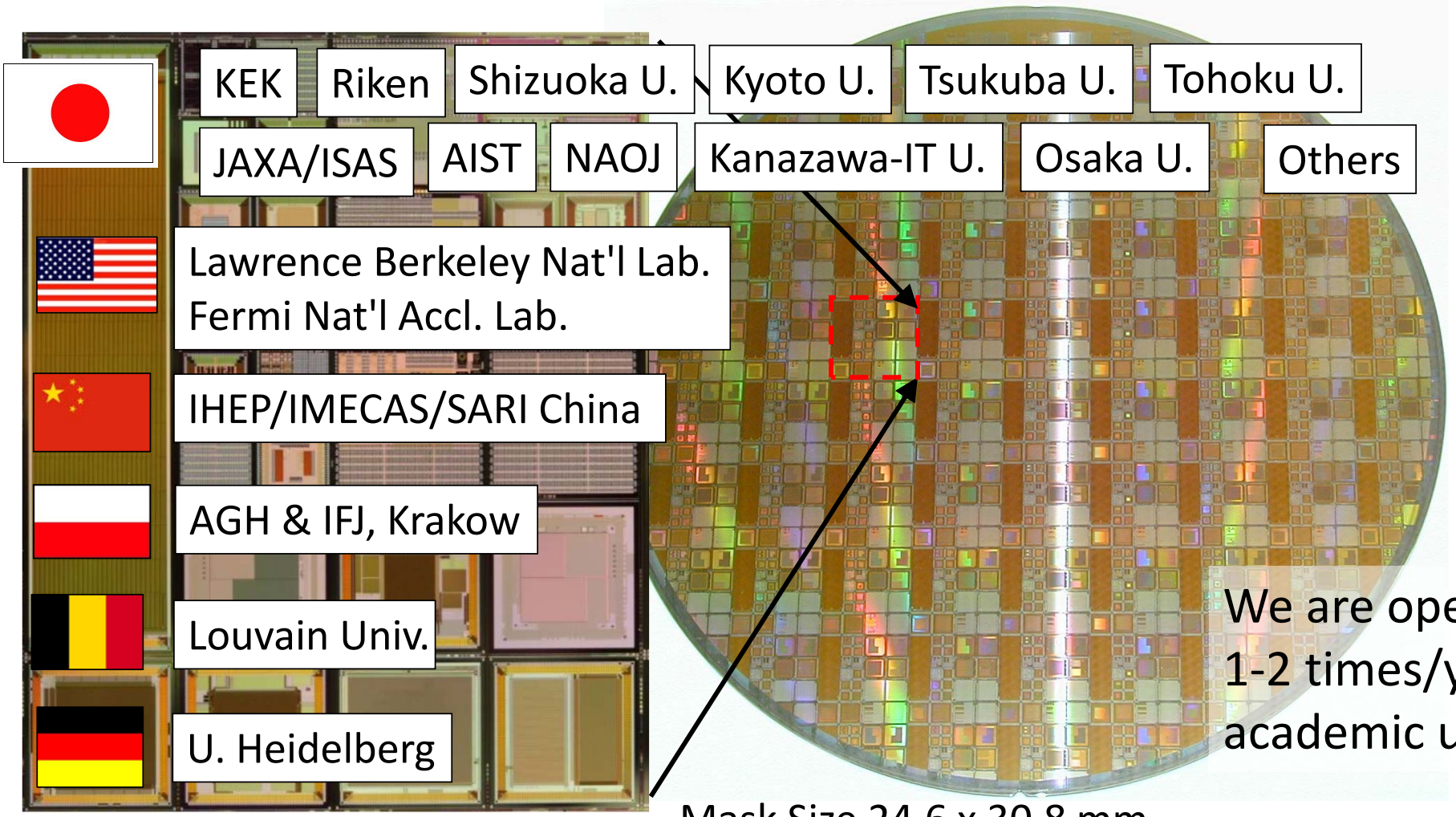
Outline of Presentation

- Introduction
- SOI Pixel Process
  3 process refinements
  - Buried Well
  - Double SOI
  - Pinned Depleted Diode
- Performance Examples of the Detector
- Summary



1st International Worksop on SOI Detector (SOIPIX2015) @Sendai, June 3-6, 2015

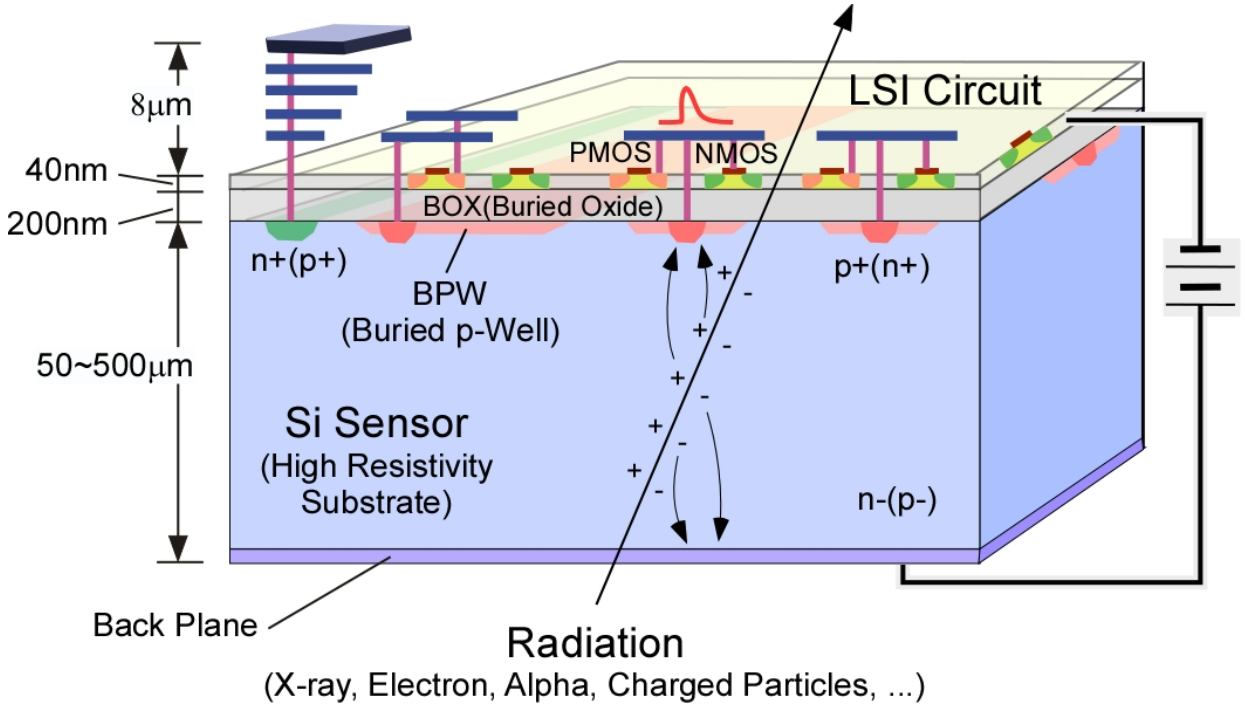
SOIPIX MPW (Multi-Project Wafer) run



We are operating 1-2 times/year for academic users.

Mask Size 24.6 x 30.8 mm

Silicon-On-Insulator Pixel (SOIPIX) Detector



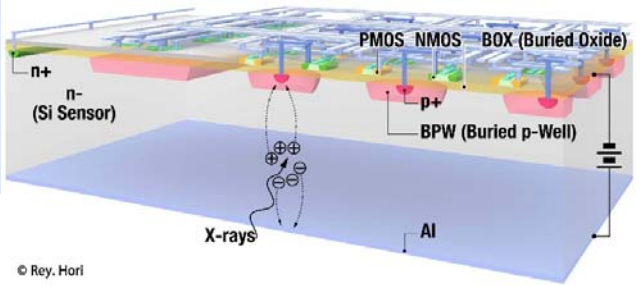
Our challenge for SOI pixel have started in 2005.
Monolithic Detector having fine resolution of silicon process and high functionality of CMOS LSI by using a SOI Pixel Technology.

Lapis Semiconductor 0.2 μm FD-SOI Pixel Process

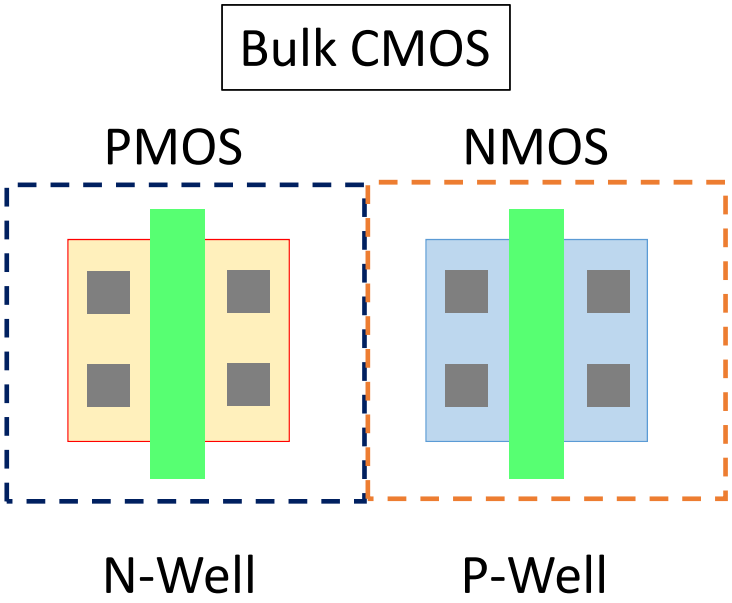
Process	0.2 μm Low-Leakage Fully-Depleted SOI CMOS 1 Poly, 5 Metal layers. MIM Capacitor (1.5 fF/um^2), DMOS Core (I/O) Voltage = 1.8 (3.3) V
SOI wafer (single)	Diameter: 200 mmϕ, 720 μm thick Top Si : Cz, ~10 Ω-cm, p-type, ~40 nm thick Buried Oxide: 200 nm thick Handle wafer: Cz (n) ~700 Ω-cm, FZ(n) > 2k Ω-cm, FZ(p) ~25 k Ω-cm etc.
Backside process	Mechanical Grind, Chemical Etching, Back side Implant, Laser Annealing and Al plating

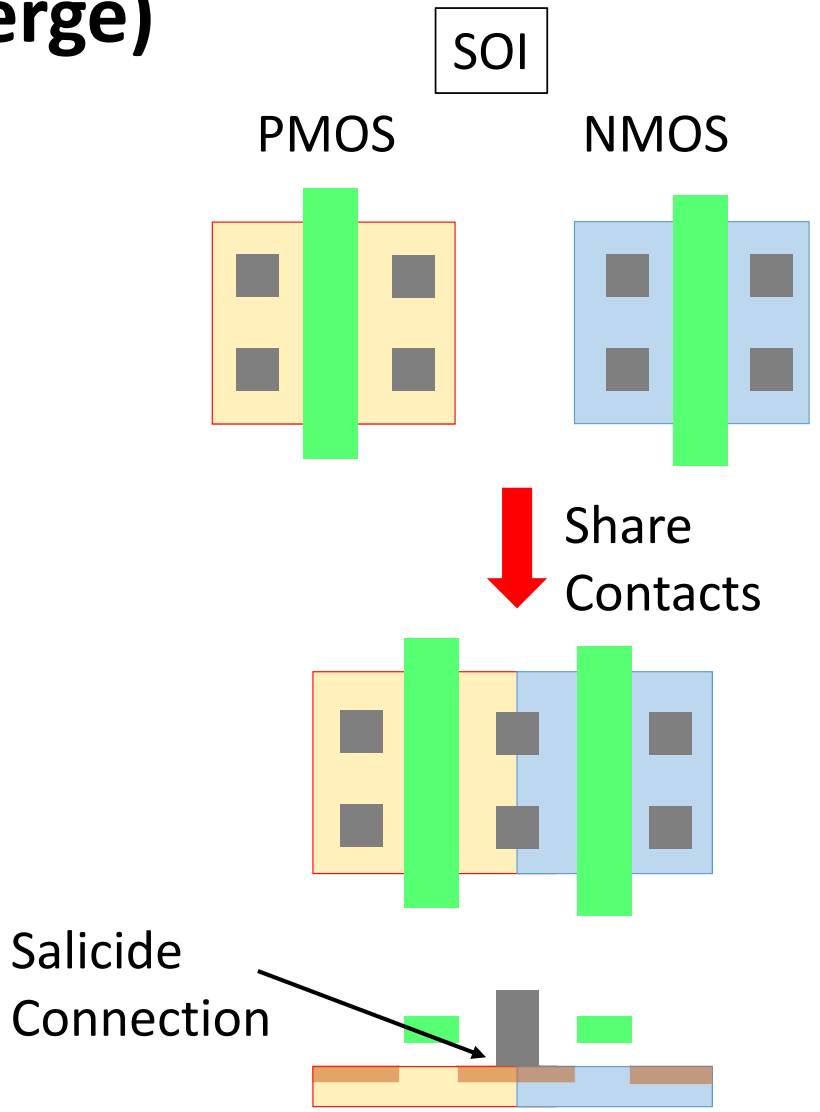
Features of SOI Pixel Detector

- Monolithic device. No mechanical bonding. Small pixel size.
- Fabricated with semiconductor process only.
  → High reliability and Low Cost.
- High Resistive fully depleted sensor (50um~700um thick) with Low sense node capacitance. → Large S/N.
- On Pixel processing with CMOS circuits.
- No Latch up and very low Single Event cross section.
- Can be operated in wide temperature (1K-570K) range.
- Based on Industry Standard Technology.



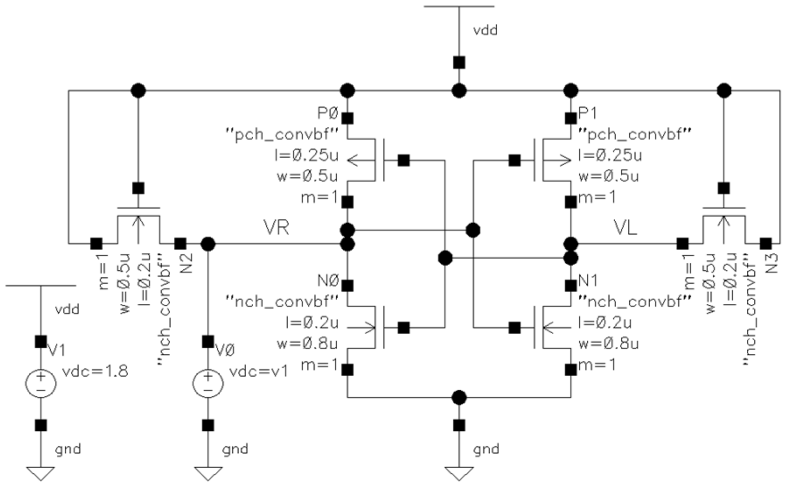
Layout Shrink（Active Merge)

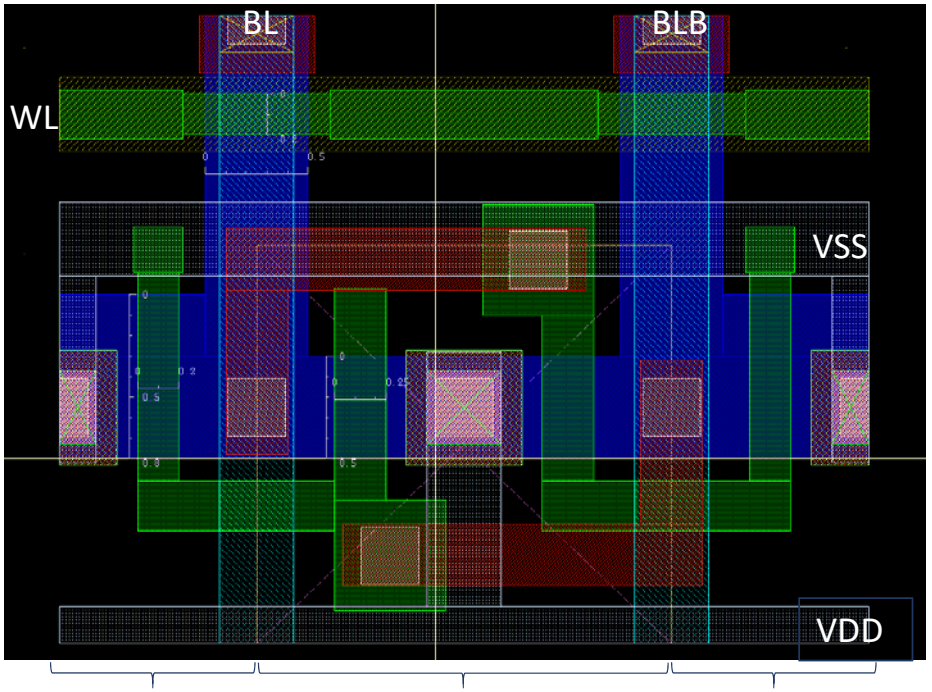




In the SOI process, it is possible to merge NMOS & PMOS Active region and share contacts.

Single Port SRAM Bit Cell with Active Merge Technique



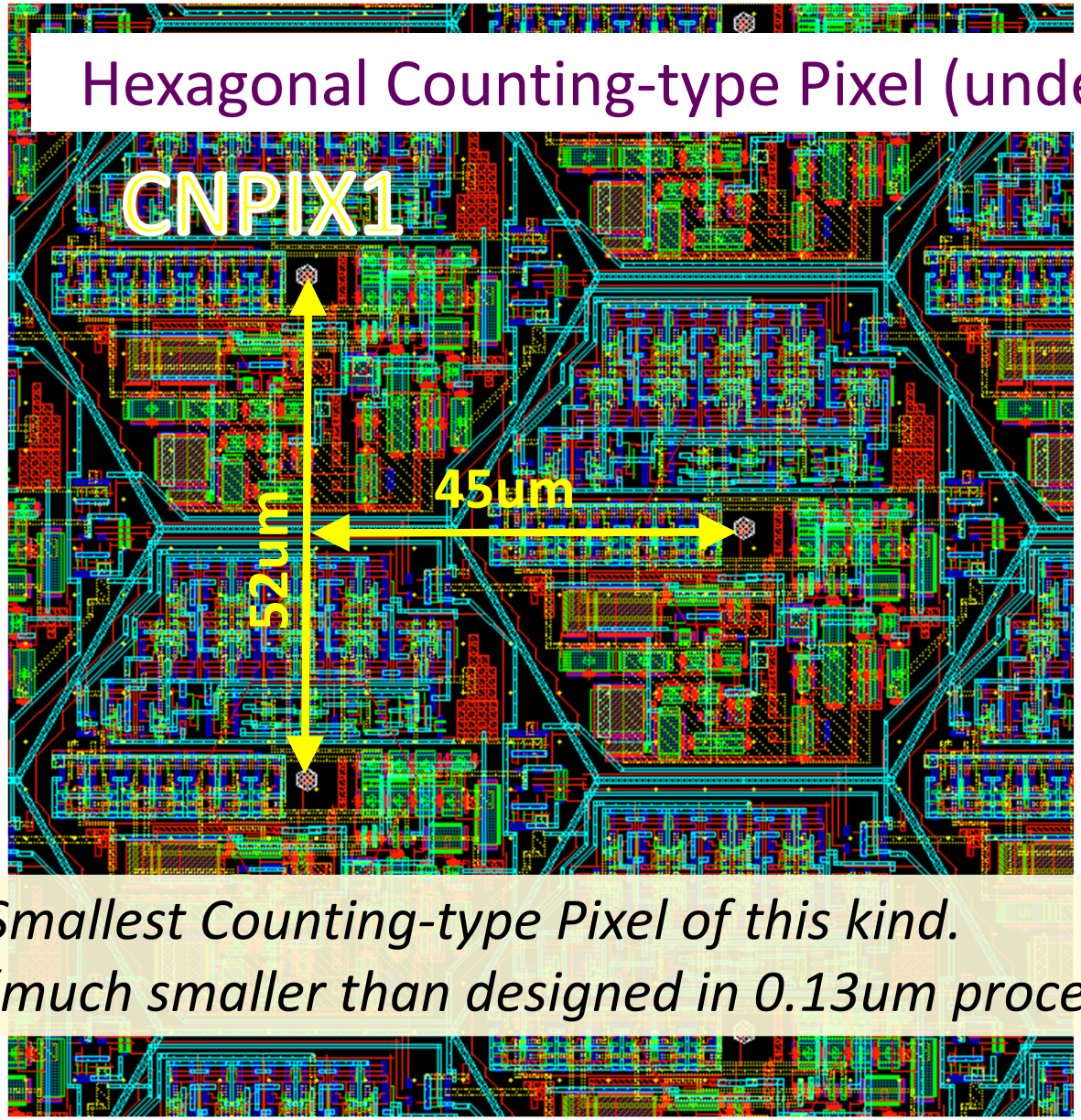


Only 1 Active region

Nch Pch Nch

Cell Size :
3.94 mm X 3.06 mm = 12.06 mm^2

Hexagonal Counting-type Pixel (under development)



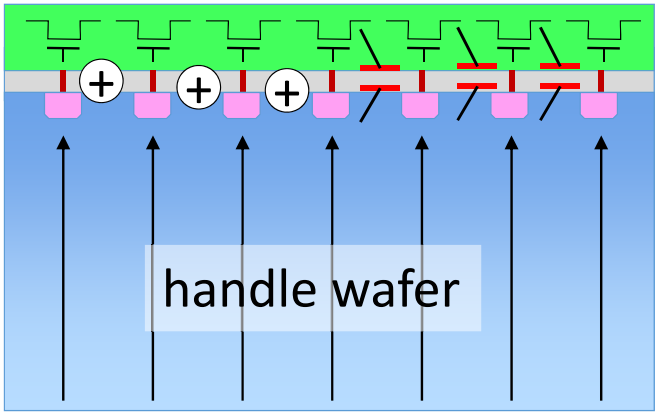
Smallest Counting-type Pixel of this kind.
(much smaller than designed in 0.13um process)

Charge Amp
+
Shaper
+
Discriminator
+
Q Share Handling
+
19bit Counter
+
7bit register

(in 2,340 um^2)

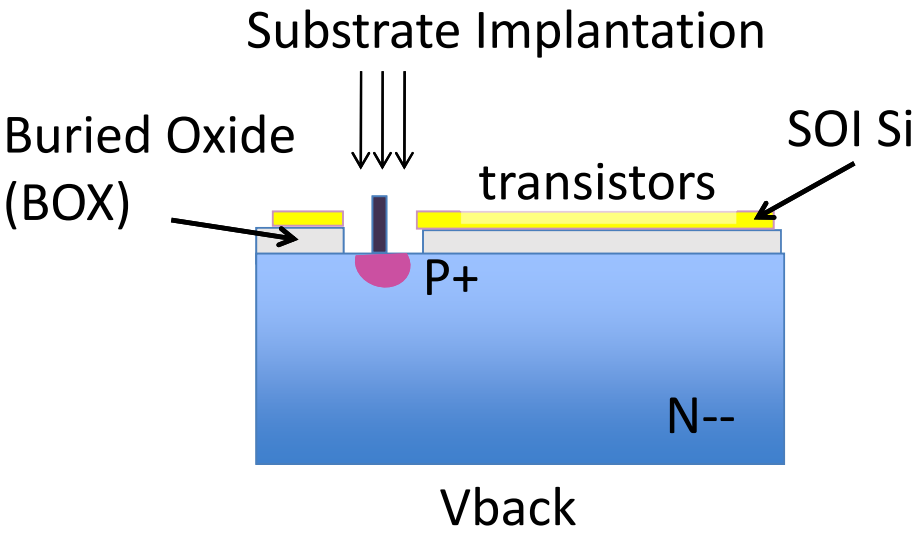
(With IHEP China)

Main issues in SOI Pixel

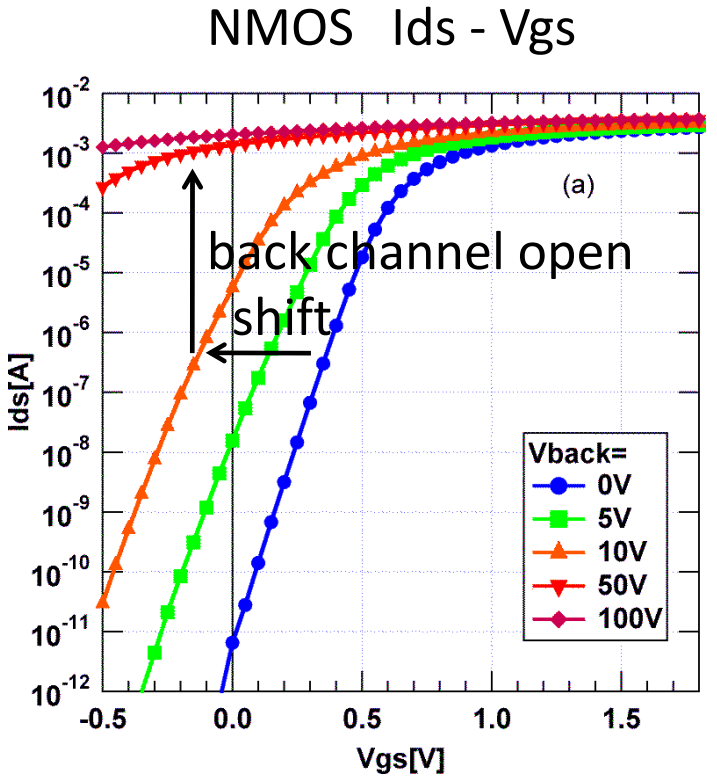


- Transistors does not work when high-voltage is applied to handle wafer. (Back-Gate Effect)
- Circuit signal and sense node couples. (Signal Cross Talk)
- Oxide trapped hole induced by radiation will shift transistor threshold voltage. (Radiation Tolerance)

Back Gate Effect

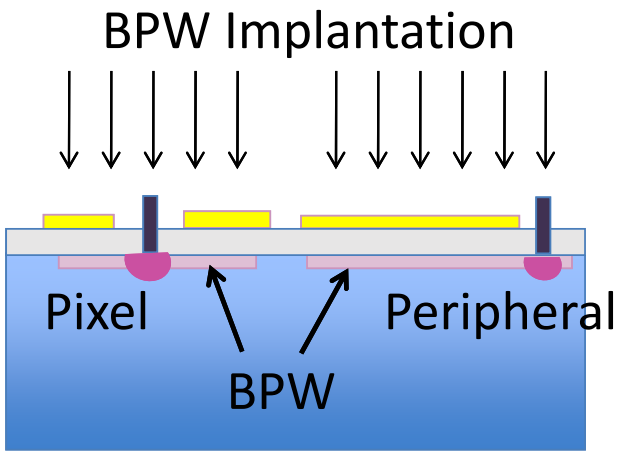


- Make P-N junction by cutting top SOI Si and BOX.
- Then implant impurity with high density.



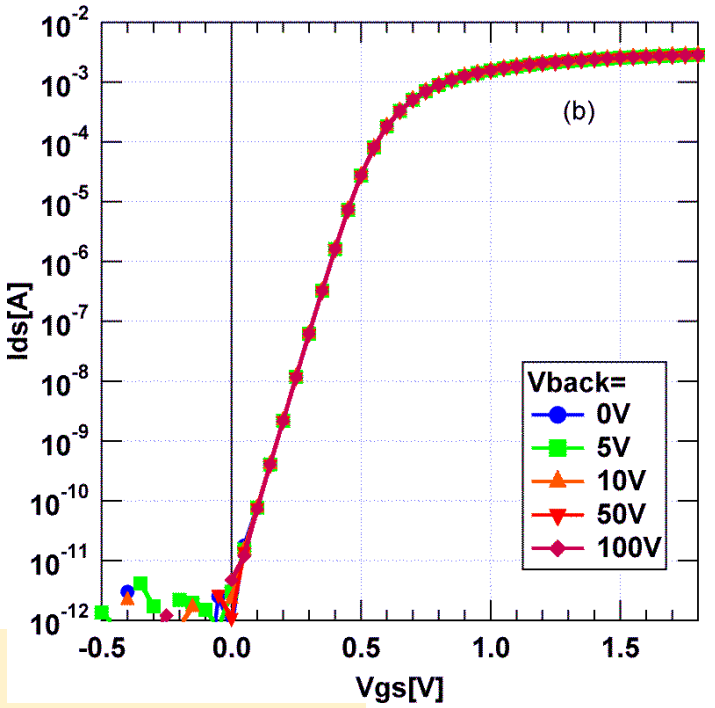
With biasing high-voltage to the backside of substrate, Leakage current will increases.

1st refinement: Buried p-Well (BPW)



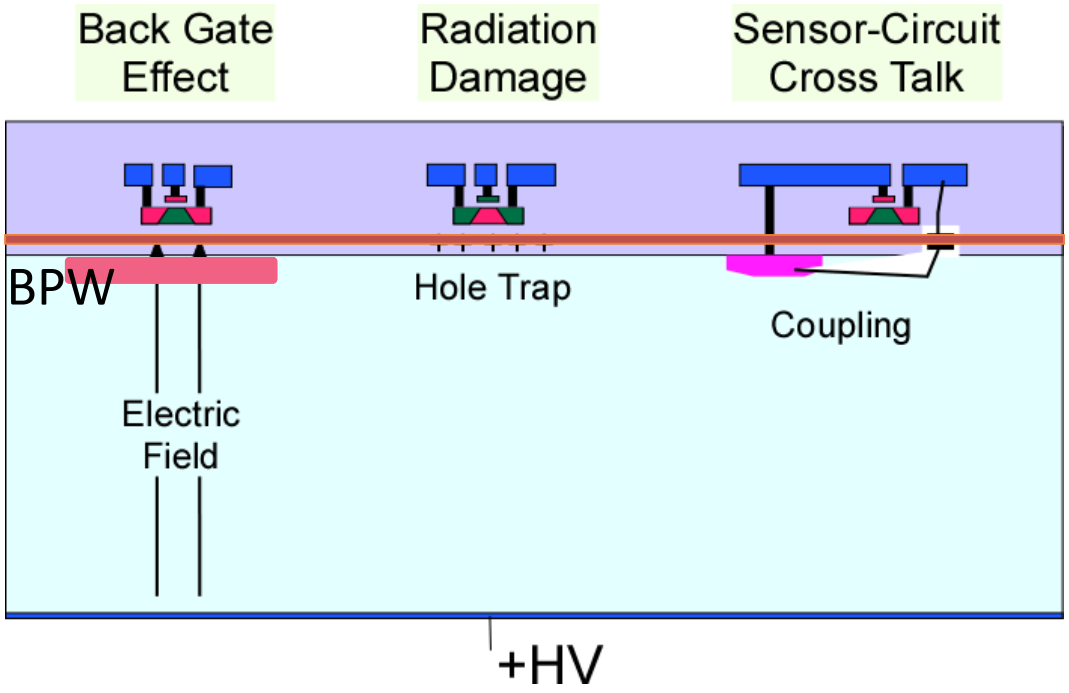
- Keep Top Si not affected
- Low Dose

NMOS Ids – Vgs with BPW=0V



- Suppress the **Back Gate Effect**.
- Shrink pixel size without loosing sensitive area.
- Increase break down voltage with low dose region.
- With biasing middle Si layer, radiation hardness is improved.

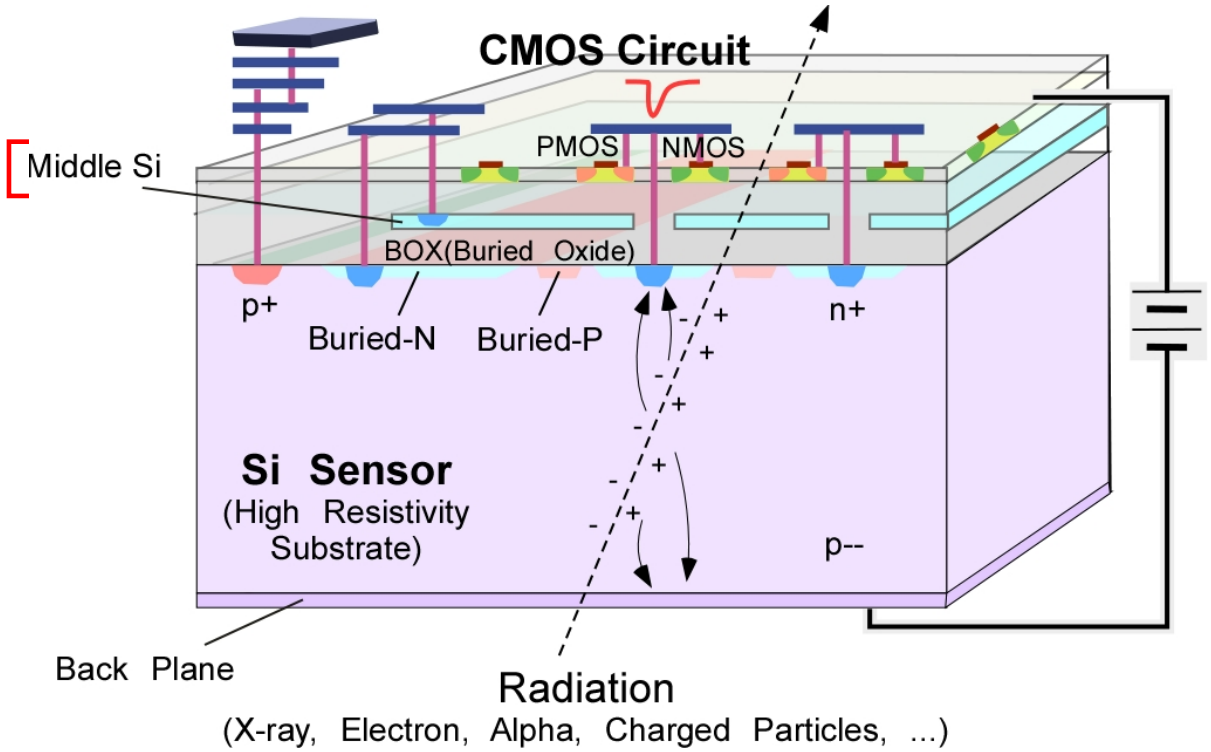
Main Issues in SOI detector (cont.)



The BPW layer solved the back gate issue, but other issues are not yet solved.

Then we introduced additional conductive layer under the transistors (→ Double SOI).

2nd refinement: Double SOI (DSOI)

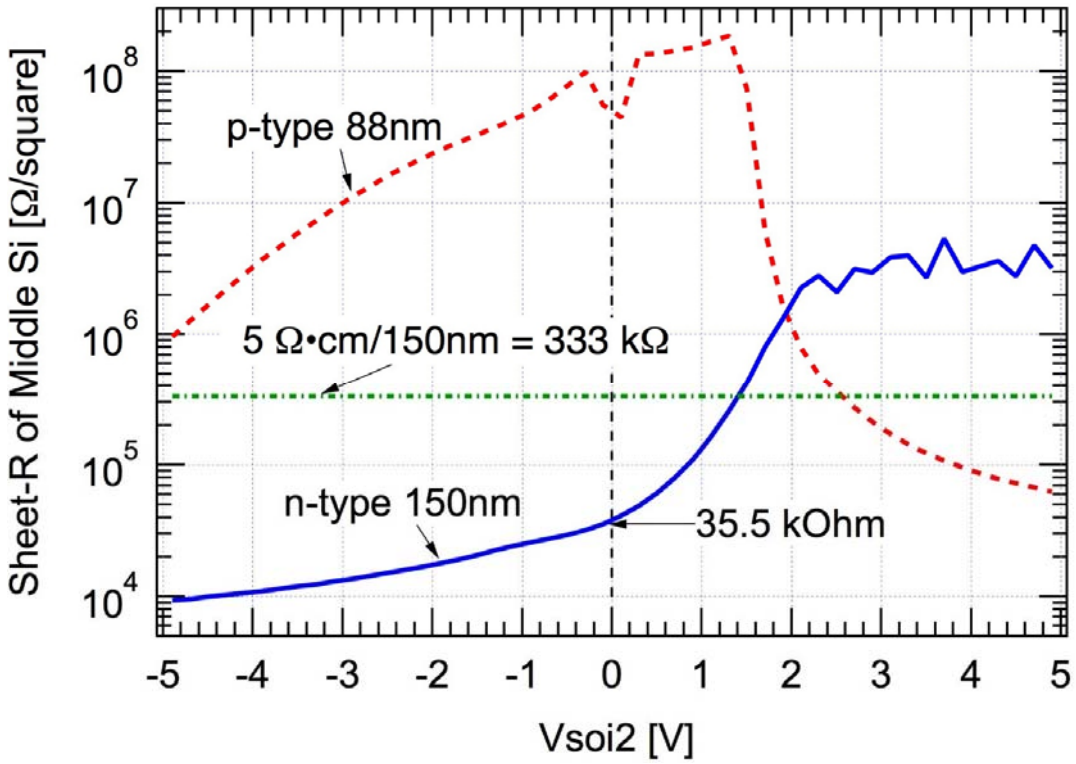


→ Miyoshi's Talk

- Middle Si layer shields coupling between sensor and circuit.
- It also compensate E-field generated by radiation trapped hole by applying negative voltage to the middle layer.
- Possible to shrink buried well size to reduce sensor capacitance.

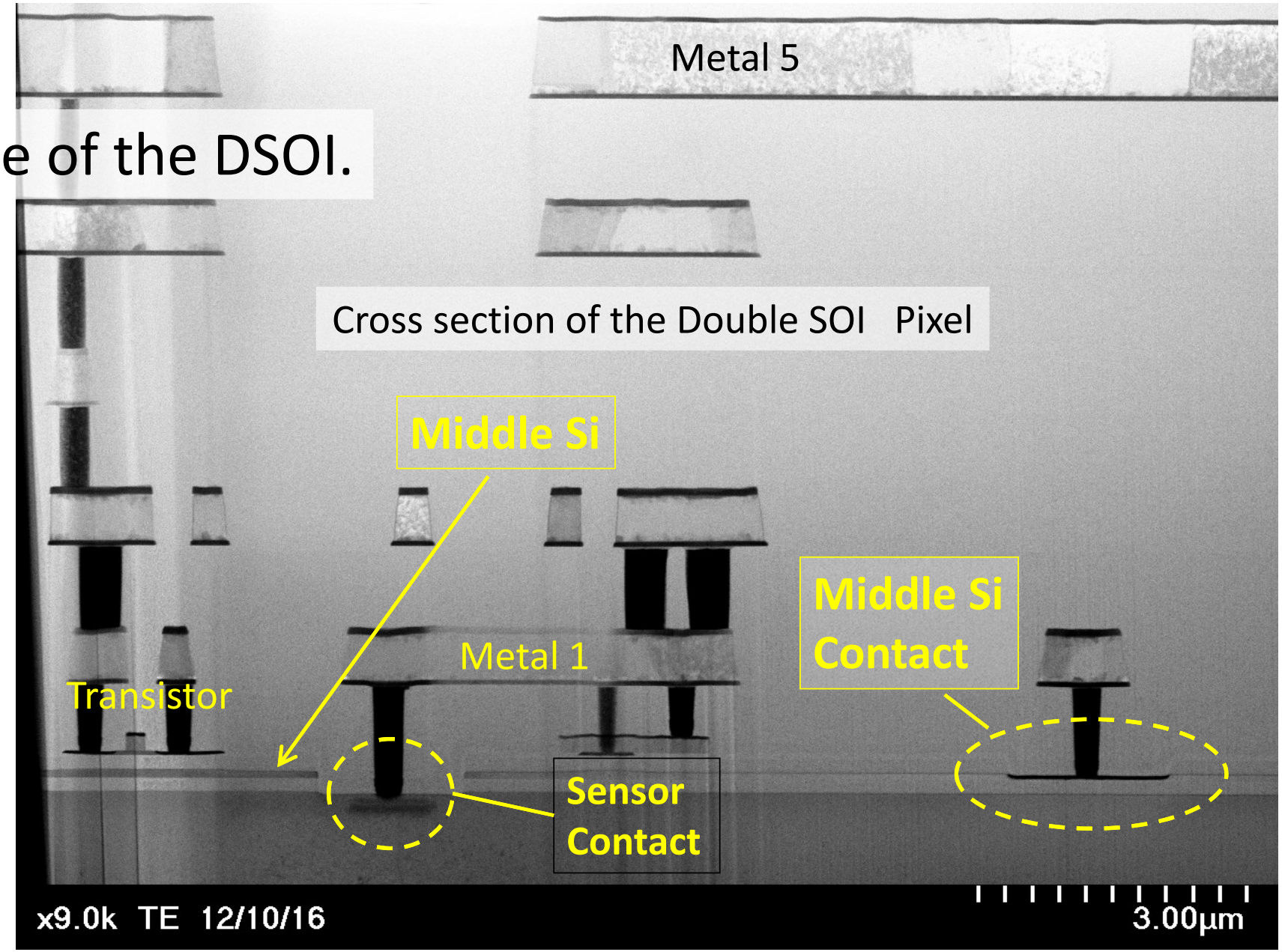
Specifications of the Double SOI wafers

	1st(SOITEC)	2nd(Shinetsu)
SOI1	p-type 88 nm, < 10 Ω •cm	p-type 88 nm, < 10 Ω •cm
BOX1	145 nm	145 nm
SOI2	p-type 88 nm, < 10 Ω •cm	n-type 150 nm, 3-5 Ω •cm
BOX2	145 nm	145 nm
Substrate	n-type Cz, 725um, ~700 Ω •cm	p-type FZ, 725um, > 5.0 k Ω •cm



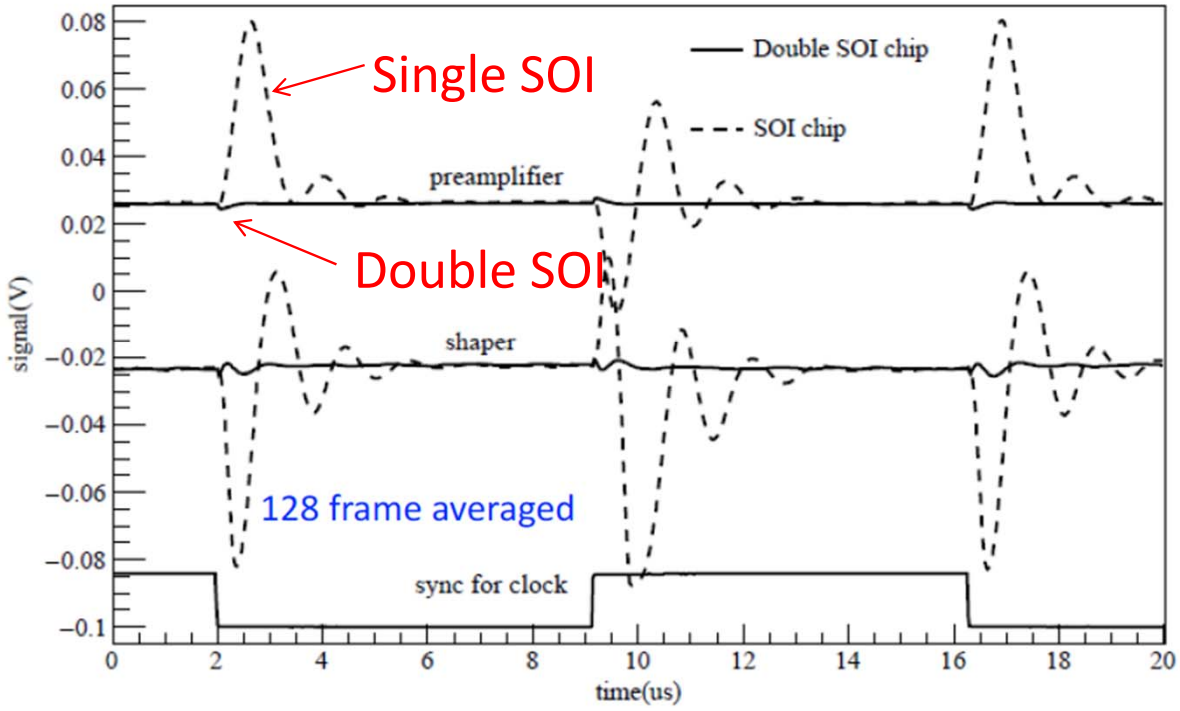
N-type middle Si layer has lower sheet resistance with negative SOI2 layer voltage, since P-type layer become depleted.

TEM image of the DSOI.



Cross Talk Reduction in Double SOI

Cross Talk from Clock line



Cross Talk between Circuit and Sensor is reduced to 1/20.

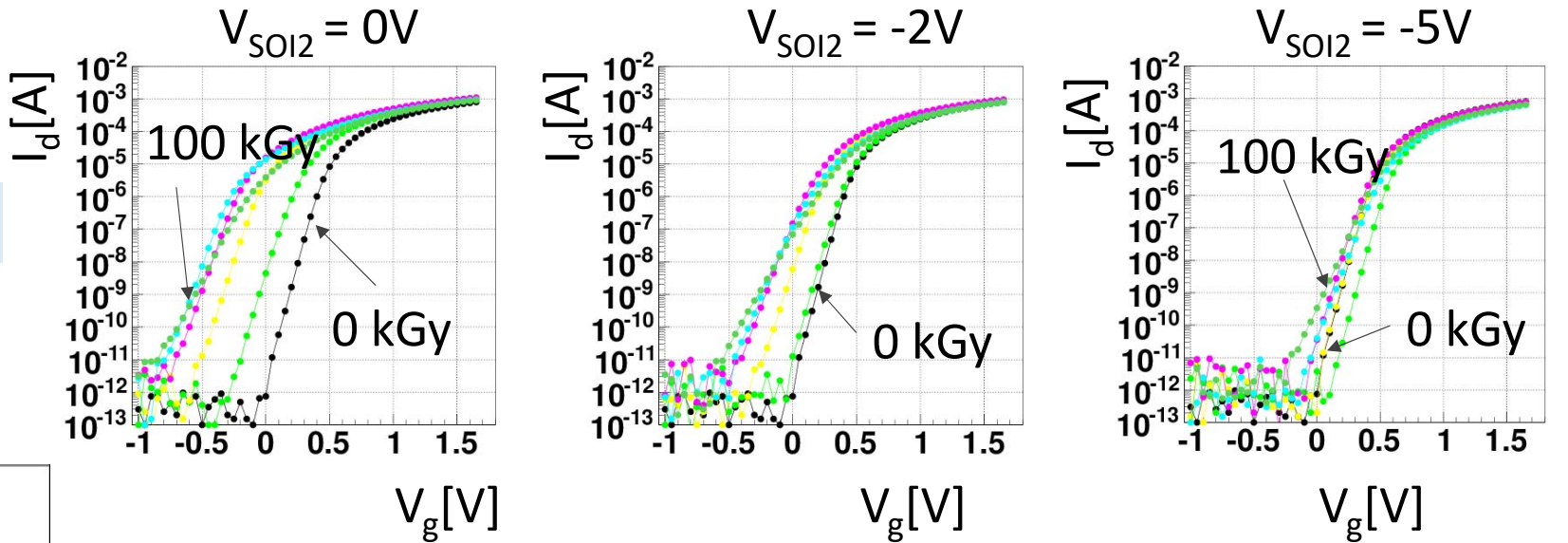
(Lu Yunpeng (IHEP))

Radiation Hardness Improvement in DSOI

(Id-Vg Characteristics v.s. SOI2 Potential)

I/O normal Vth
Source-Tie Tr.
L/W =0.35um/5um

NMOS



By setting Middle Si potential (Vsoi2）to -5V, Id-Vg curve returned nearly to pre-irradiation value at 100 kGy(Si) (10 Mrad).

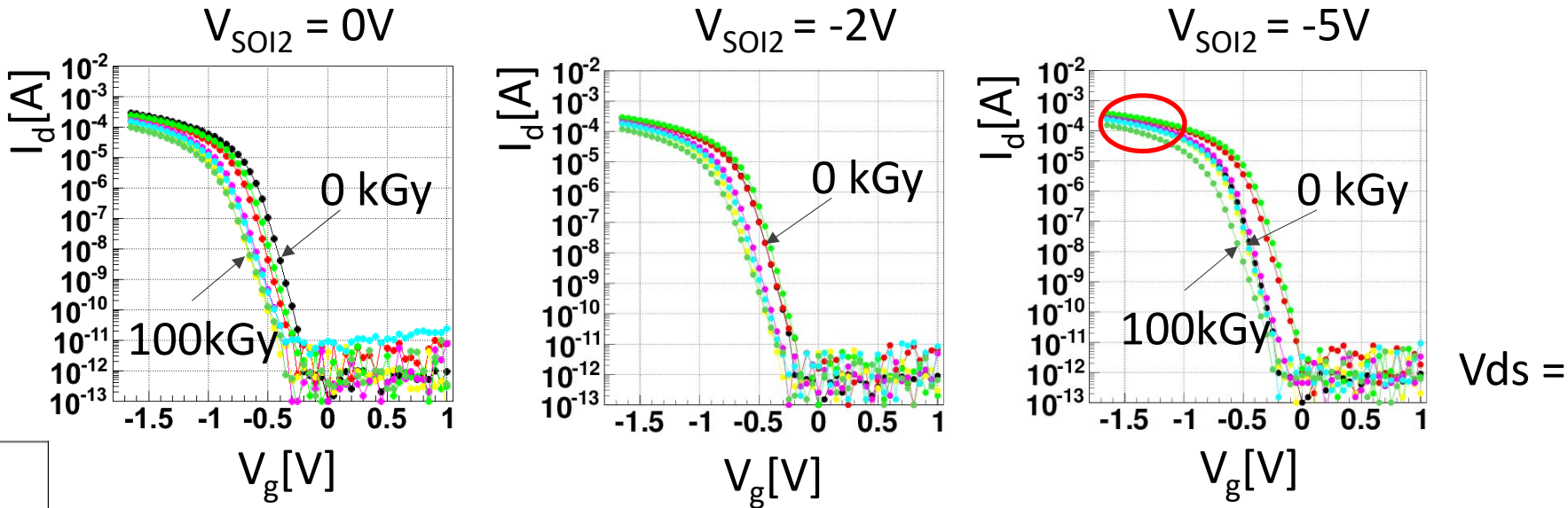
(U. of Tsukuba)

Radiation Hardness Improvement in DSOI

(Id-Vg Characteristics v.s. SOI2 Potential)

I/O Normal Vt
Source-Tie
L/W =0.35um/5um

PMOS



Vds = -1.8V

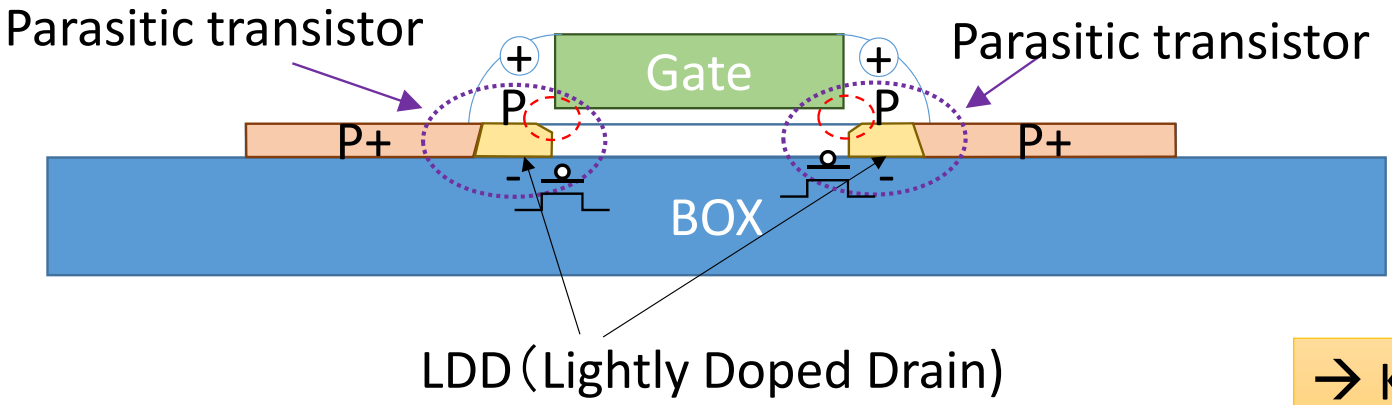
0kGy
0.5kGy
1kGy
2kGy
5kGy
10kGy
20kGy
100kGy

Threshold voltage shift is not so sensitive to radiation dose and the middle Si potential. However, Drain Current decreases by 80% at 100 kGy(Si).

(U. of Tsukuba)

Dose Increase in Lightly Doped Drain (LDD) Region

- Major cause of the drain current degradation in PMOS with radiation is Vth increase at gate edge due to positive charge generation in spacer.
- Charge in spacer control the Vth of the parasitic transistor.
- To reduce this effect, lightly doped drain (LDD) dose should be increased.
- Present process has rather low dose in LDD region to aiming lower power.



→ Kurachi's Talk

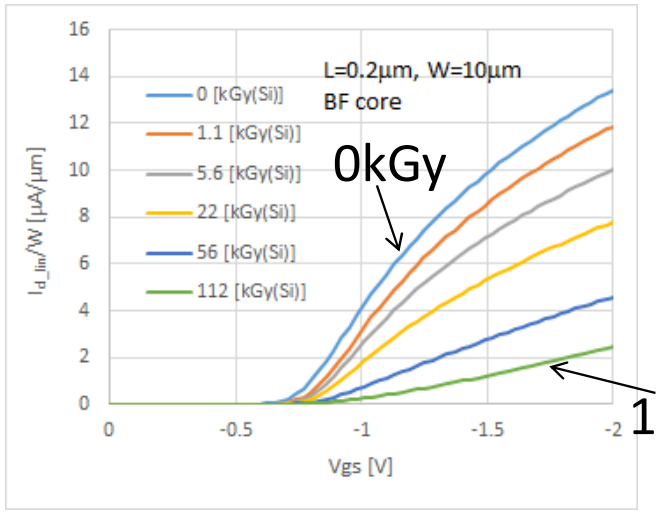
Recovery of the drain current reduction

PMOS

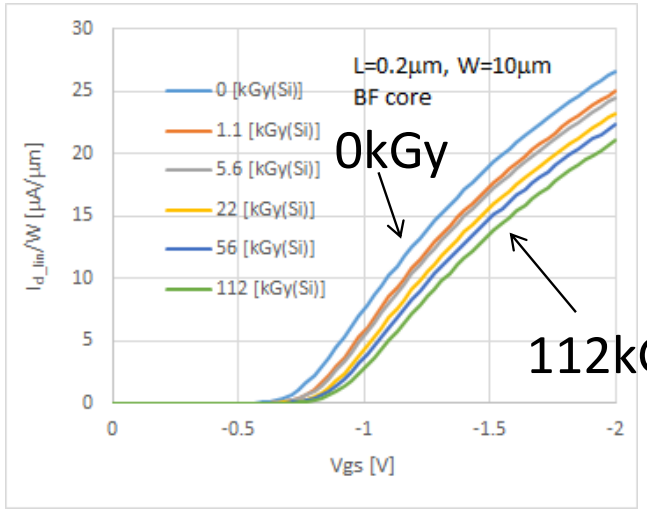
Vds=-0.1V

Linear Id

Previous Process



LDD Dose x 6



By increasing Implantation dose of PLDD region 6 times higher than present value, the degradation is reduced from 80% to 20% at 112 kGy(Si).

Ref.) I. Kurachi, et al. "Analysis of Effective Gate Length Modulation by X-Ray Irradiation for Fully Depleted SOI p-MOSFETs, IEEE Trans. on Elec. Dev. Vol. 62, Aug. 2015, pp. 2371-2376.

3rd refinement: Pinned Depleted Diode (SOIPIX-PDD)

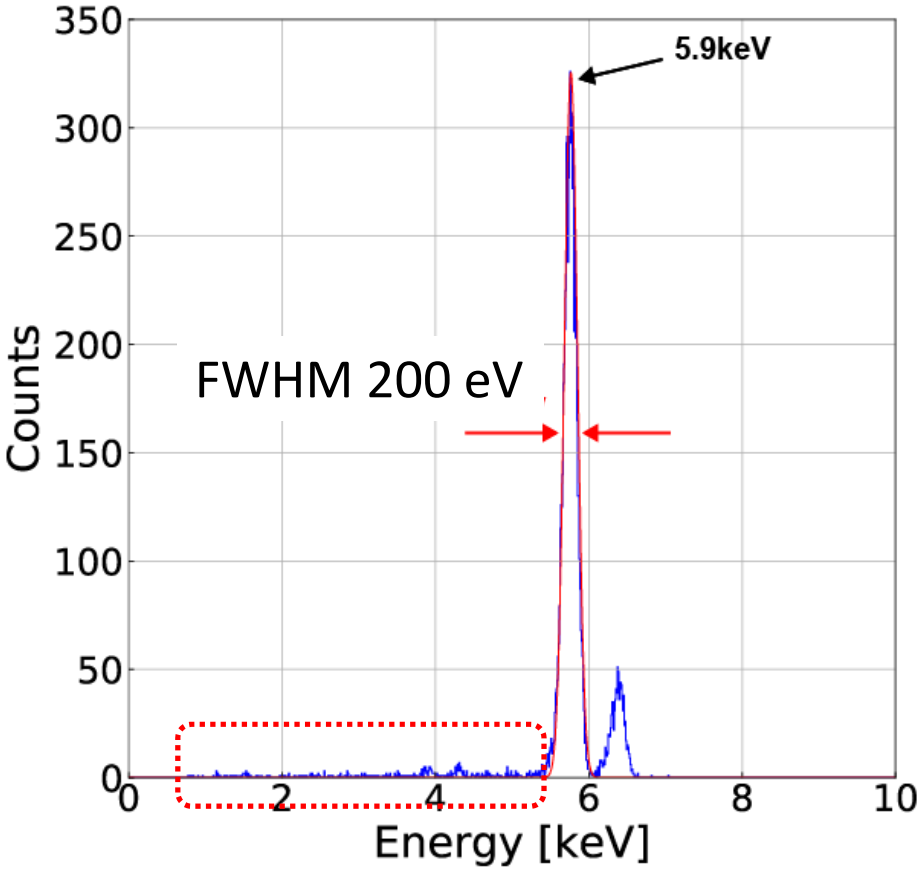
There are relatively large surface leakage current.

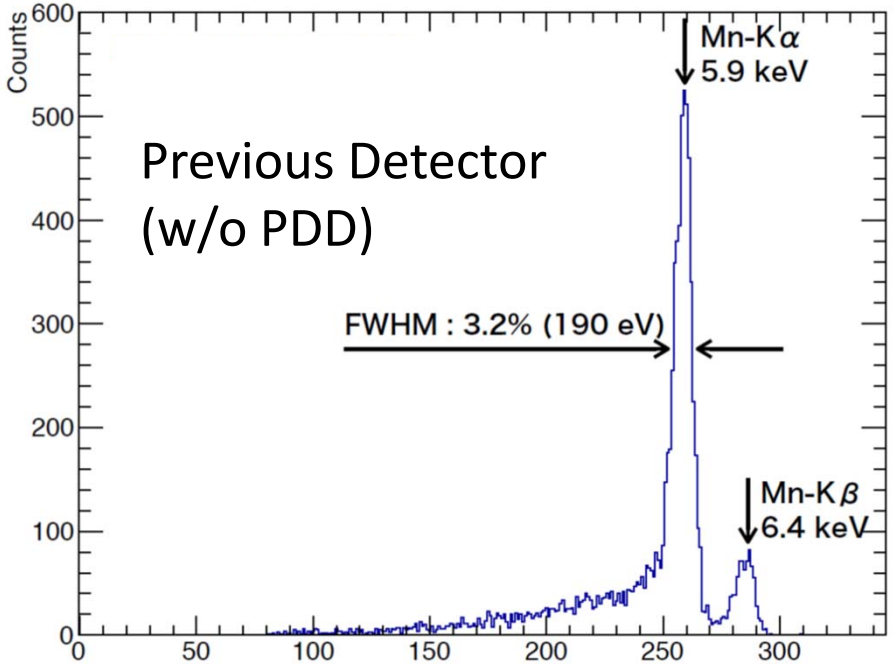
Leakage current between BOX and Substrate is pinned with BPW while avoiding punch throw with deep BNW layer.

→ See Kawahito's Talk

(H. Kamehama et al., 'A Low-Noise X-ray Astronomical SOI Pixel Detector Using a Pinned Depleted Diode Structure, to be published in Sensors.)

Energy Resolution:
X-ray Spectrum of ^{55}Fe using the SOIPIX-PDD





Gain = 70 μV/e-
Noise = 11.0 e-
Dark Current = 56 pA/cm2 @-35˚C

Very good Resolution (low noise) and no tail in the peak (showing perfect charge collection efficiency).

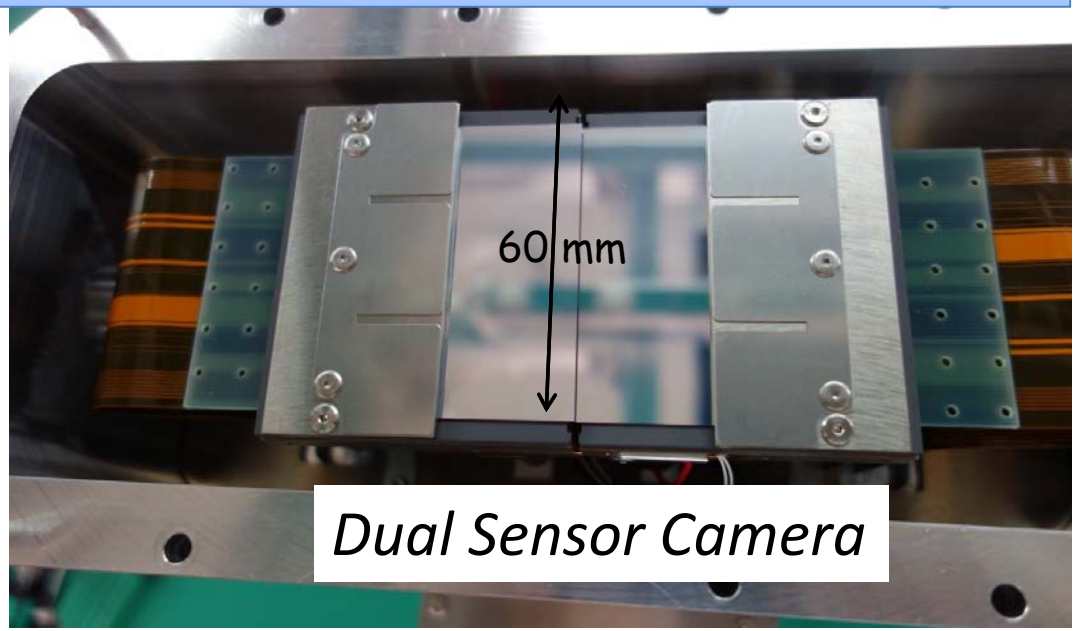
(Shizuoka & Kyoto Univ.)

SOI Photon-Imaging Array Sensor (*SOPHIAS)*

for X-ray Free Electron Laser (XFEL) SACLA

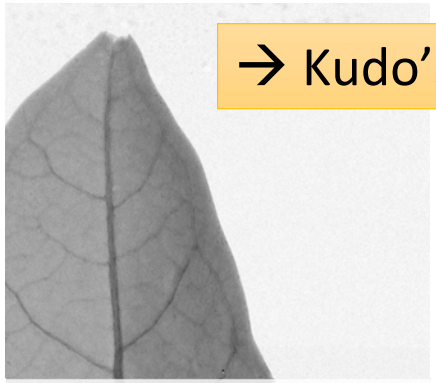
Utilization of SOPHIAS has been started for various experiments in SACLA@RIKEN.

- Dynamics of Atomic Structure
- Direct Observation of Chemical Reactions
- etc.

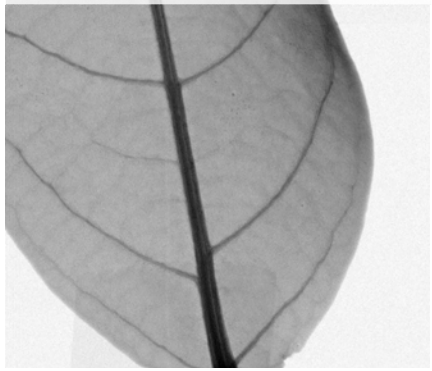


Dual Sensor Camera

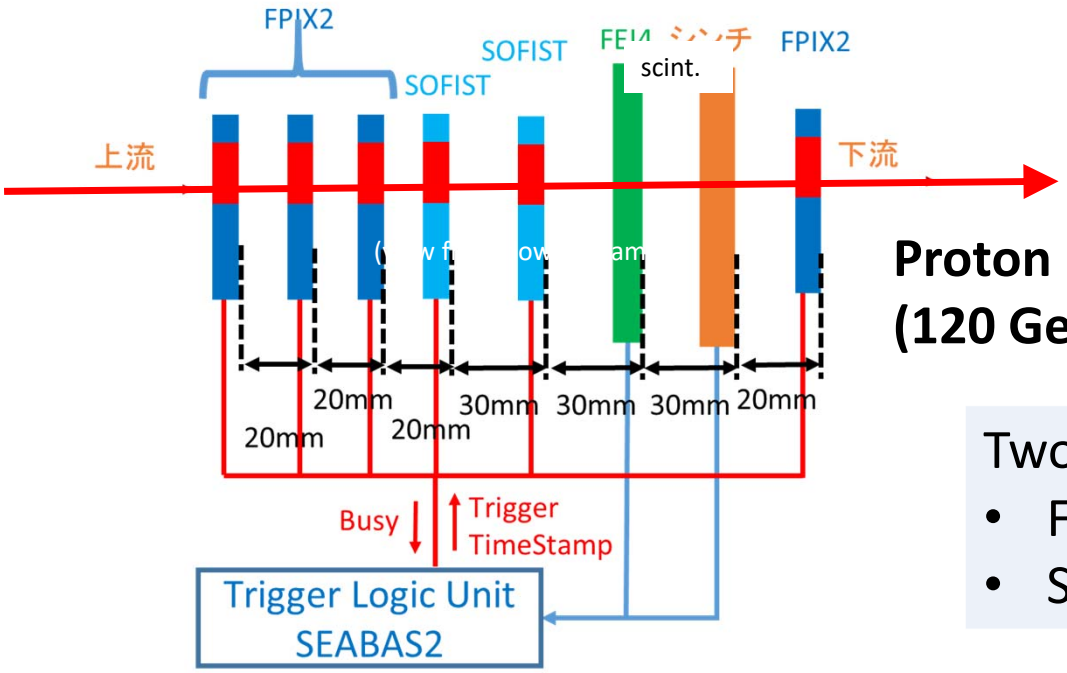
→ Kudo's Talk

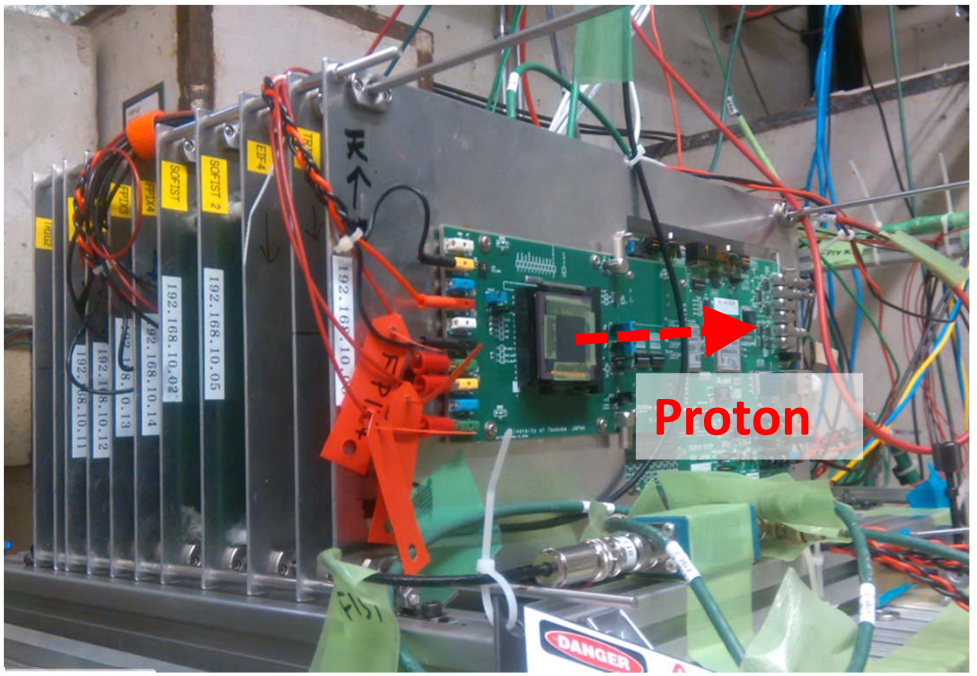


X-ray Tube Cu 22kV 400uA
5000 frames accumulated
(total exposure: 500 s)
Sensor-detector:2m



Tracking Resolution: High-Energy Beam test @Fermi National Accelerator Lab.



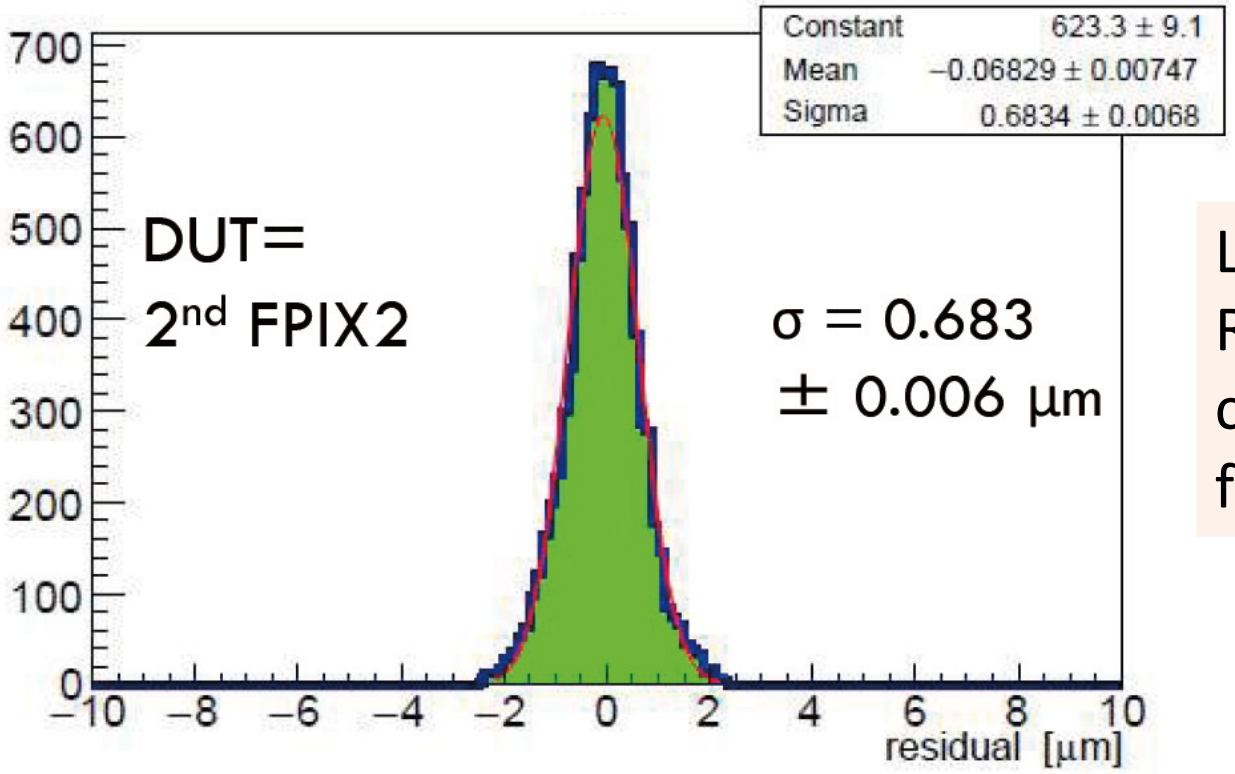


Proton Beam (120 GeV/c)

Two kinds of SOIPIX-DSOI detectors are used:

- FPIX2 x 4: 8 μm square pixel detector
- SOFIST1 x 2: 20 μm square pixel detector

Tracking Resolution (cont.)



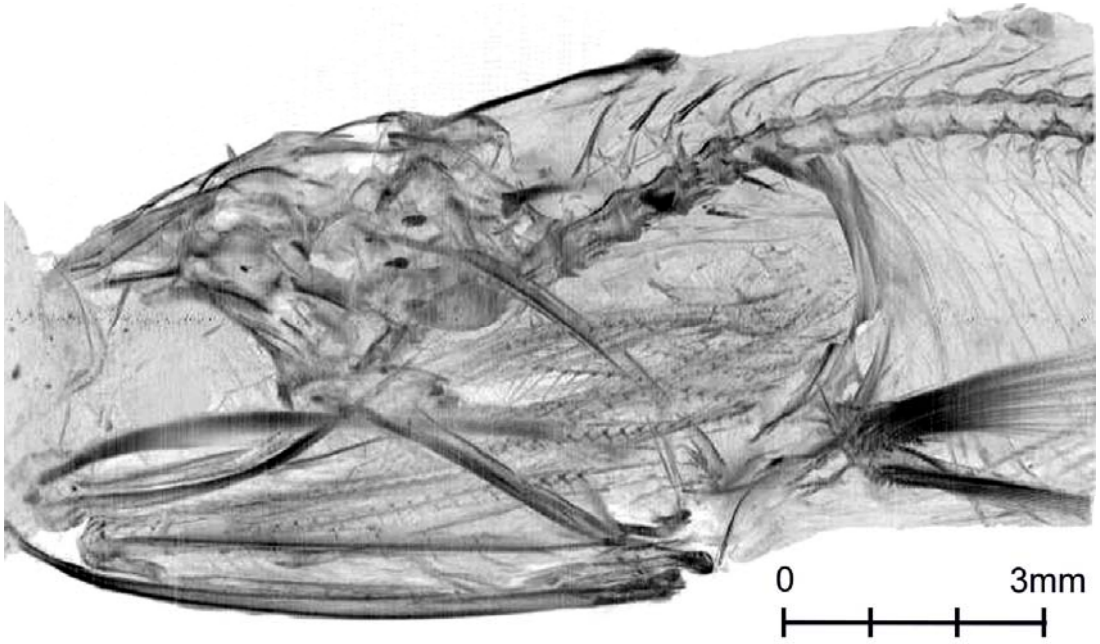
Less than 1 μm Position Resolution for high-energy charged particle is achieved first in the world .

(K. Hara et al., Development of Silicon-on-Insulator Pixel Detectors, Proceedings of Science, to be published)

Summary

- Three main refine techniques are developed in the SOIPIX process.
- Buried Well is very effective to shield high-voltage for sensor region.
- Double SOI technology is excellent in shielding and radiation hardness improvement.
- With Pinned Depleted Diode (PDD) structure, Leakage current is reduced to less than 60 pA/cm^2, and very good charge collection efficiency and low noise is obtained.
- Large SOPHIAS detectors are being used in many Synch. Rad. Exp.
- Tracking resolution of 0.7 μm is achieved with 8 μm SOI pixel.
- Many kinds of SOI radiation detectors are being developed for various scientific applications.

Thank you for your kind attention!



3D CT
R. Nishimura