CMOS technologies and power distribution components for HL-LHC: radiation strikes back

F. Faccio
CERN - EP/ESE
Episode IV: A New Hope

<table>
<thead>
<tr>
<th>time</th>
<th>1998 .................... 2005</th>
</tr>
</thead>
<tbody>
<tr>
<td>TID target</td>
<td>10Mrad .................. 50Mrad</td>
</tr>
</tbody>
</table>
The accumulation of TID-induced ‘defects’ in an oxide decreases with the thickness of the oxide. Leakage currents can be eliminated by design (Hardness By Design, HBD).

Defects in the STI oxide can open conductive paths between n+ diffusions

HBD techniques systematically used in 0.25um

250nm used in 1998-2006 and now in LHC
Radiation effect

Total Ionising Dose
This is the ‘classical’ problem for CMOS technologies

Displacement Damage
Only relevant for circuits using diodes or parasitic bipolar devices in CMOS

Single Event Effects
Traceable to the interaction of a single particle
Can lead to temporary or permanent failure

Common wisdom in 2000-2005

Easily tamed
250nm: use HBD and dedicated digital library

Not an issue in CMOS

SEU, SET: mitigation techniques required (most common: TMR)
SEL: not an issue in 0.25um with HBD (guardrings)
Episode V:
Radiation Strikes Back
Leakage current “peak” in 130nm ICs

Variability in radiation response (novel 130nm process)

Large degradation in 65nm transistors (short and narrow channel effects)

True Dose-Rate effect in CMOS

SEL in almost production-ready ICs (novel 130nm process)
The properties of the defects (hole traps, interface states) in the 130nm process have been studied in these two publications:


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- F.Faccio	et	al.,	"Total	onizing
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- F.Faccio,	G.Cervelli,	"Radia7on-induced
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effects
tn deep
submicron	CMOS	transistors",	IEEE	Trans.	Nucl.	Science,	Vol.52,	No.6,	December

The leakage current is the sum of different mechanisms involving:

- the creation/trapping of charge (by radiation)
- its passivation/de-trapping (by thermal excitation)

These phenomena are Dose Rate and Temperature dependent, so it is not easy to forecast the real leakage in the application (environmental dependency)!

The last point refers to full annealing at 100°C, and finding the shift with TID. Nevertheless, we have not addressed their detailed nature in our study.

For narrow channel transistors, this effect is known in CMOS technologies as the “narrow channel effect”, and it is observable in any deep submicron transistor. This effect is known in CMOS technologies as 

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Large logic 130nm circuits in cold environments might show a significant increase of power consumption due to leakage currents.

Current consumption in the ATLAS IBL in the experiment during data acquisition.
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NMOS transistors from different FABs (same manufacturer) show a very different radiation response, in particular for the source-drain leakage current.

Talk at the 2017 TWEPP that can be found under the header “Stability of the TID response of the 65 and 130nm technologies” in the CERN Foundry Services web page:

https://espace.cern.ch/asics-support/docs/_layouts/15/start.aspx#/SitePages/Conferences.aspx

if you do not have access, email a request to foundry.services@cern.ch
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Leakage current does not appear in 65nm NMOS transistors consistently in all samples measured so far!

 Radiation damage is severe in short and narrow channel transistors, where it depends on the bias and temperature applied both during and after irradiation

 Radiation-Induced Narrow Channel Effect (RINCE)

 Radiation-Induced Short Channel Effect (RISCE)
**RINCE** is studied on transistors with very long channel (10\(\mu\)m). It is particularly detrimental for PMOS transistors, and it presents little recovery with post-exposure annealing (defects seem to be stable).

![Graph showing irradiation and annealing effects on nMOS and pMOS transistors.](image)

- **Irradiation**
  - nMOS
  - pMOS
- **Marginal evolution**
- **Large degradation**
- **Annealing**
  - nMOS
  - pMOS
- **Slow evolution / slight recover.**
**RINCE** is traceable to radiation-induced defects in the STI oxide

Charge trapped in the oxide (faster)

Charge trapped at the interface, negative for nMOS, positive for pMOS (slower)

Electric field

Radiation induced narrow channel effects (RINCE).
**RISCE** is studied on Enclosed Layout Transistors (ELTs).
Short-channel ELTs are subject to two distinct effects:

1. **Decrease of on-current during exposure**

2. **Threshold voltage shift**
   During or after irradiation depending on transistor polarity, temperature, applied bias

![Graphs showing on-current decrease and threshold voltage shift](image)

This is particularly relevant for PMOS transistors!
Both effects originate in the LDD spacers
The buildup of charge in defects located in the spacer oxide influences the amount of carriers in the LDD extensions, affecting the parasitic series resistance.

Ionization in the spacers frees hydrogen (protons, neutral and/or molecular hydrogen). This can later transport and reach into the gate oxide where it can de-passivate Si-H bonds. Coming from the source/drain spacers, it will give origin to defects concentrated close to these regions.
Standard qualification procedures for CMOS foresee a 1-week annealing period post-irradiation at 100°C. This considerably worsens the performance of PMOS transistors.

Is this needed AND is this representative of the real degradation?

Transistors’ size: W=0.6um, L=60nm
Irradiation conditions:
* Bias:
  “Diode” => |Vgs|=|Vds|=1.2V
We have extracted the activation energy extracted of 0.92 eV for the process. We can hence estimate the post-irradiation evolution of the transistors’s current at different temperature.

The evolution is considerably slower below 0°C.

No need to take the Vth shift of PMOS into account IF circuits are forbidden to be biased at high temperature (cut power supply if T>0°C?)
For those wishing to know more...


Talk of G.Borghello (CERN) at the 2017 TWEPP that can be found under the header “Total Ionising Dose response of 65nm MOSFETs irradiated to ultra-high doses” in the CERN Foundry Services web page: https://espace.cern.ch/asics-support/docs/_layouts/15/start.aspx#/SitePages/Conferences.aspx
if you do not have access, email a request to foundry.services@cern.ch
Measurements on samples from other two 65nm manufacturers showed comparable or even worse damage.
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SEL in almost production-ready ICs (novel 130nm process)
Measurements on identical samples in the 65nm technology at different facilities (X-rays and $^{60}$Co) show a consistent trend to larger damage at lower dose rate.

Qualitatively similar results are observed in samples from our “novel” 130nm technology.

This dose rate dependency of the damage has to be studied:
- bias and temperature dependence
- physical origin (STI? Spacers?)
- influence of the transistor’s size

The effect should then be included in our qualification procedure!
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Single Event Latchup was observed in full ASICs designed in the “novel” 130nm technology:

**Velopix (LHCb)**
SEL observed during heavy ion tests in Louvain-la-Neuve, then confirmed and localised with pulsed laser tests in Montpellier

**SAMPA (ALICE)**
SEL observed during 180MeV protons irradiation
For Velopix, a map of the sensitive points was produced scanning a part of the logic with a pulsed laser beam.

Map produced by the pulsed laser test

The map was compared to the one produced by a software script run on the layout and producing a colour-coded map of the distance to the nearest substrate/well contact (dark blue = small distance; red = large distance).

Map produced by the software script

**SEL sensitive regions correspond to those with the largest distance!**
The High Density logic in Velopix has been modified in Velopix2. As shown in the software-produced map for this new version, the distance from the NWELL and Substrate contacts has been decreased systematically to a maximum of 10um.

Velopix2 has been irradiated with heavy ions and no SEL has been detected!

Talk at the 2017 TWEPP that can be found under the header “Single Event Latchup in 130nm circuits” in the CERN Foundry Services web page:
https://espace.cern.ch/asics-support/docs/_layouts/15/start.aspx#/SitePages/Conferences.aspx
if you do not have access, email a request to foundry.services@cern.ch
Do not blindly trust “common sense”!

Radiation effects are complex and often surprising...
Radiation and magnetic field tolerant DCDC converters

- High voltage & radiation tolerance
- Air core inductors
- Large current switching
- Reliability requirements
- EMI requirements
- Sensitivity to displacement damage
- Packaging (cooling, large currents)
Within CERN-ESE, we develop radiation and magnetic field tolerant components for a flexible power distribution system

Example implementation

1st stage buck converter

2.5 (small load)

2nd stage buck converter

0.8 (digital)

2nd stage buck converter

1.2 (analog)

Linear regulator

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### Common specifications

<table>
<thead>
<tr>
<th>Main electrical parameters</th>
<th>FEAST2.1</th>
<th>bPOL12V</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage*</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output voltage</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output current*</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Max output power*</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Programmable switching frequency*</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Inductor value*</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Protection features</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Over-current protection peak level</td>
<td>~6 A</td>
<td></td>
</tr>
<tr>
<td>Over-temperature protection threshold</td>
<td>~100°C</td>
<td></td>
</tr>
<tr>
<td>Under-voltage lockout threshold</td>
<td>~4.5 V</td>
<td></td>
</tr>
<tr>
<td>Soft-Start duration</td>
<td>~470 us</td>
<td></td>
</tr>
<tr>
<td>Control features</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Enable (input) threshold</td>
<td>~815 mV</td>
<td></td>
</tr>
<tr>
<td>Power Good flag (output)</td>
<td>Open Drain</td>
<td></td>
</tr>
<tr>
<td>Radiation tolerance</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Total Ionizing Dose</td>
<td>&gt; 300 Mrad</td>
<td></td>
</tr>
<tr>
<td>Displacement Damage tolerance</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(1MeV eq. neutron flux)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Development status</td>
<td>Production (&gt;60,000 already</td>
<td>Final Prototype</td>
</tr>
<tr>
<td></td>
<td>distributed)</td>
<td></td>
</tr>
<tr>
<td>Availability</td>
<td>Packaged chip (QFN32)</td>
<td>Packaged chip (QFN32)</td>
</tr>
<tr>
<td></td>
<td>2 DCDC modules</td>
<td></td>
</tr>
</tbody>
</table>

* Safe operating conditions are application-dependent
**bPOL2V5** is the prototype 2nd stage buck converter, developed in 130nm CMOS

(reference: G.Ripamonti’s talk at TWEPP2017 “A 2.5V Step-Down DC-DC converter for Two-Stages Power Distribution Systems”)

### Target specifications

<table>
<thead>
<tr>
<th>Spec</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage</td>
<td>2.0V ÷ 2.7V</td>
</tr>
<tr>
<td>Output voltage</td>
<td>0.6V ÷ 1.5V</td>
</tr>
<tr>
<td>Output current</td>
<td>≲ 3A (optimized @ 2A)</td>
</tr>
<tr>
<td>Switching frequency</td>
<td>&gt; 4MHz</td>
</tr>
<tr>
<td>Inductor value</td>
<td>&lt; 150nH</td>
</tr>
<tr>
<td>External components</td>
<td>Only C&lt;sub&gt;in&lt;/sub&gt;, C&lt;sub&gt;out&lt;/sub&gt;, L</td>
</tr>
<tr>
<td>Assembly</td>
<td>C4 Bump-bonding</td>
</tr>
<tr>
<td>Radiation Tolerance</td>
<td></td>
</tr>
<tr>
<td>Total Ionising Dose</td>
<td>&gt; 300 Mrad</td>
</tr>
<tr>
<td>Displacement Damage</td>
<td>&gt; 4 × 10&lt;sup&gt;15&lt;/sup&gt; n/cm&lt;sup&gt;2&lt;/sup&gt;</td>
</tr>
<tr>
<td>SEEs: absence of destructive events and of output power interruptions</td>
<td>&gt; 40 MeVcm&lt;sup&gt;2&lt;/sup&gt;mg&lt;sup&gt;-1&lt;/sup&gt;</td>
</tr>
</tbody>
</table>

A second prototype will be characterised in January (assembly is very time consuming). An alternative resonant architecture is explored, allowing to lower the inductance value to 10nH
linPOL12V is the prototype 2-channels linear regulator working with an input voltage of up to 12V (custom development for ATLAS ITK, but could be made available for other groups)

**Target specifications**

<table>
<thead>
<tr>
<th>Feature</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage</td>
<td>5V ÷ 12V</td>
</tr>
<tr>
<td>Output voltage</td>
<td>0.6V ÷ 5V (1.4V and 3.3V without the addition of external resistors)</td>
</tr>
<tr>
<td>Output current</td>
<td>≲ 80mA</td>
</tr>
<tr>
<td>External Components</td>
<td>C\textsubscript{in}, C\textsubscript{out}, R\textsubscript{out}, R\textsubscript{select}</td>
</tr>
<tr>
<td>Package</td>
<td>DFN8 (2x2mm)</td>
</tr>
</tbody>
</table>

**Radiation Tolerance**

<table>
<thead>
<tr>
<th>Feature</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Total Ionising Dose</td>
<td>&gt; 300 Mrad</td>
</tr>
<tr>
<td>Displacement</td>
<td>&gt; 2 × 10^{15} n/cm\textsuperscript{2}</td>
</tr>
<tr>
<td>SEE: absence of destructive events and of output power interruptions</td>
<td>&gt; 40 MeVcm\textsuperscript{2}mg\textsuperscript{-1}</td>
</tr>
</tbody>
</table>

A first prototype will be characterised in late spring 2018 (but the design is extracted from bPOL12V, already measured in silicon)
A family of components for power distribution systems is being developed at CERN.

These components are meant to help power distribution in HEP experiments where radiation and magnetic field tolerance are required.