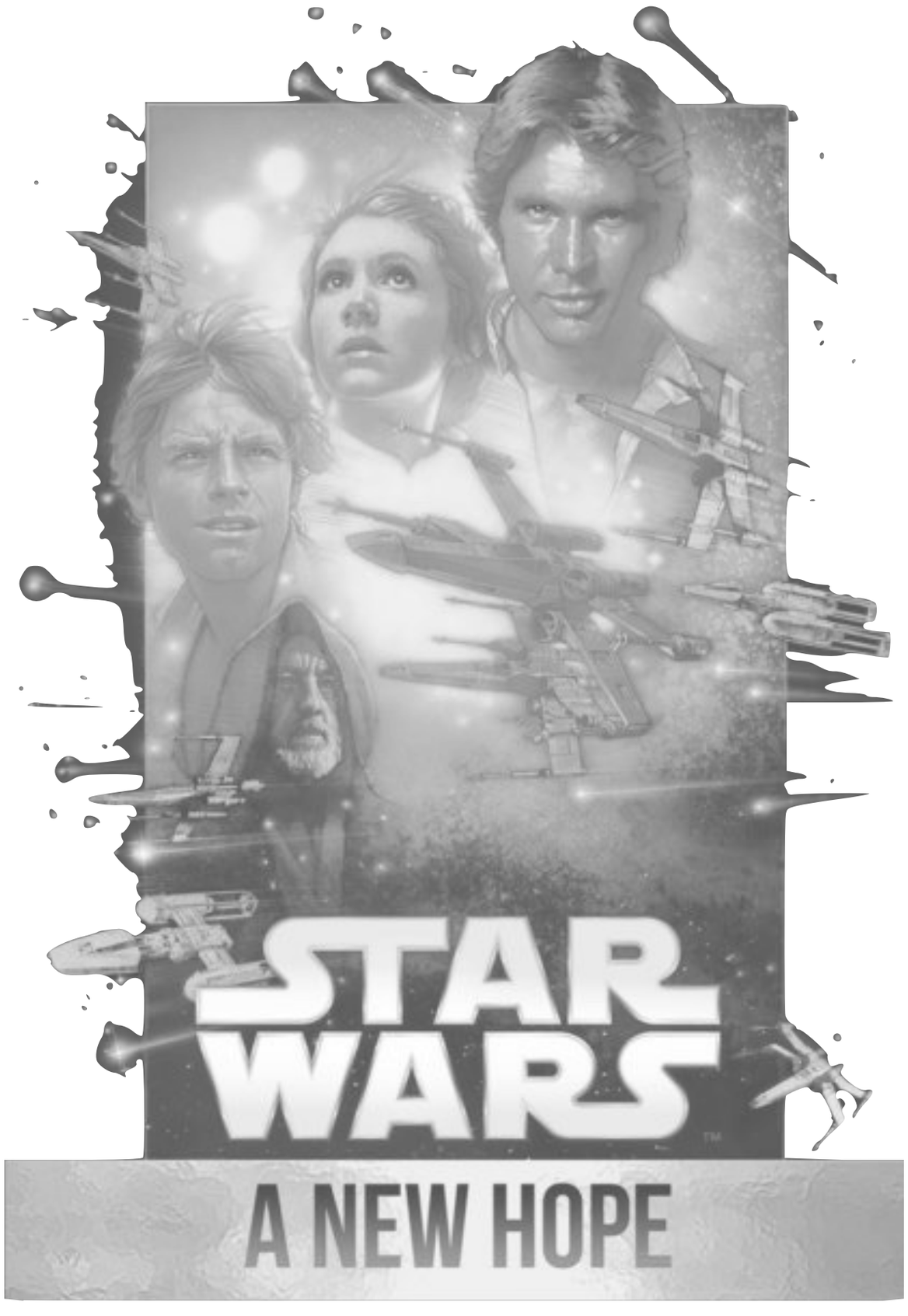
CMOS technologies and power distribution components for HL-LHC: radiation strikes back

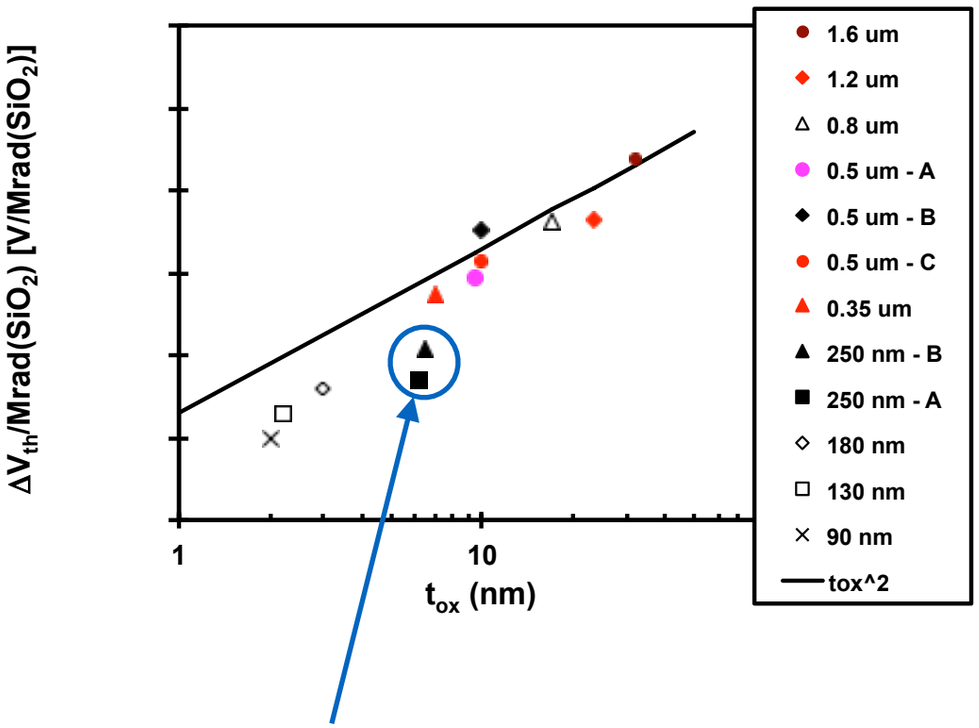
F.Faccio
CERN - EP/ESE



Episode IV:
A New Hope

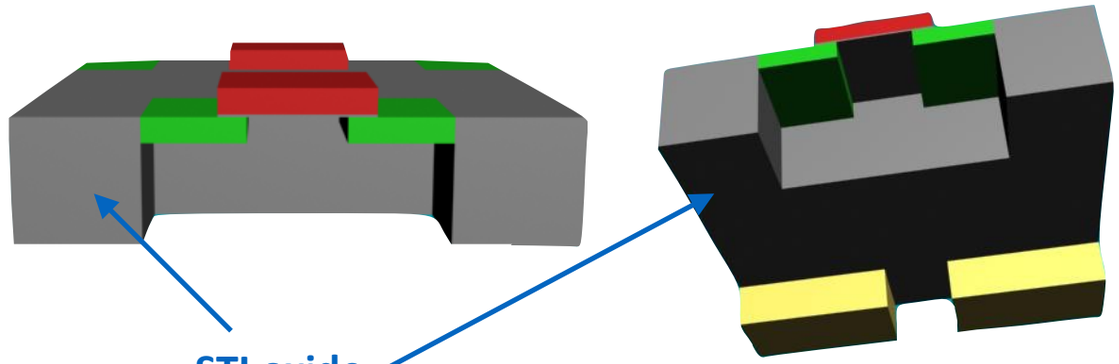
time	**1998……2005**
TID target	**10Mrad……50Mrad**

The accumulation of TID-induced ‘defects’ in an oxide decreases with the thickness of the oxide.
Leakage currents can be eliminated by design (Hardness By Design, HBD).

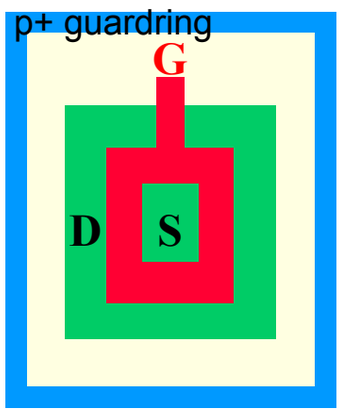


250nm used in 1998-2006 and now in LHC

Defects in the STI oxide can open conductive paths between n+ diffusions

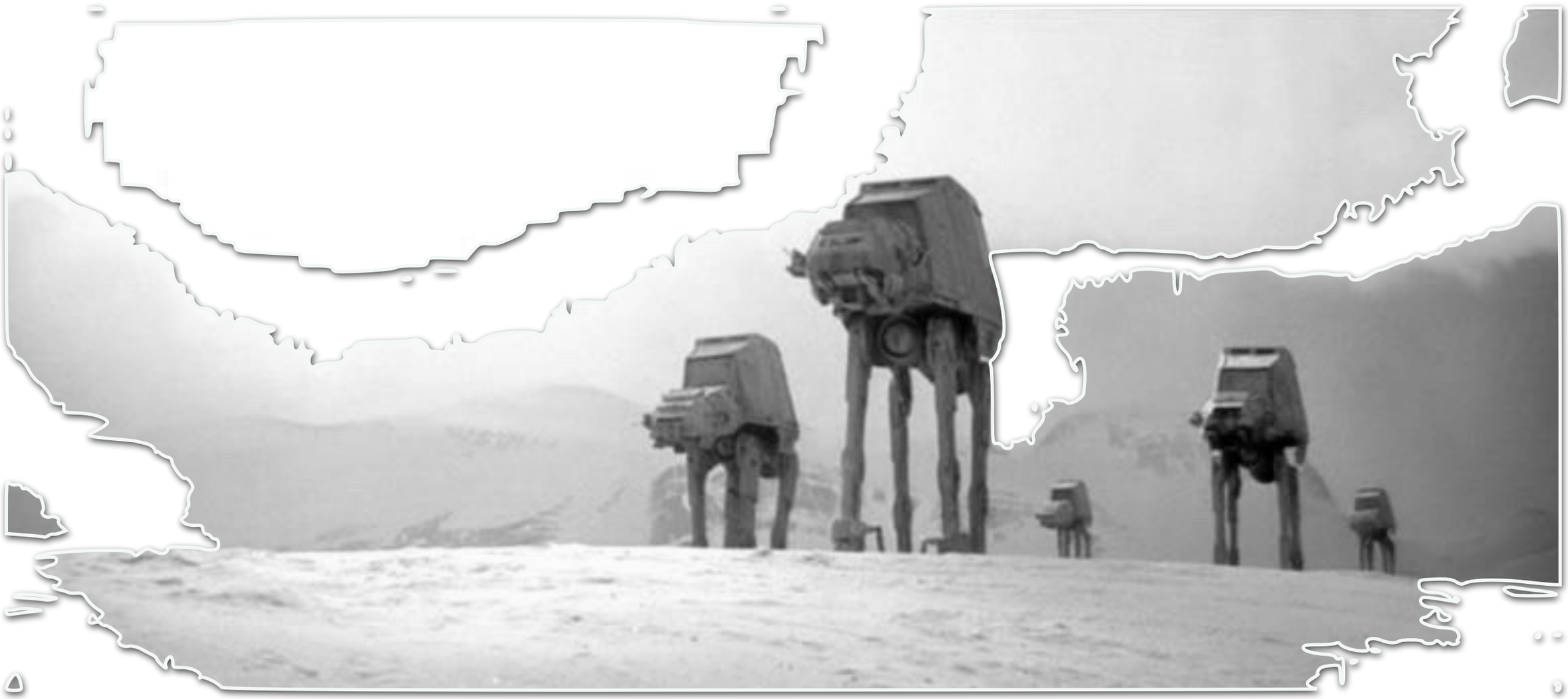


HBD techniques systematically used in 0.25um

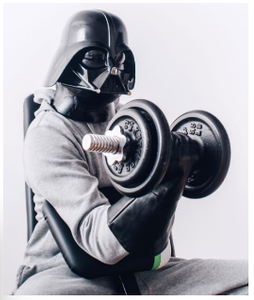


Radiation effect	Common wisdom in 2000-2005
Total Ionising Dose This is the ‘classical’ problem for CMOS technologies	**Easily tamed** **250nm: use HBD and dedicated digital library**
Displacement Damage Only relevant for circuits using diodes or parasitic bipolar devices in CMOS	**Not an issue in CMOS**
Single Event Effects Traceable to the interaction of a single particle Can lead to temporary or permanent failure	**SEU, SET: mitigation techniques required (most common: TMR)** **SEL: not an issue in 0.25um with HBD (guardrings)**

Episode V:
Radiation Strikes Back



Leakage current “peak” in 130nm ICs



Variability in radiation response (novel 130nm process)

Large degradation in 65nm transistors (short and narrow channel effects)

True Dose-Rate effect in CMOS

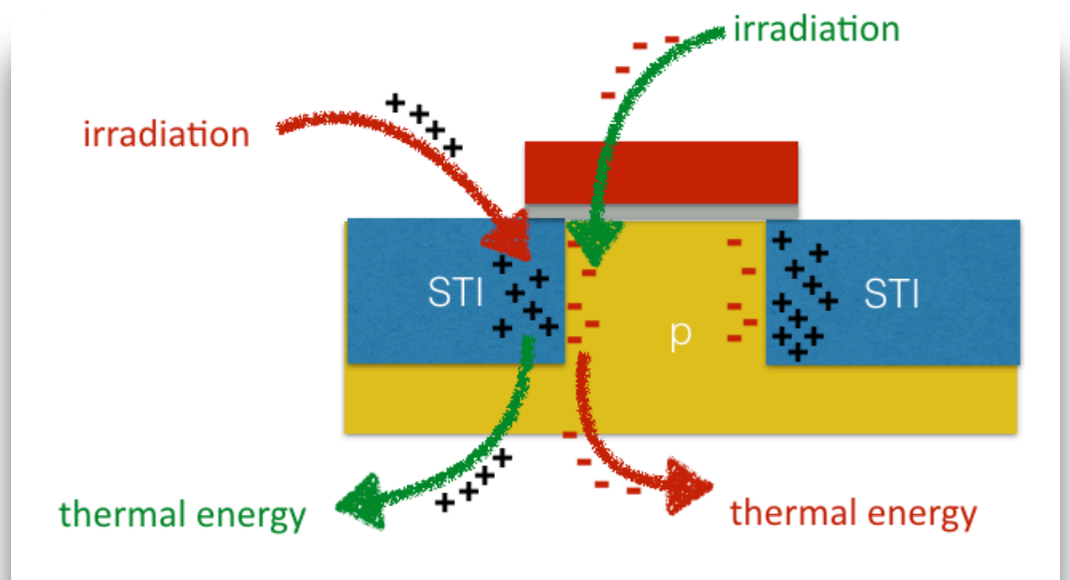
SEL in almost production-ready ICs (novel 130nm process)

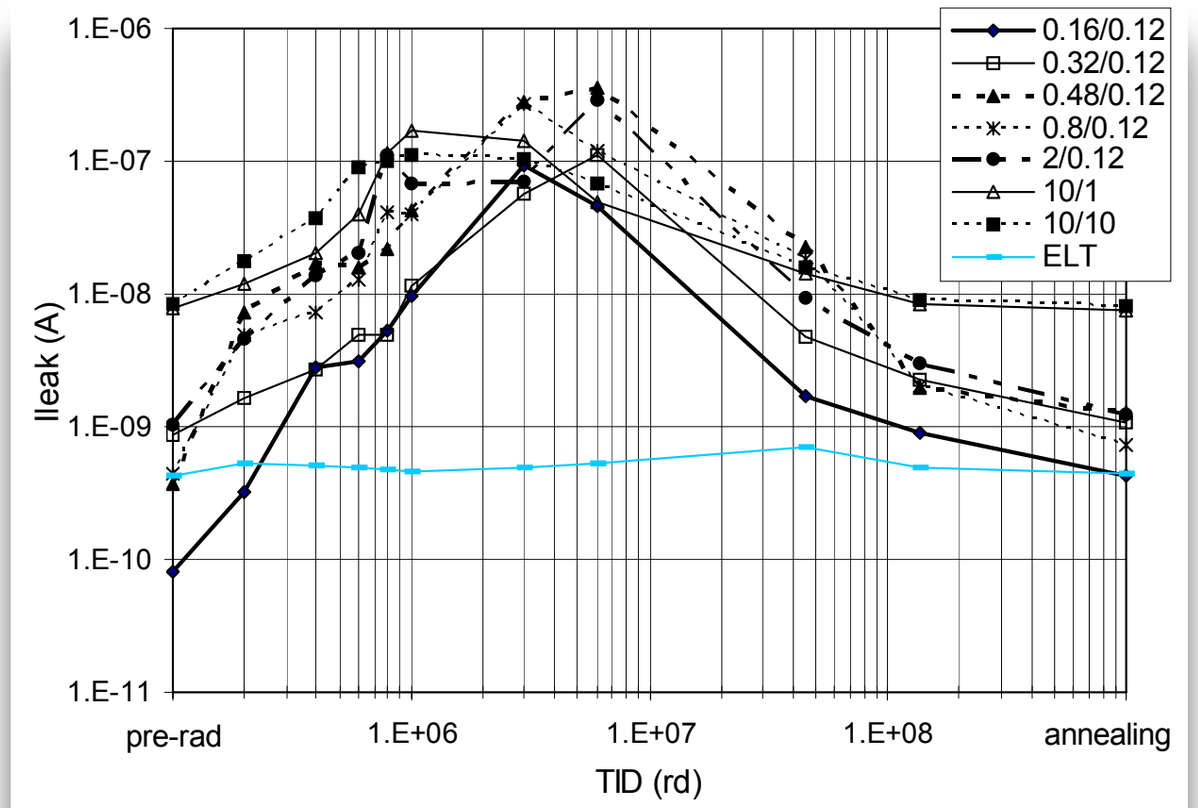
In the 130nm technology selected around 2005, we took the decision NOT to develop a dedicated HBD digital library.

The leakage current is the sum of different mechanisms involving:

- **the creation/trapping of charge (by radiation)**
- **its passivation/de-trapping (by thermal excitation)**

These phenomena are Dose Rate and Temperature dependent, so it is not easy to forecast the real leakage in the application (environmental dependency)!



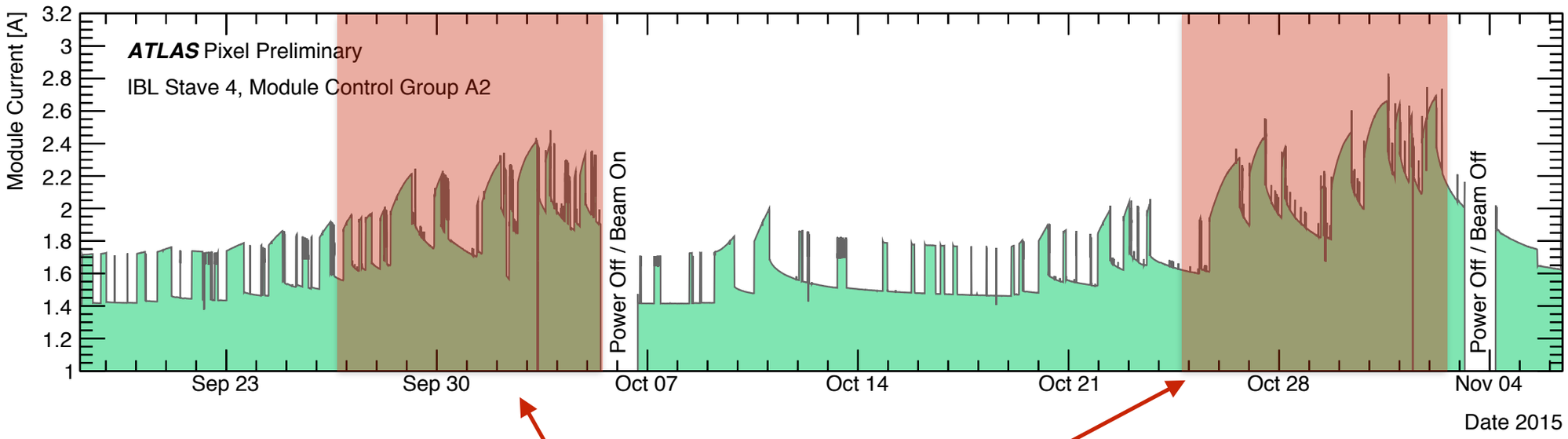


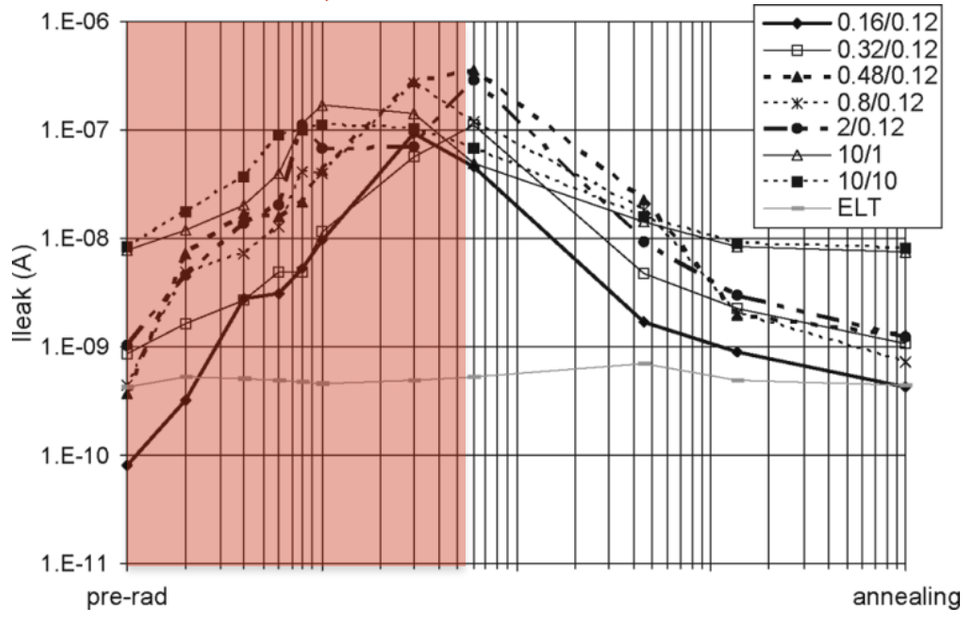
The properties of the defects (hole traps, interface states) in the 130nm process have been studied in these two publications:

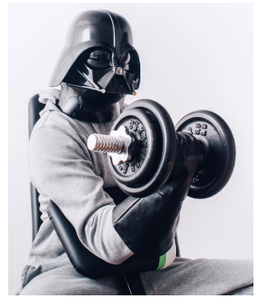
- F.Faccio, G.Cervelli, "Radiation-induced edge effects in deep submicron CMOS transistors", IEEE Trans. Nucl. Science, Vol.52, No.6, December 2005, pp.2413-2420
- F.Faccio et al., "Total ionizing dose effects in shallow trench isolation oxides", Microelectronics Reliability 48 (2008) 1000-1007

Large logic 130nm circuits in cold environments might show a significant increase of power consumption due to leakage currents

Current consumption in the ATLAS IBL in the experiment during data acquisition







Leakage current “peak” in 130nm ICs

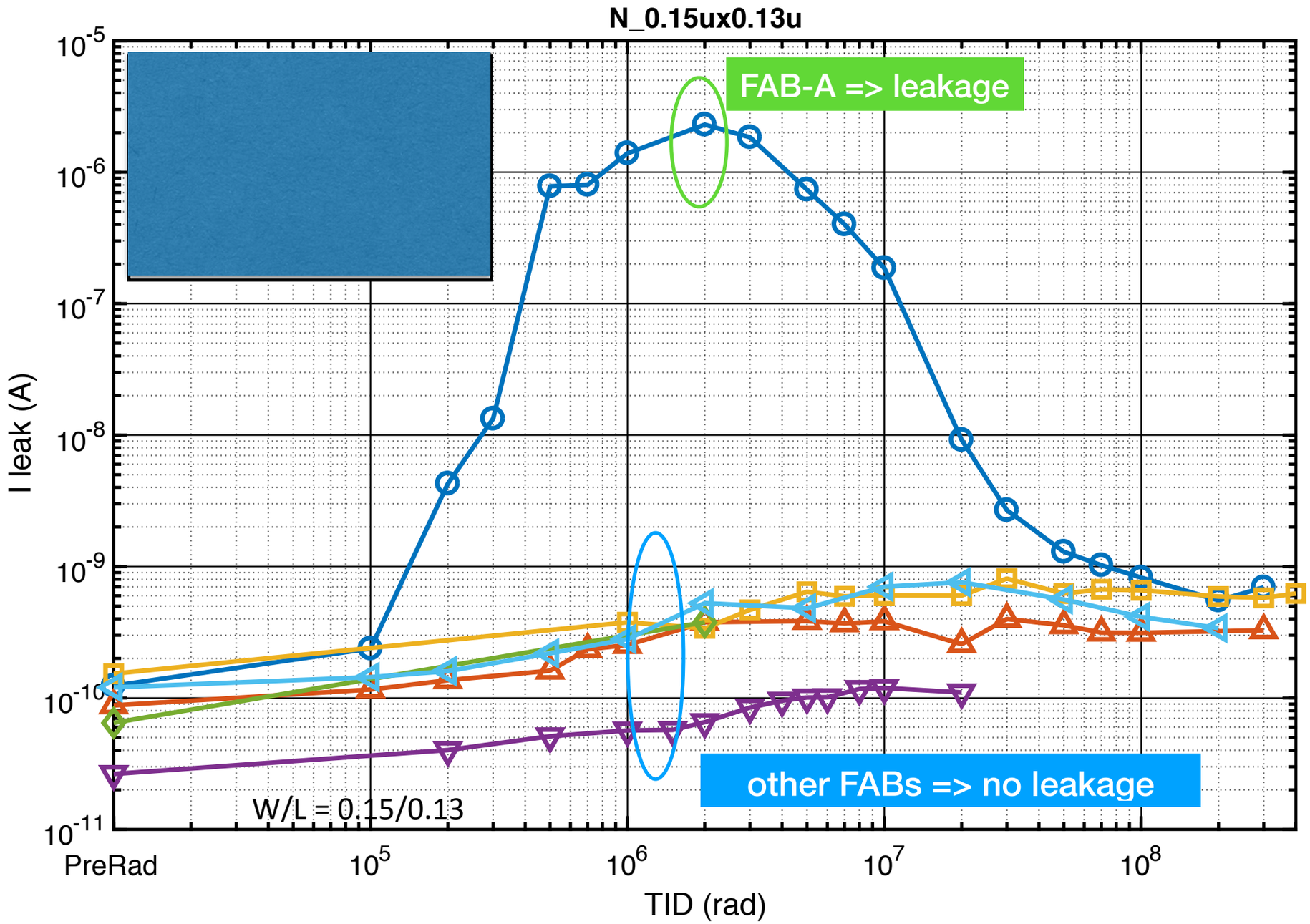
Variability in radiation response (novel 130nm process)

Large degradation in 65nm transistors (short and narrow channel effects)

True Dose-Rate effect in CMOS

SEL in almost production-ready ICs (novel 130nm process)

NMOS transistors from different FABs (same manufacturer) show a very different radiation response, in particular for the source-drain leakage current



Talk at the 2017 TWEPP that can be found under the header "Stability of the TID response of the 65 and 130nm technologies" in the CERN Foundry Services web page:

https://espace.cern.ch/asics-support/docs/_layouts/15/start.aspx#/SitePages/Conferences.aspx

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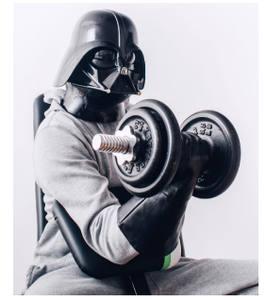

Leakage current “peak” in 130nm ICs

Variability in radiation response (novel 130nm process)

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True Dose-Rate effect in CMOS

SEL in almost production-ready ICs (novel 130nm process)

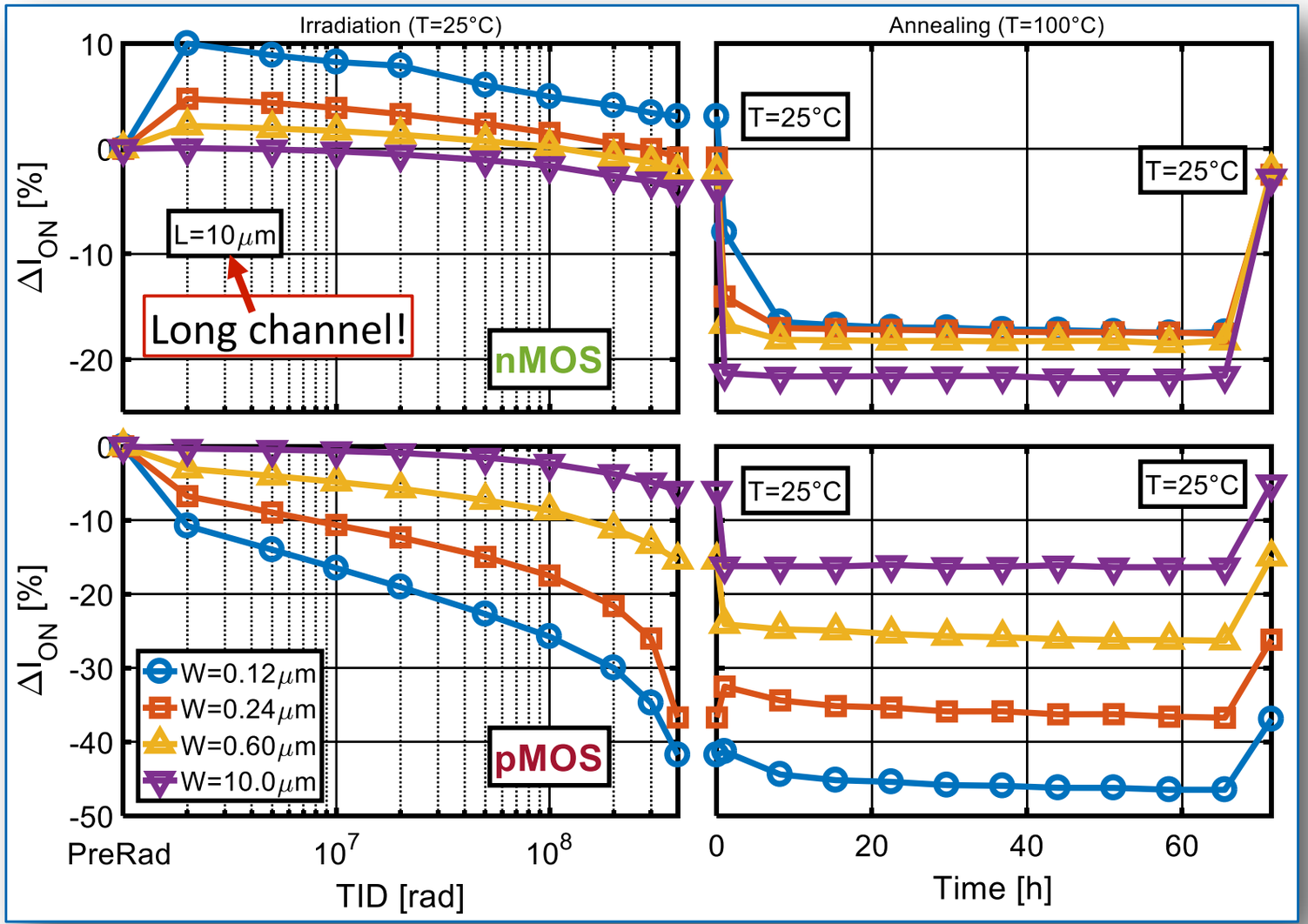
Leakage current does not appear in 65nm NMOS transistors consistently in all samples measured so far!

Radiation damage is severe in short and narrow channel transistors, where it depends on the bias and temperature applied both during and after irradiation

Radiation-Induced Narrow Channel Effect (RINCE)

Radiation-Induced Short Channel Effect (RISCE)

RINCE is studied on transistors with very long channel (10um).
It is particularly detrimental for PMOS transistors, and it presents little recovery with post-exposure annealing (defects seem to be stable)



Irradiation

nMOS

pMOS

Marginal evolution

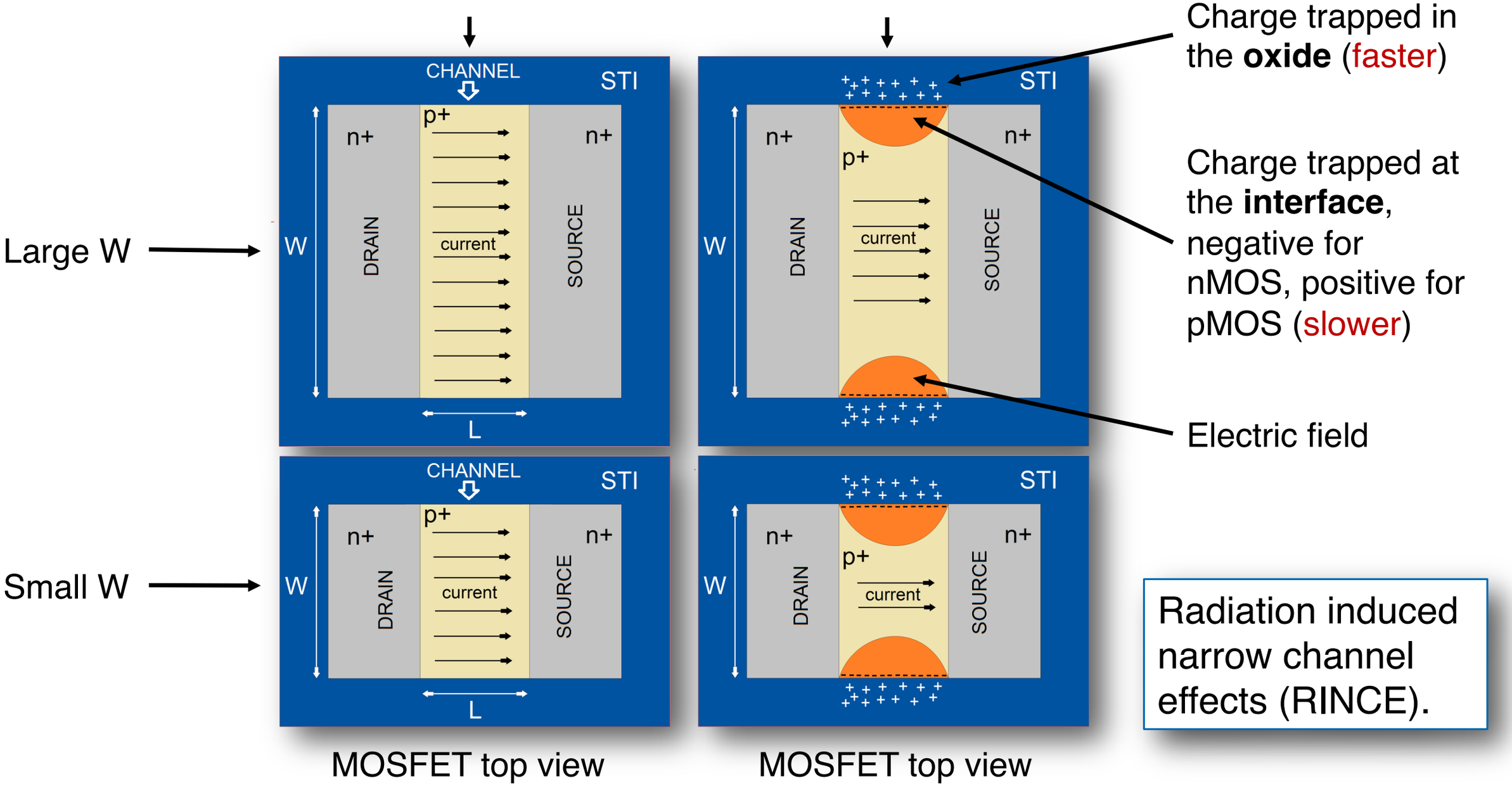
Large degradation

Annealing

nMOS
pMOS

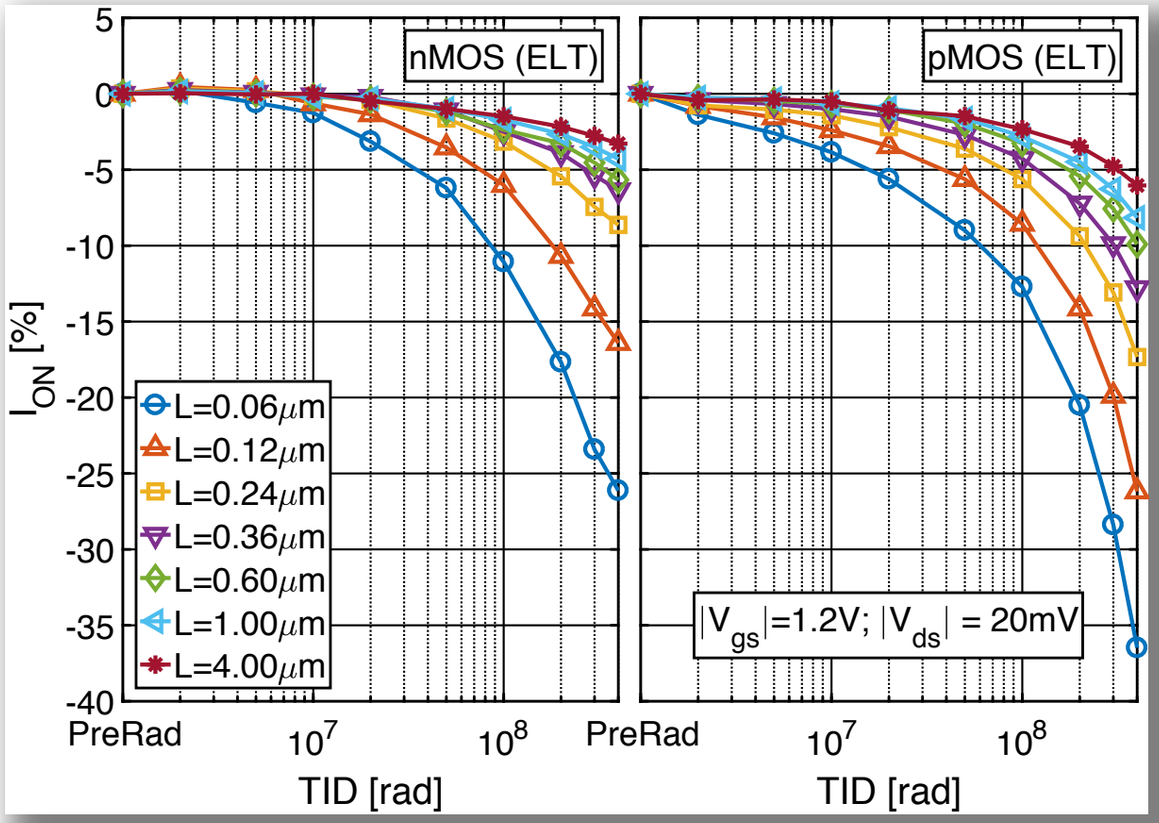
Slow evolution / slight recover.

RINCE is traceable to radiation-induced defects in the STI oxide



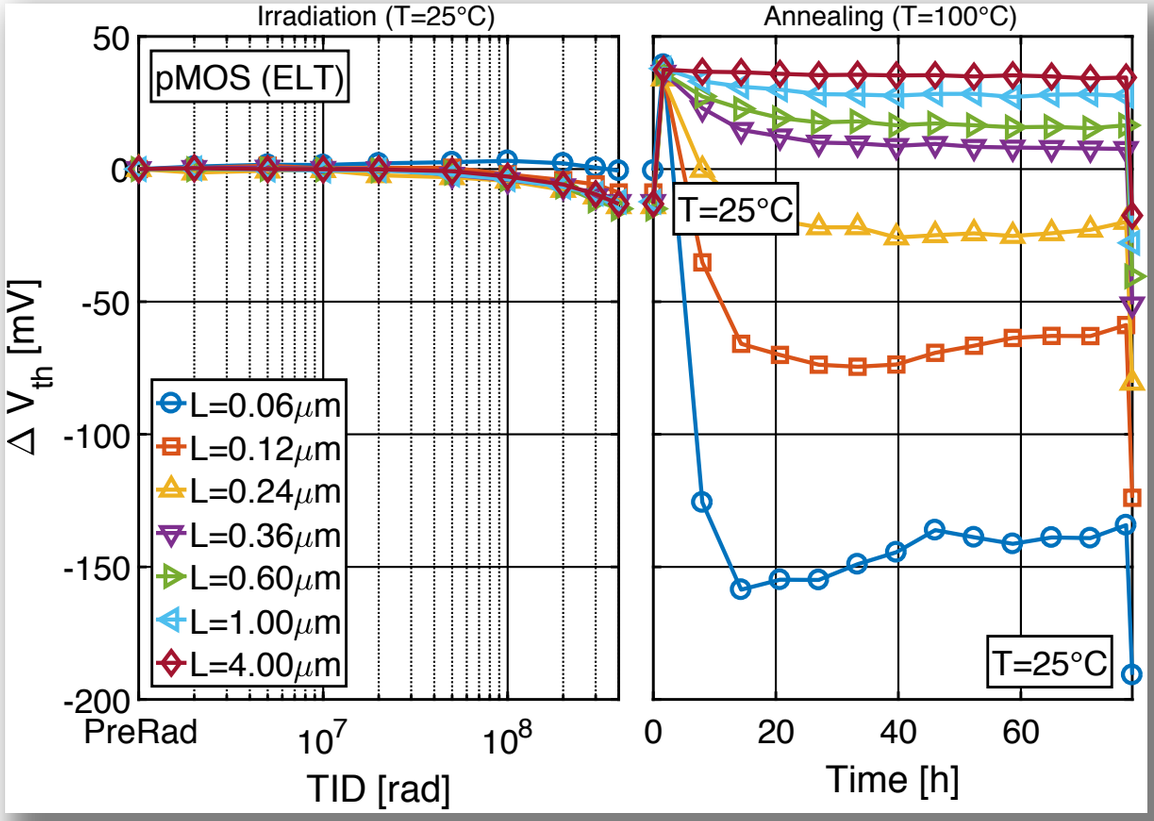
RISCE is studied on Enclosed Layout Transistors (ELTs).
Short-channel ELTs are subject to two distinct effects:

1. Decrease of on-current during exposure



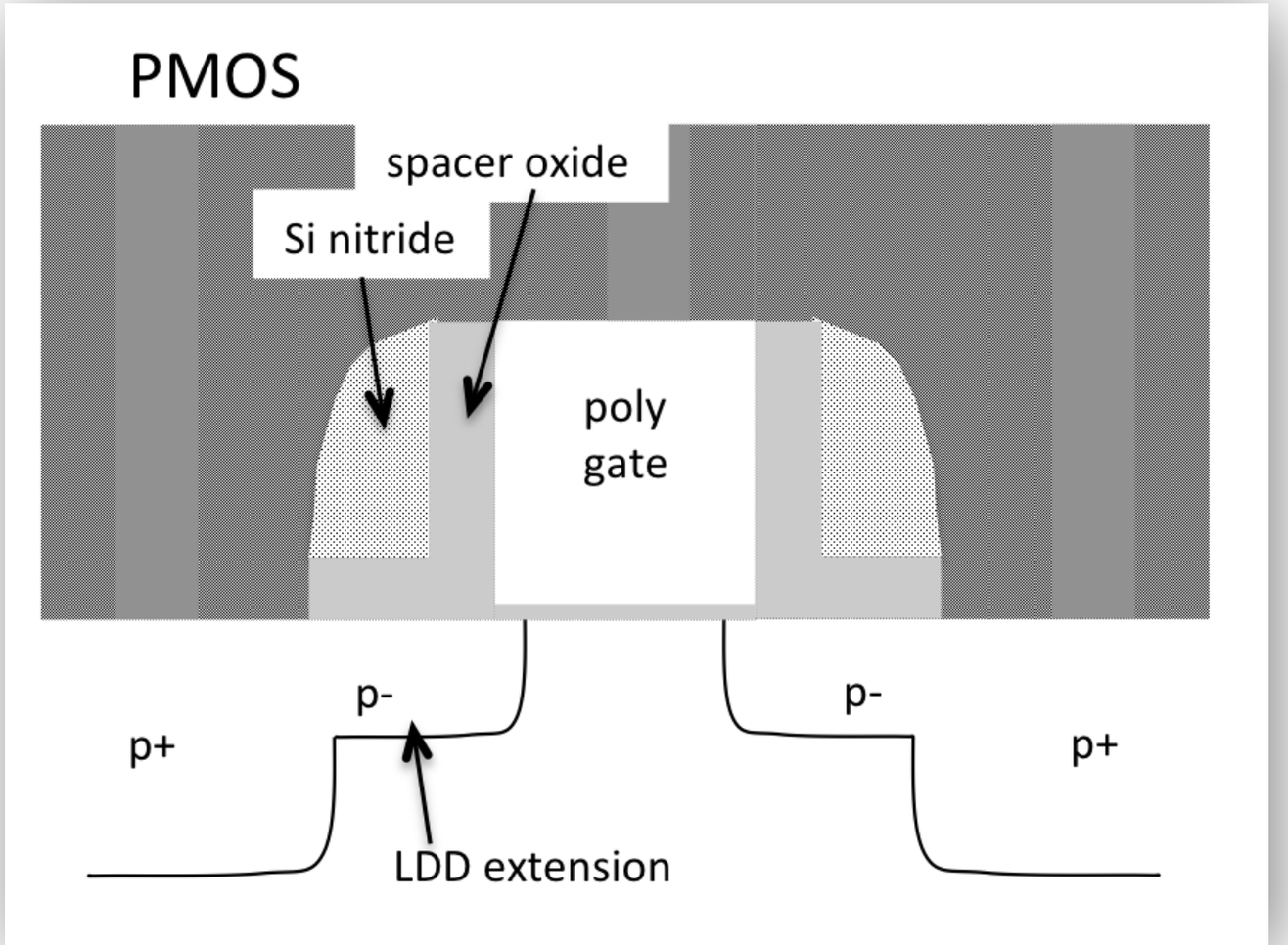
2. Threshold voltage shift

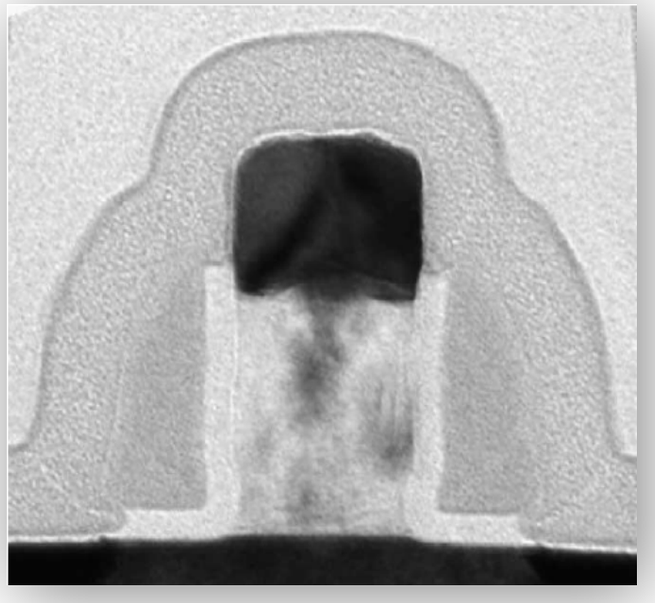
During or after irradiation depending on transistor polarity, temperature, applied bias



This is particularly relevant for PMOS transistors!

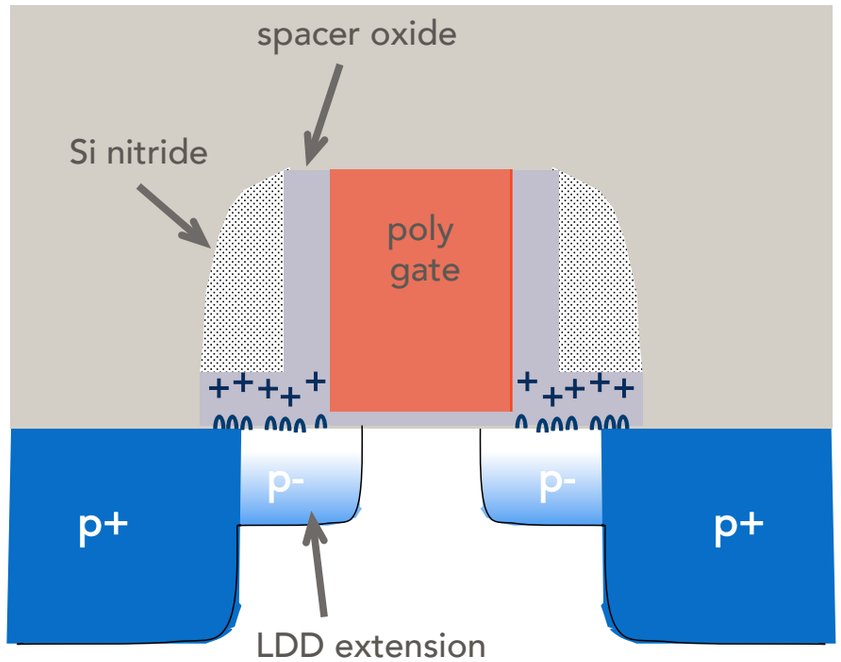
Both effects originate in the LDD spacers





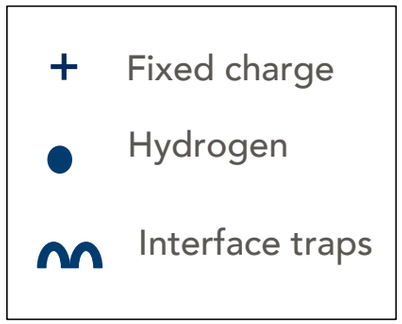
TEM image

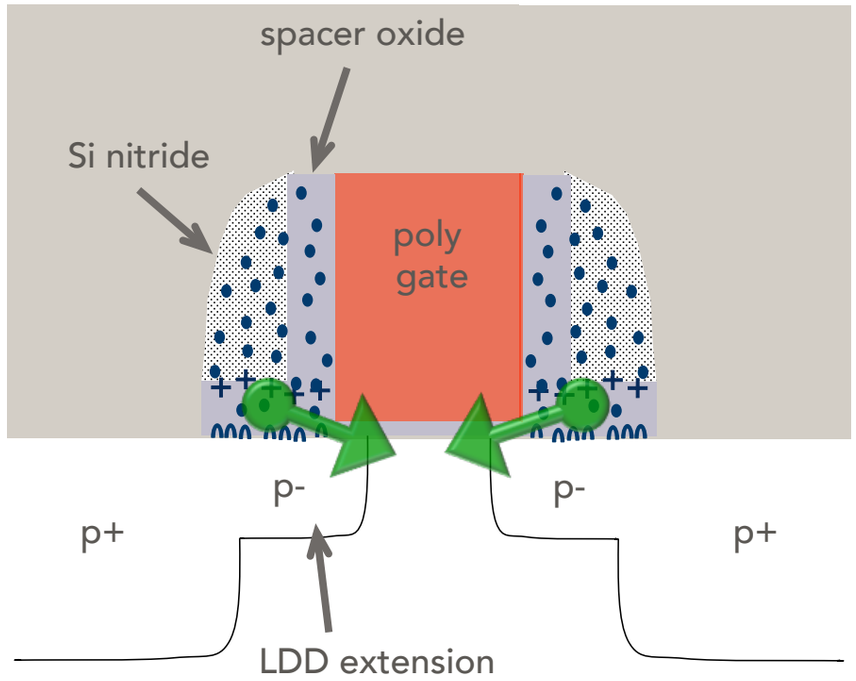
1. Decrease of on-current during exposure



The buildup of charge in defects located in the spacer oxide influences the amount of carriers in the LDD extensions, affecting the parasitic series resistance

2. Threshold voltage shift



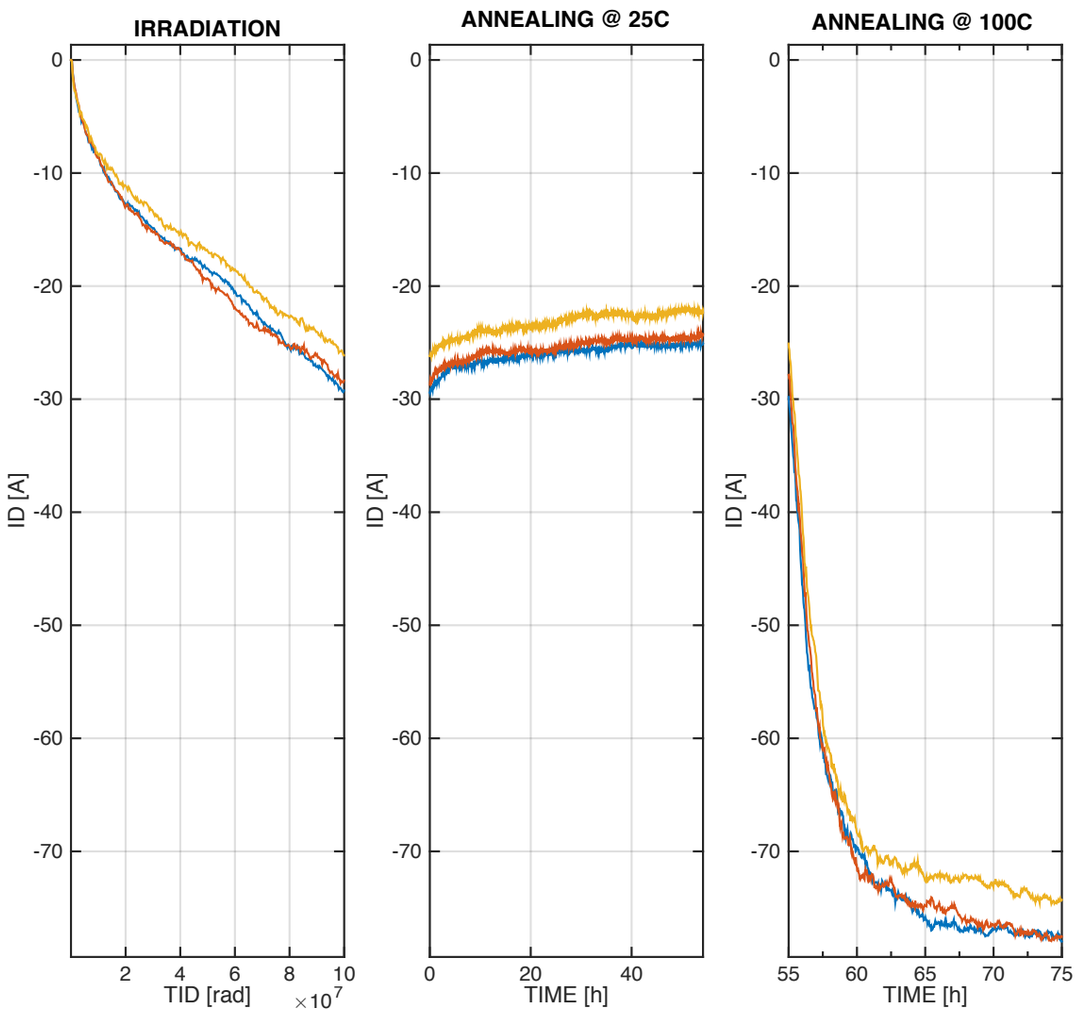


Ionization in the spacers frees hydrogen (protons, neutral and/or molecular hydrogen).
This can later transport and reach into the gate oxide where it can de-passivate Si-H bonds.
Coming from the source/drain spacers, it will give origin to defects concentrated close to these regions.

Standard qualification procedures for CMOS foresee a 1-week annealing period post-irradiation at 100°C. This considerably worsens the performance of PMOS transistors.

Is this needed AND is this representative of the real degradation?

Delta Id (%)

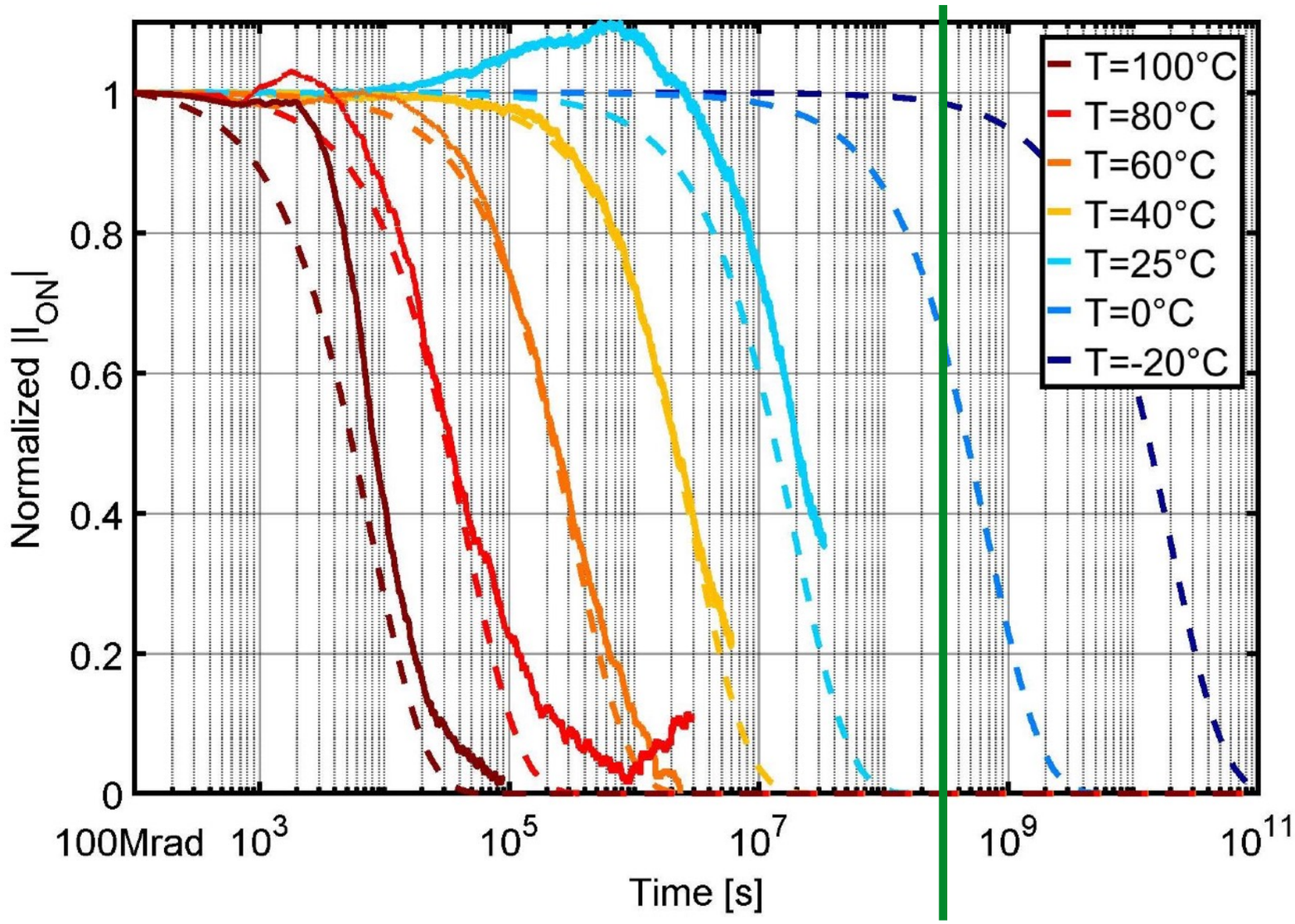


Decrease of I_{on}

V_{th} shift

Transistors' size: W=0.6um, L=60nm
Irradiation conditions:
* Bias:
"Diode" => |Vgs|=|Vds|=1.2V

We have extracted the activation energy extracted of 0.92 eV for the process.
We can hence estimate the post-irradiation evolution of the transistors's current at different temperature.
The evolution is considerably slower below 0°C.
No need to take the Vth shift of PMOS into account IF circuits are forbidden to be biased at high temperature (cut power supply if T>0°C?)



For those wishing to know more…

F. Faccio et al., "Influence of LDD spacers and H^+ transport on the total-ionizing-dose response of 65 nm MOSFETs irradiated to ultra-high doses", to be published in IEEE Trans. Nucl. Science, Vol.65, No.1, January 2018 - already available via IEEE Xplore. (Recipient of the Outstanding paper award at the 2017 NSREC in New Orleans)

Talk of G.Borghello (CERN) at the 2017 TWEPP that can be found under the header "Total Ionising Dose response of 65nm MOSFETs irradiated to ultra-high doses" in the CERN Foundry Services web page:

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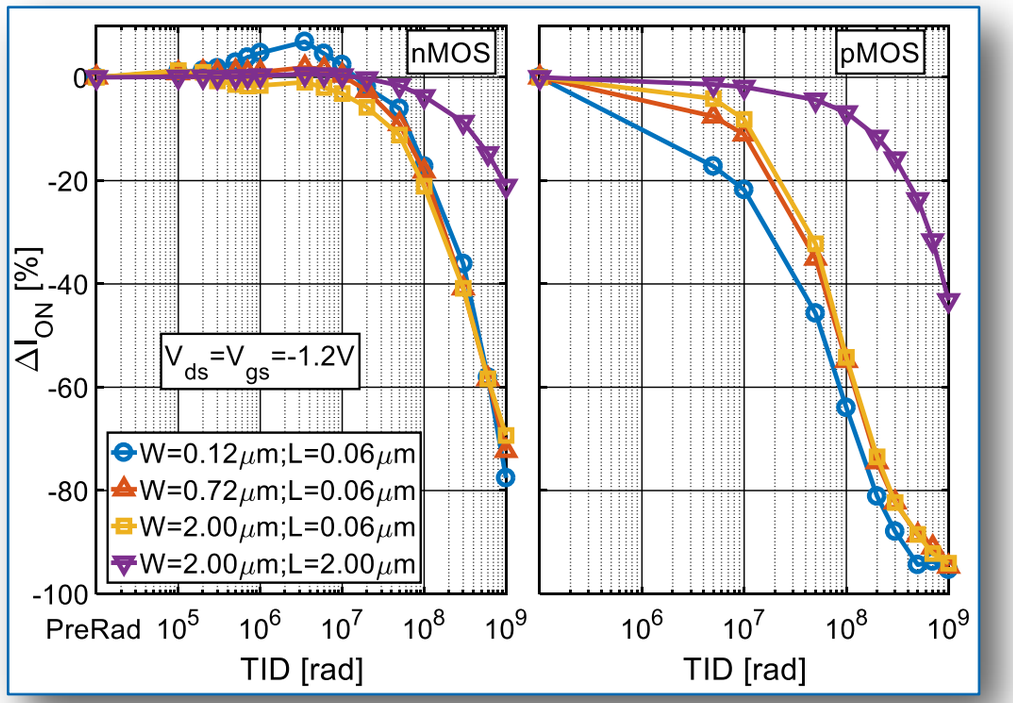
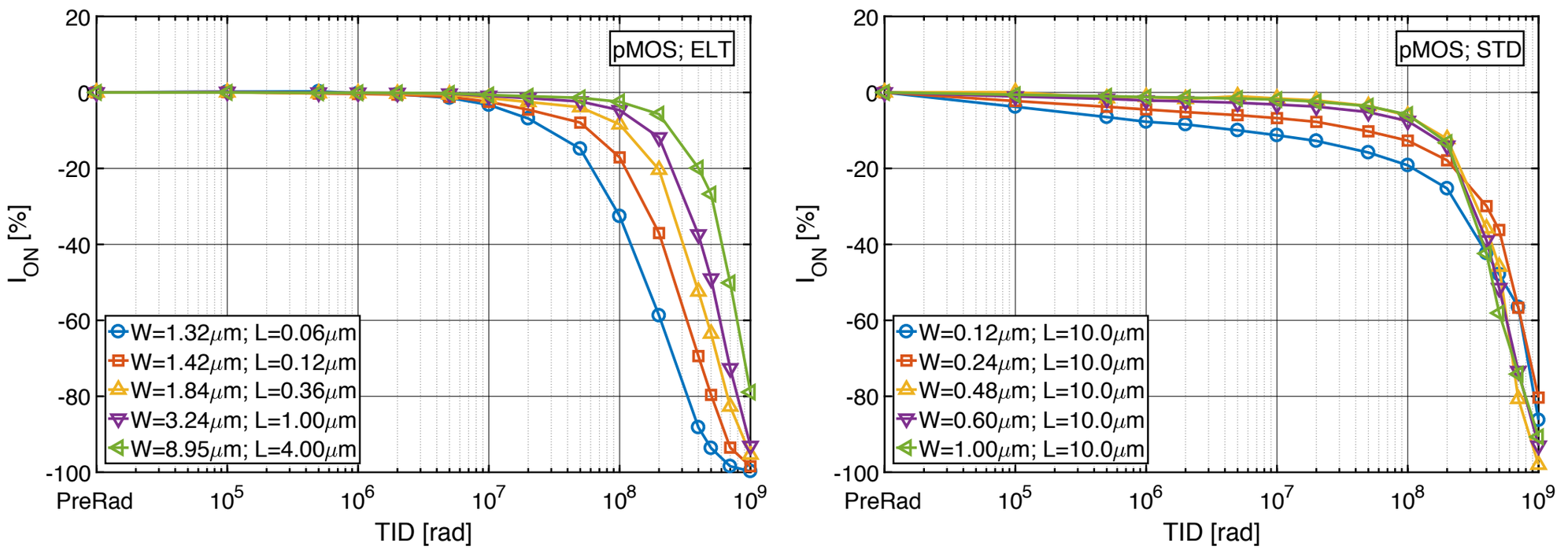
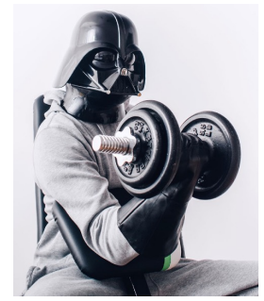
Measurements on samples from other two 65nm manufacturers showed comparable or even worse damage

Supplier X



Supplier Y





Leakage current “peak” in 130nm ICs

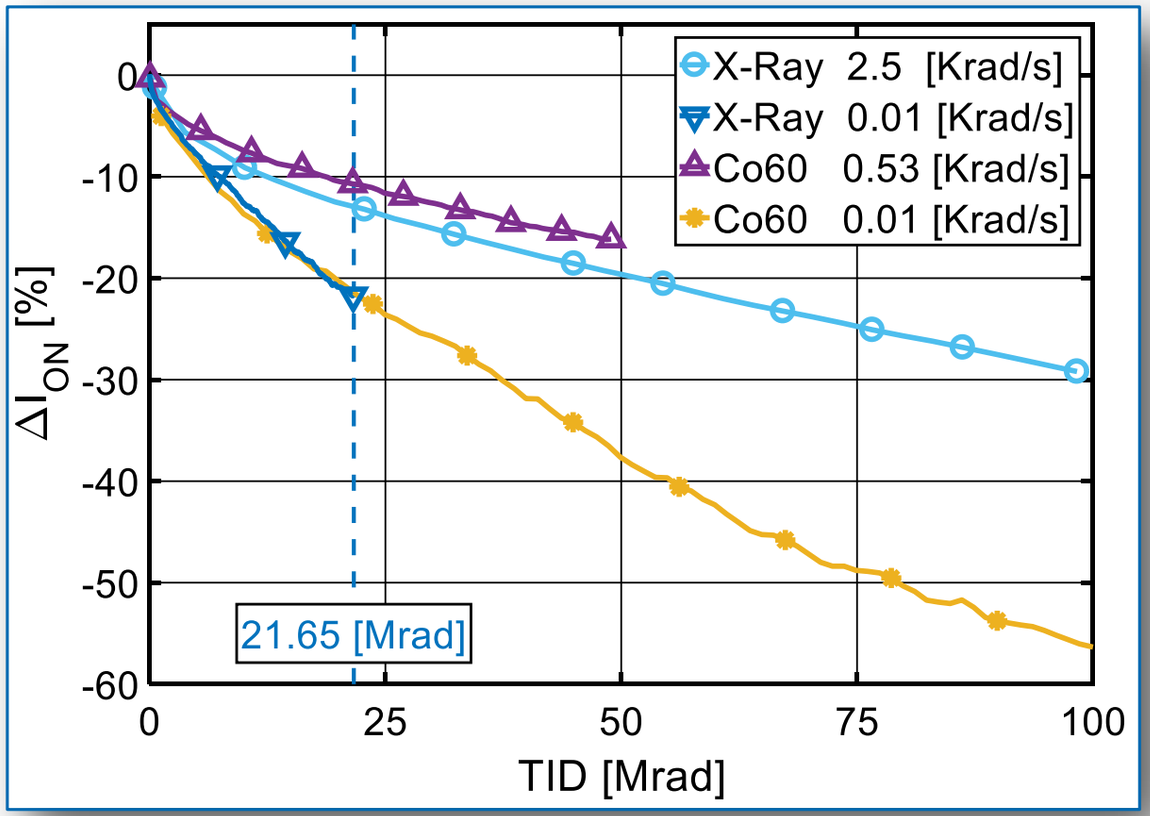
Variability in radiation response (novel 130nm process)

Large degradation in 65nm transistors (short and narrow channel effects)

True Dose-Rate effect in CMOS

SEL in almost production-ready ICs (novel 130nm process)

Measurements on identical samples in the 65nm technology at different facilities (X-rays and ^{60}Co) show a consistent trend to larger damage at lower dose rate

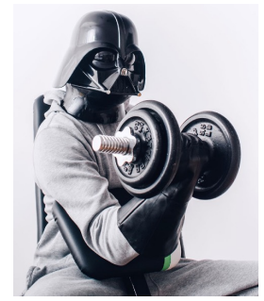


Qualitatively similar results are observed in samples from our "novel" 130nm technology

This dose rate dependency of the damage has to be studied:

- **bias and temperature dependence**
- **physical origin (STI? Spacers?)**
- **influence of the transistor's size**

The effect should then be included in our qualification procedure!



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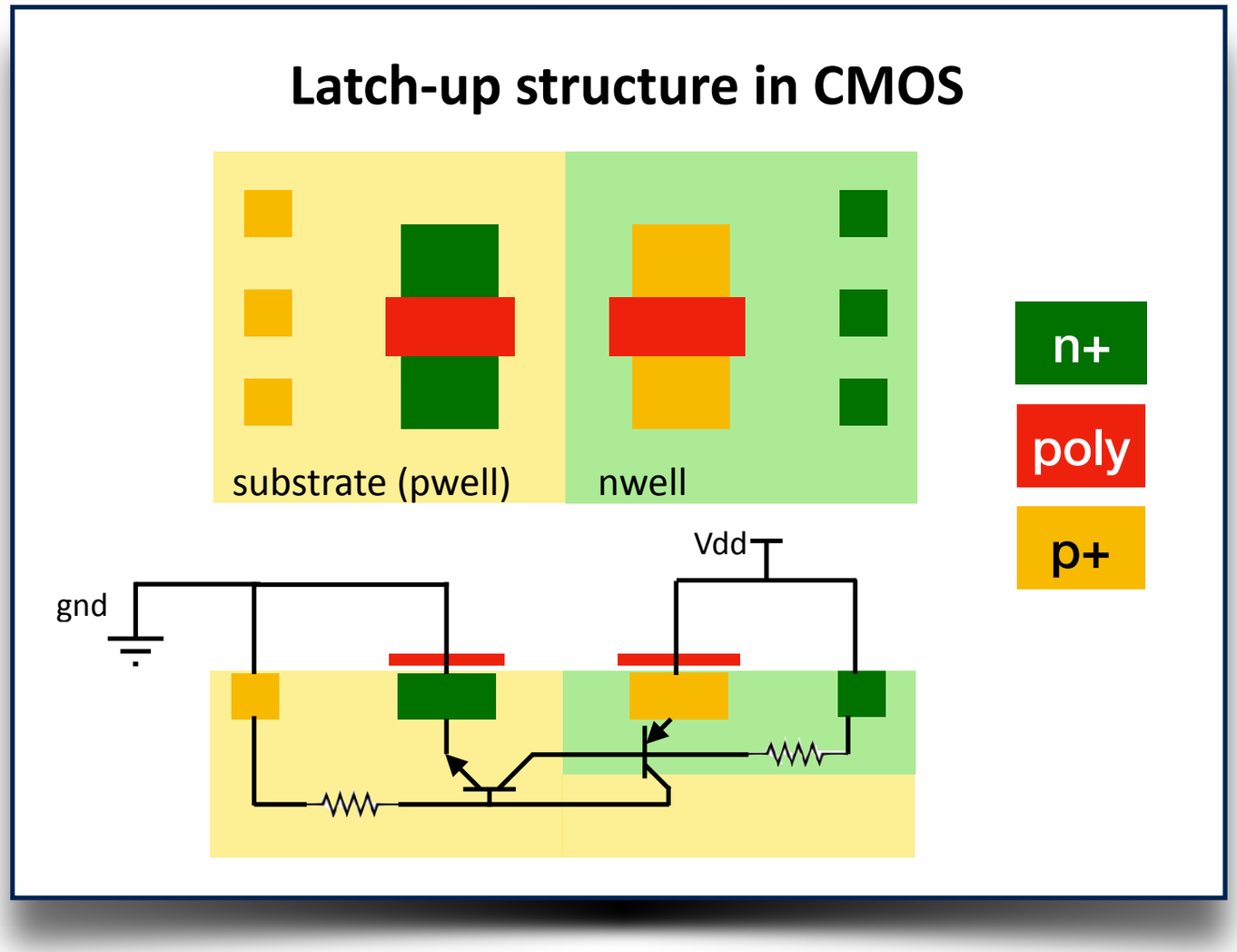
Single Event Latchup was observed in full ASICs designed in the “novel” 130nm technology:

Velopix (LHCb)

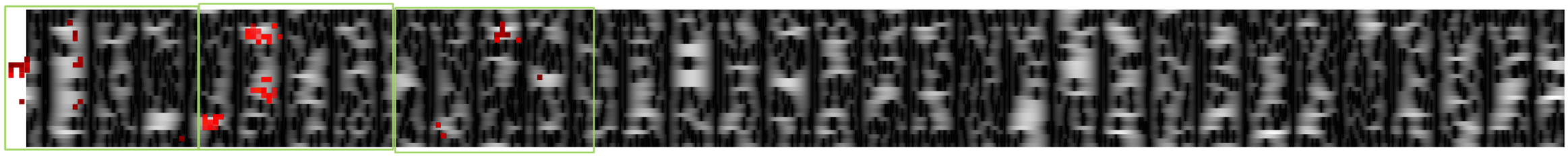
SEL observed during heavy ion tests in Louvain-la-Neuve, then confirmed and localised with pulsed laser tests in Montpellier

SAMPA (ALICE)

SEL observed during 180MeV protons irradiation

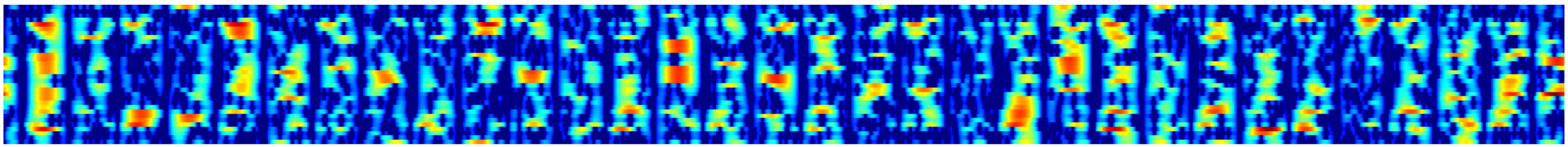


For Velopix, a map of the sensitive points was produced scanning a part of the logic with a pulsed laser beam.



Map produced by the pulsed laser test

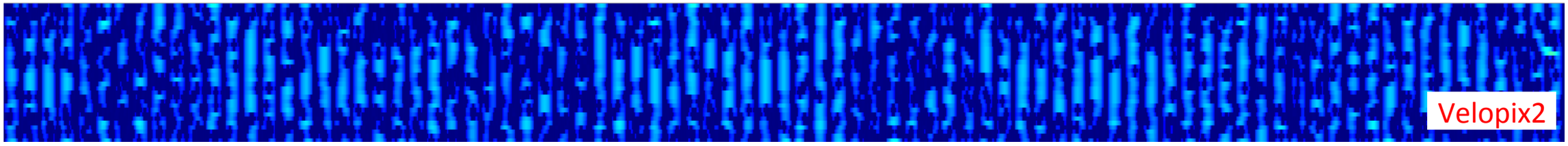
The map was compared to the one produced by a software script run on the layout and producing a colour-coded map of the distance to the nearest substrate/well contact (dark blue = small distance; red = large distance).



Map produced by the software script

SEL sensitive regions correspond to those with the largest distance!

The High Density logic in Velopix has been modified in Velopix2.
As shown in the software-produced map for this new version, the distance from the NWELL and Substrate contacts has been decreased systematically to a maximum of 10um.



Velopix2 has been irradiated with heavy ions and no SEL has been detected!

Talk at the 2017 TWEPP that can be found under the header “Single Event Latchup in 130nm circuits” in the CERN Foundry Services web page:

https://espace.cern.ch/asics-support/docs/_layouts/15/start.aspx#/SitePages/Conferences.aspx

if you do not have access, email a request to foundry.services@cern.ch

OF RADIATION

Do not blindly trust “common sense”!

Radiation effects are complex and often surprising…

Radiation and magnetic field tolerant DCDC converters

High voltage & radiation tolerance

EMI requirements

Air core inductors

Sensitivity to displacement damage

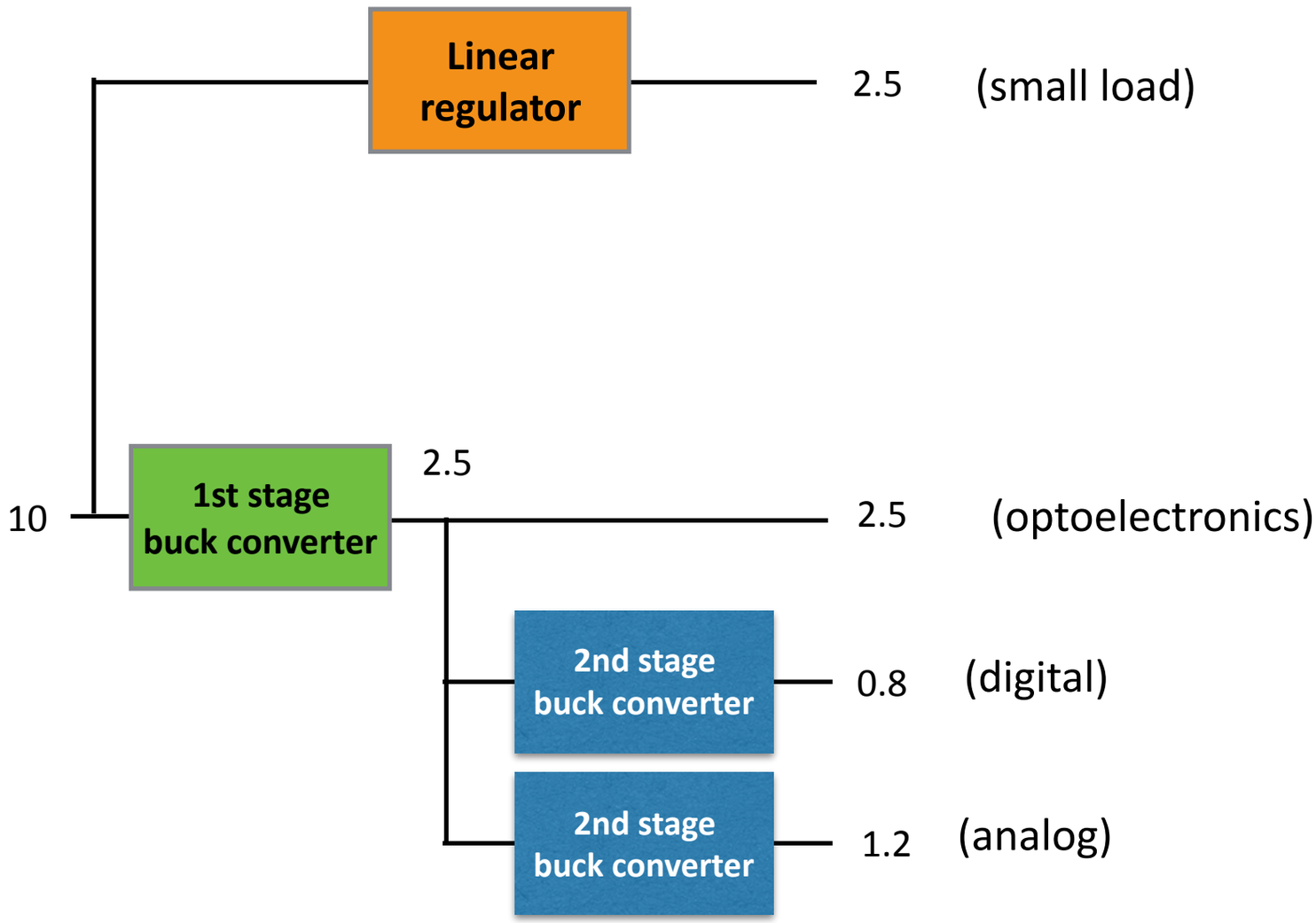
Large current switching

Packaging (cooling, large currents)

Reliability requirements

Within CERN-ESE, we develop radiation and magnetic field tolerant components for a flexible power distribution system

Example implementation



1st stage buck converter

Two versions of the first stage converter are/will be available

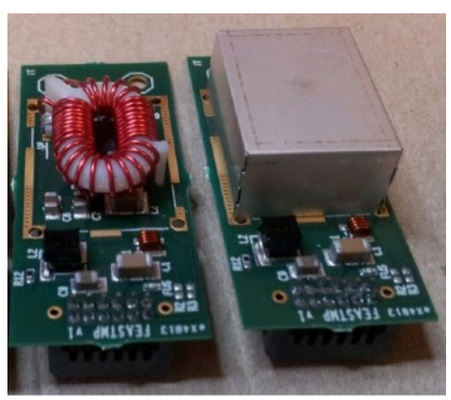
Common specifications

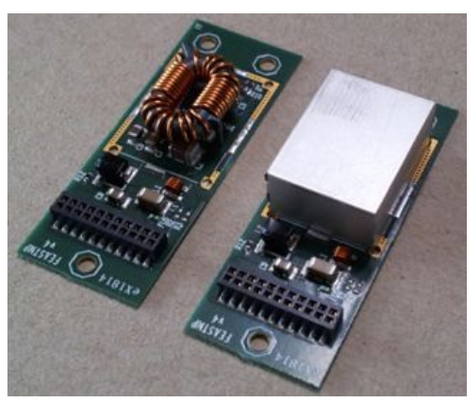
Main electrical parameters	
Input voltage*	5 - 12 V
Output voltage	0.6 - 5 V
Output current*	0 - 4 A
Max output power*	10 W
Programmable switching frequency*	1 - 3 MHz
Inductor value*	0.15 - 1.5 uH
Protection features	
Over-current protection peak level	~6 A
Over-temperature protection threshold	~100°C
Under-voltage lockout threshold	~4.5 V
Soft-Start duration	~470 us
Control features	
Enable (input) threshold	~815 mV
Power Good flag (output)	Open Drain
Radiation tolerance	
Total Ionizing Dose	> 300 Mrad
Displacement Damage (1MeV eq. neutron flux)	version dependent
SEEs: absence of destructive events and of output power interruptions	> 65 MeVcm^{2}mg^{-1}

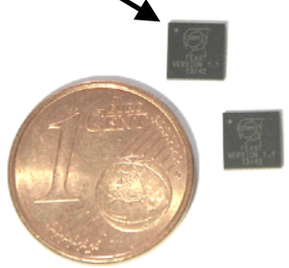
* Safe operating conditions are application-dependent

Main distinctive features

	FEAST2.1	bPOL12V
Displacement Damage tolerance (1MeV eq. neutron flux)	5x10^{14} n/cm^2	>2x10^{15} n/cm^2
Development status	Production (>60,000 already distributed)	Final Prototype
Availability	Packaged chip (QFN32) 2 DCDC modules	Packaged chip (QFN32)







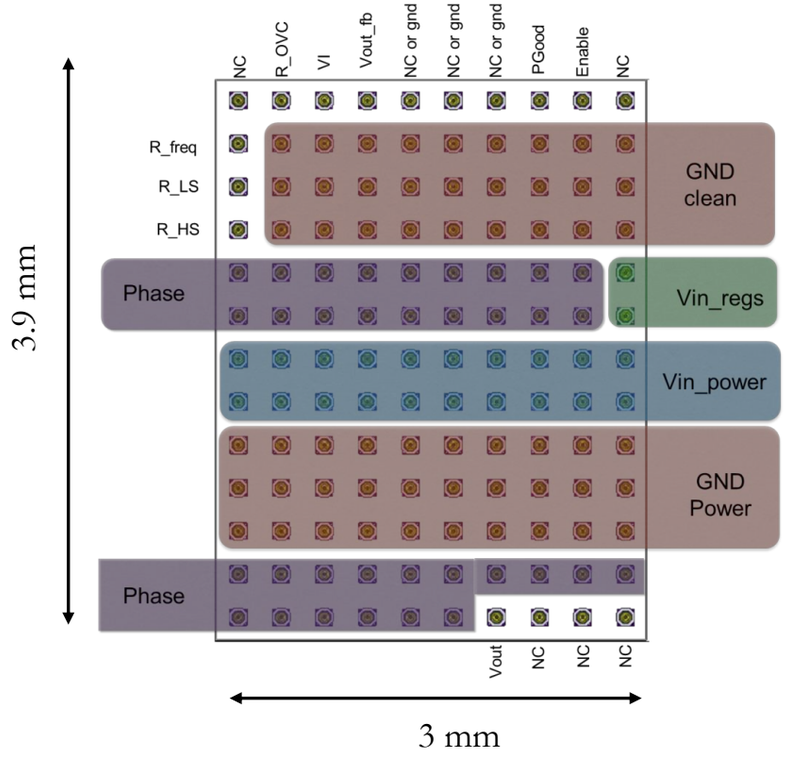
2nd stage buck converter

bPOL2V5 is the prototype 2nd stage buck converter, developed in 130nm CMOS

(reference: G.Ripamonti's talk at TWEPP2017 "A 2.5V Step-Down DC-DC converter for Two-Stages Power Distribution Systems")

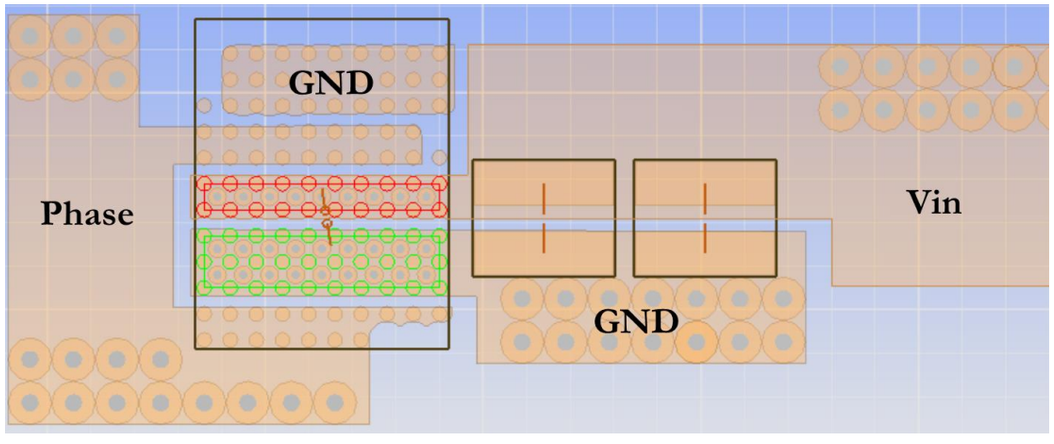
Target specifications

Input voltage	2.0V ÷ 2.7V
Output voltage	0.6V ÷ 1.5V
Output current	≲ 3A (optimized @ 2A)
Switching frequency	> 4MHz
Inductor value	< 150nH
External components	Only C_{in}, C_{out}, L
Assembly	C4 Bump-bonding
Radiation Tolerance	
Total Ionising Dose	> 300 Mrad
Displacement Damage	> 4 10^{15} n/cm^2
SEEs: absence of destructive events and of output power interruptions	> 40 MeVcm^{2}mg^{-1}



Chip dimension and bump array

PCB layout is critical for reliable integration



A second prototype will be characterised in January (assembly is very time consuming).
An alternative resonant architecture is explored, allowing to lower the inductance value to 10nH

Linear regulator

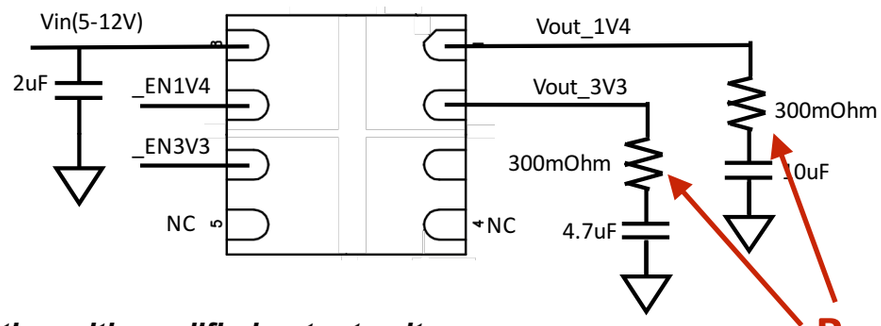
linPOL12V is the prototype 2-channels linear regulator working with an input voltage of up to 12V

(custom development for ATLAS ITK, but could be made available for other groups)

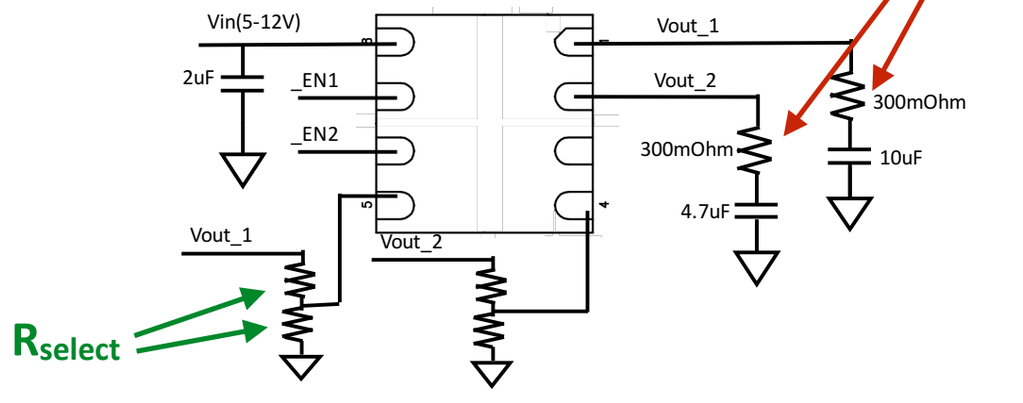
Target specifications

Input voltage	5V ÷ 12V
Output voltage	0.6V ÷ 5V (1.4V and 3.3V without the addition of external resistors)
Output current	≲ 80mA
External	C_{in}, C_{out}, R_{out}, R_{select}
Package	DFN8 (2x2mm)
Radiation Tolerance	
Total Ionising Dose	> 300 Mrad
Displacement	> 2 10^{15} n/cm^2
SEEs: absence of destructive events and of output power interruptions	> 40 MeVcm^{2}mg^{-1}

Typical application with default output voltages (3.3V and 1.4V)



Typical application with modified output voltages



A first prototype will be characterised in late spring 2018
(but the design is extracted from bPOL12V, already measured in silicon)

A family of components for power distribution systems is being developed at CERN.

These components are meant to help power distribution in HEP experiments where radiation and magnetic field tolerance are required.