Status and roadmap of hybridization technologies technologies technologies relevant to future pixel detectors

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3D-IC Technology ≠ LSI Technology

- unpredictable
  Application driven technology
- Need flexibility
  System technology
  Many integration methods

- Predictable
- Precisive but inflexible

3DIC Supply chain

Base devices

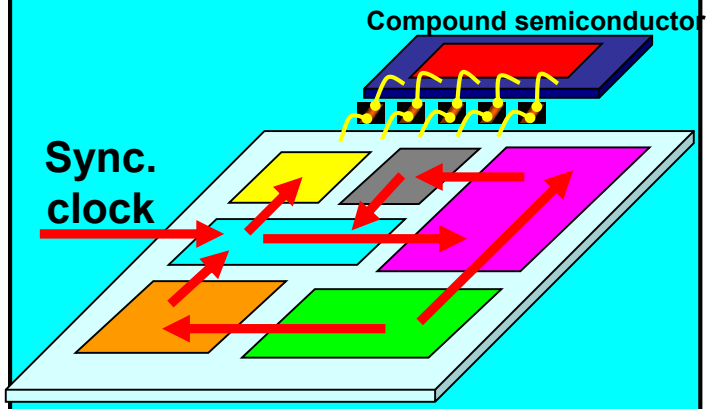
4 inch Si wafer
6 inch Si wafer
8 inch Si wafer
12 inch Si wafer
Shuttle service (LSI Chip)
Compound Semiconductor (Chip/Wafer)

⋮

→ **3D integration**

Unique Points of 3D-LSI

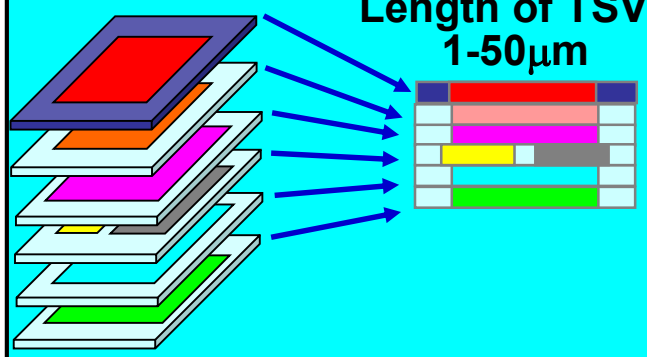
Conventional SoC



Long Global interconnect
→large RC delay, large C_P

Repartitioning Die

3D-SoC

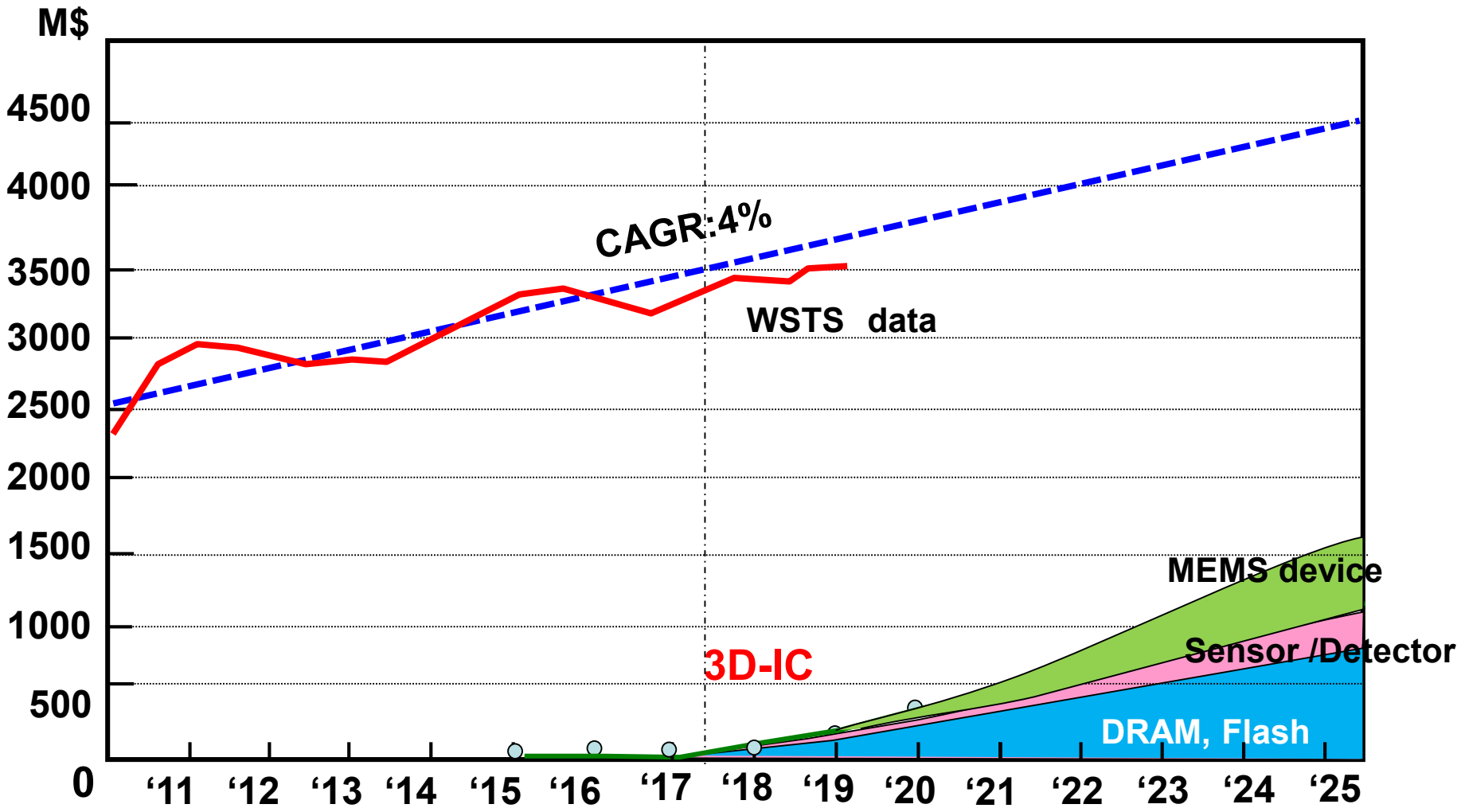


-Short global interconnect
→small RC delay, small C_P
-High band width
-Small form factor

1. Increase of electrical performances
2. Increase of circuit density
3. New Architecture (Hyper-parallel processing, Multifunction, etc)
4. Heterogeneous integration
5. Better yield

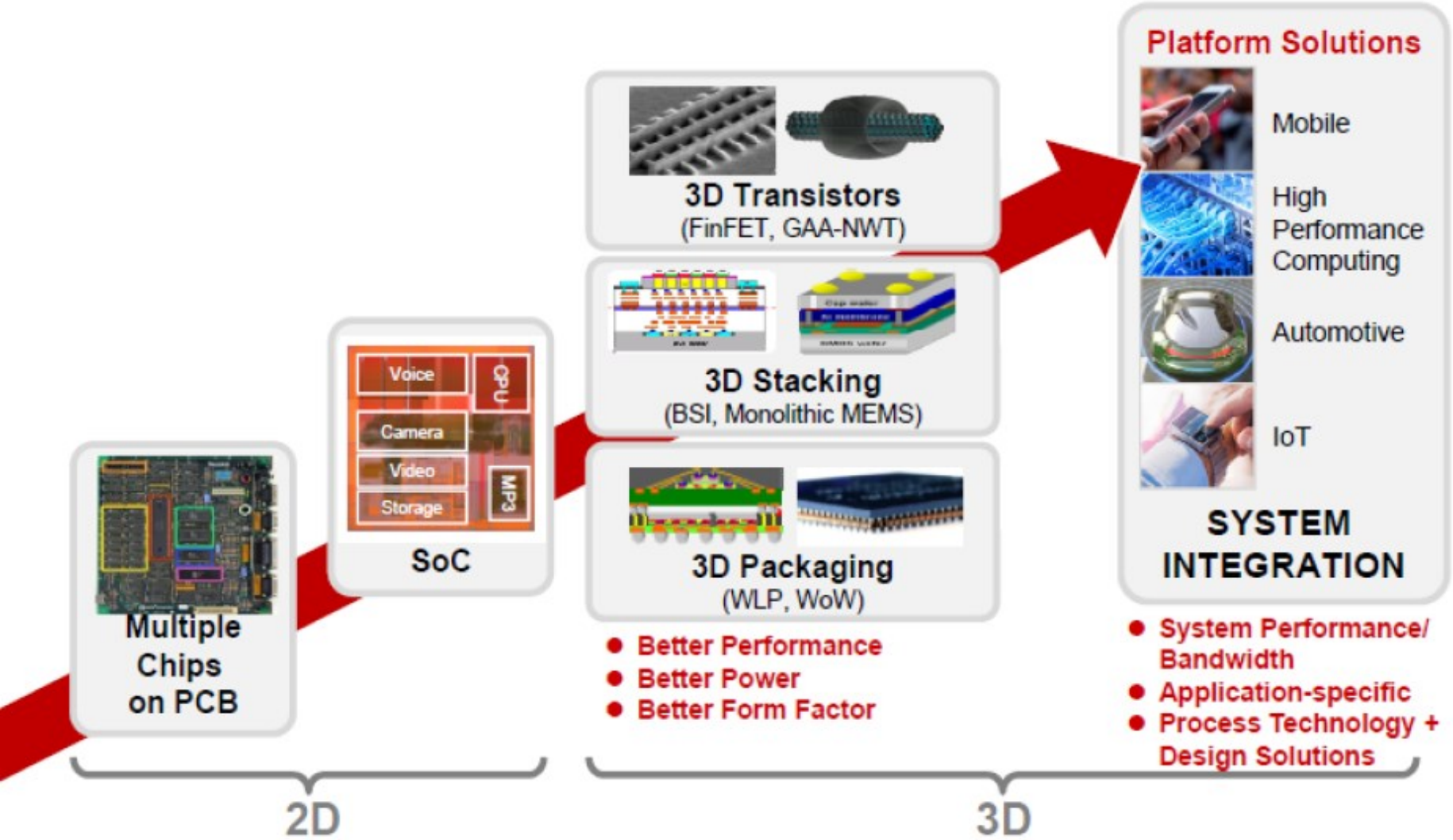
TSV：Through Silicon Via

Semiconductor Market Forecast



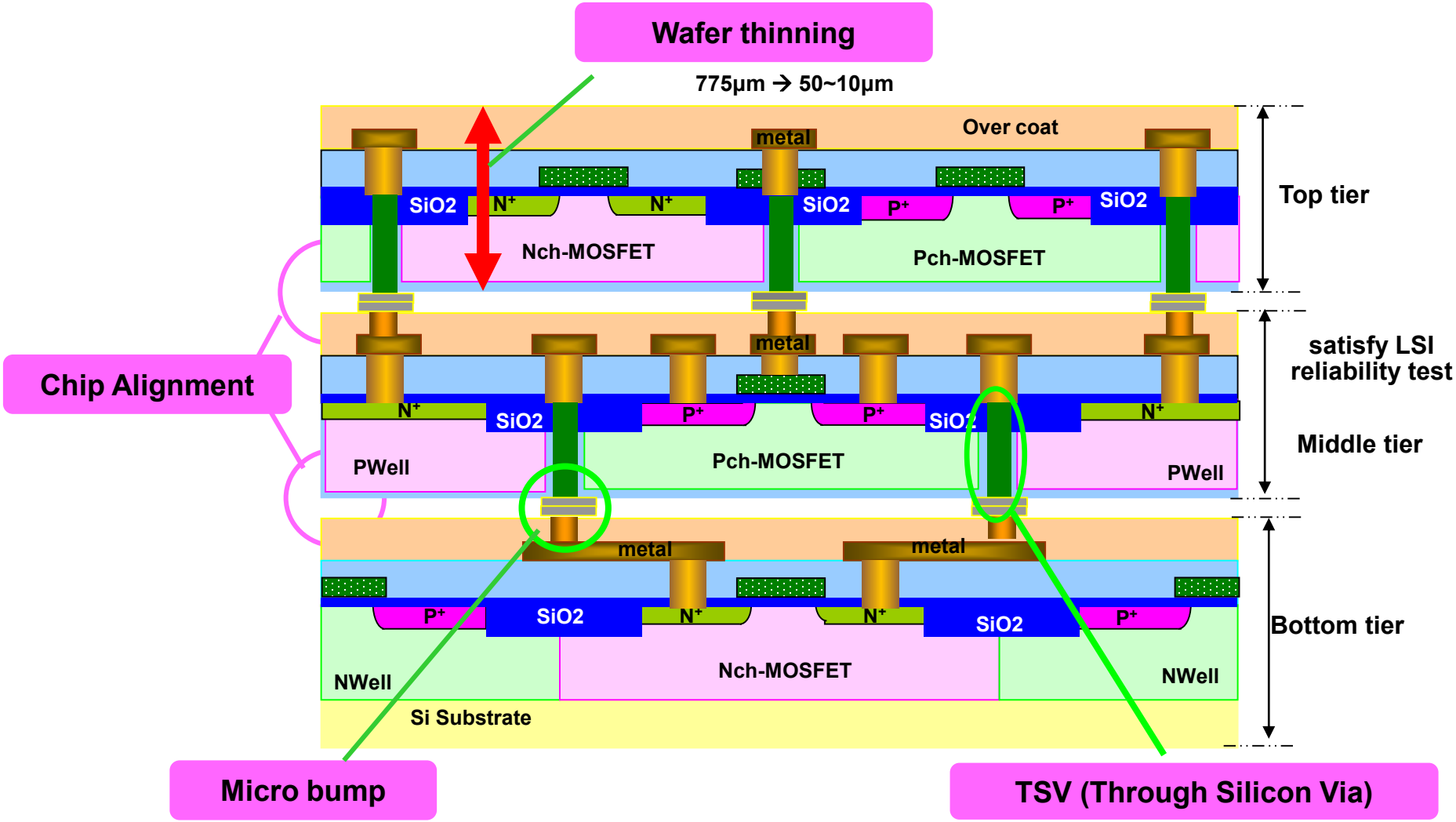
WSTS: World Semiconductor Trade Statistic Inc. (2017)

Chip & System Integration Trends for better PPA & System Performance

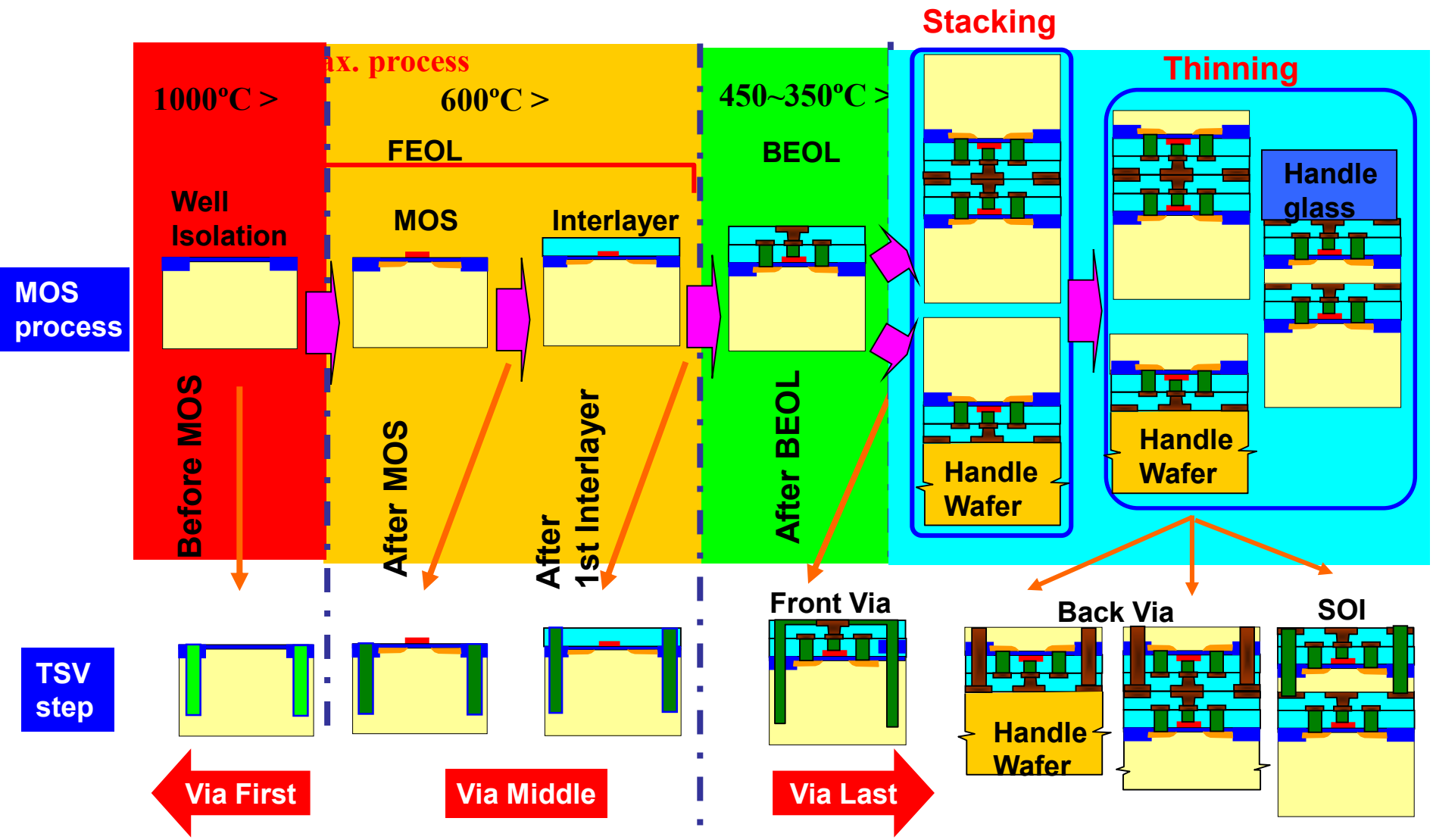


Source: Cliff Hou (TSMC), ISSCC 2017 (Plenary)

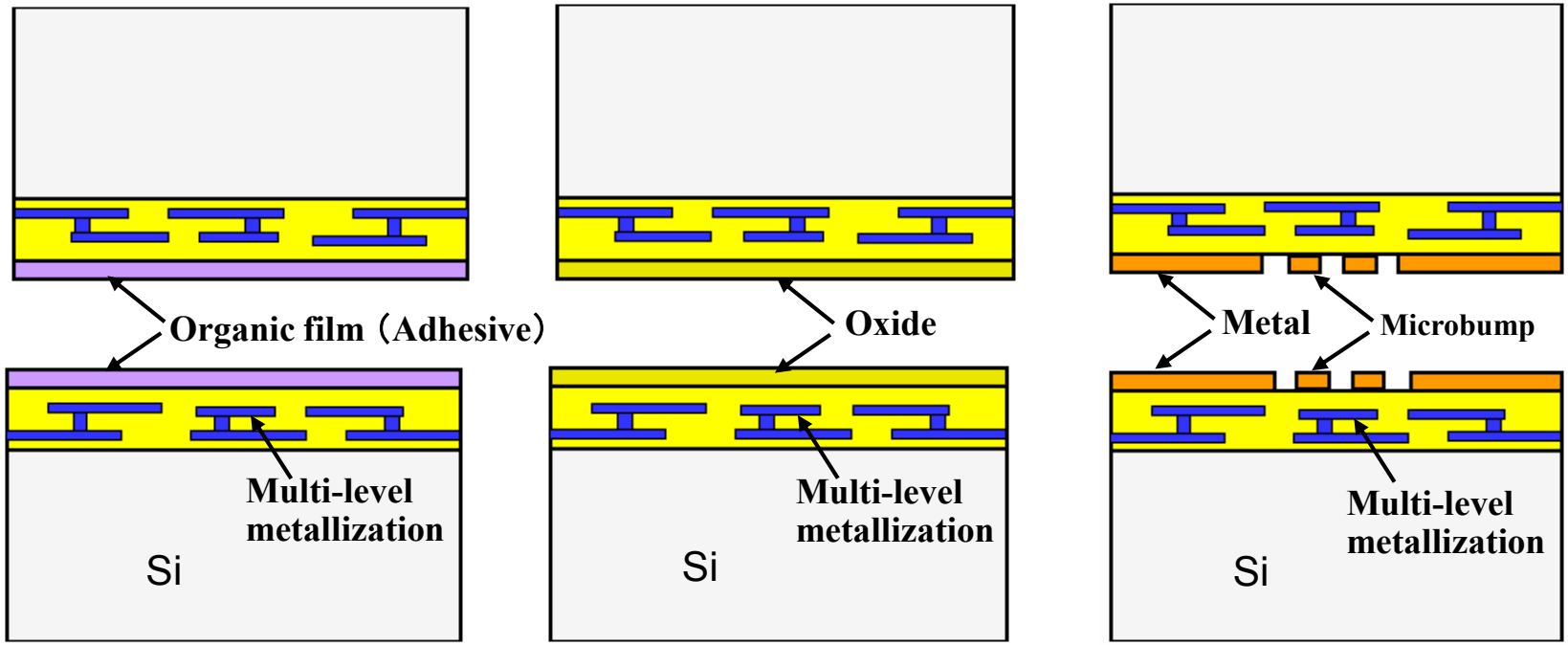
Key technologies of 3D-IC Integration



TSV process classification



Wafer Bonding Methods -1



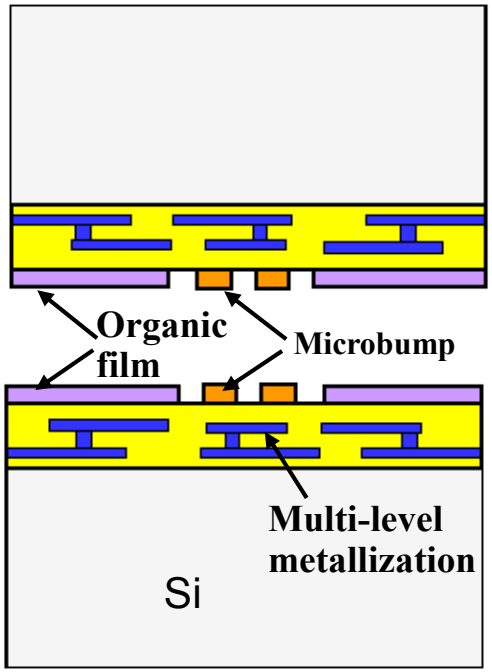
Adhesive Bonding

Oxide Fusion Bonding

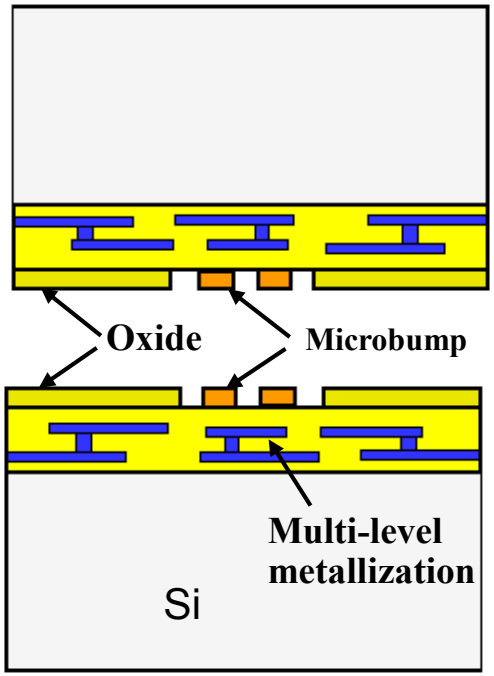
Metal (Cu) Fusion Bonding

Metal (Cu/SnAg) Eutetic Bonding

Wafer Bonding Methods -2



Adhesive/ Metal Bonding



Oxide/ Metal Bonding

(Hybrid bonding)

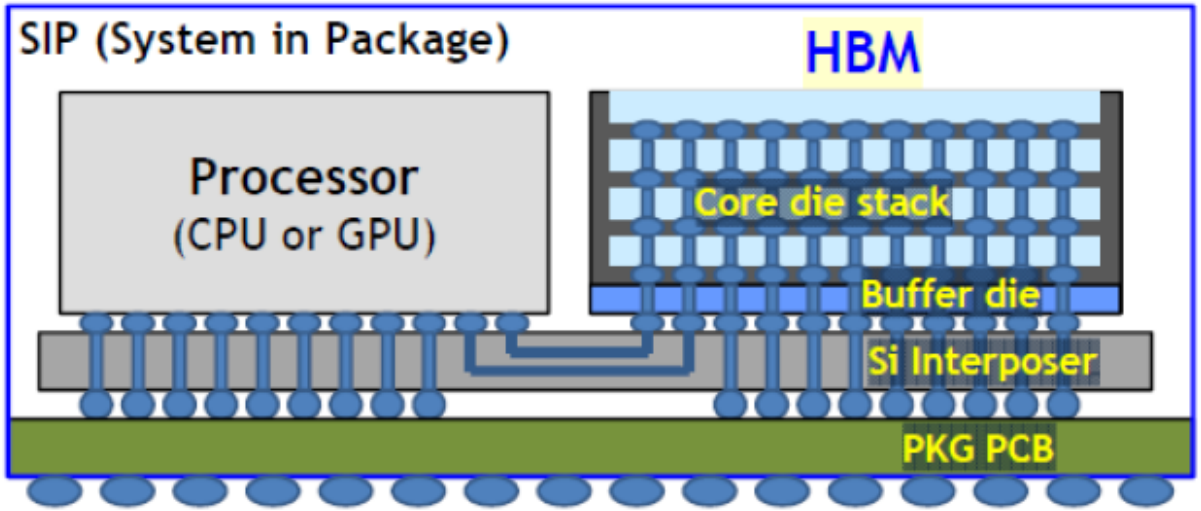
T-Micro

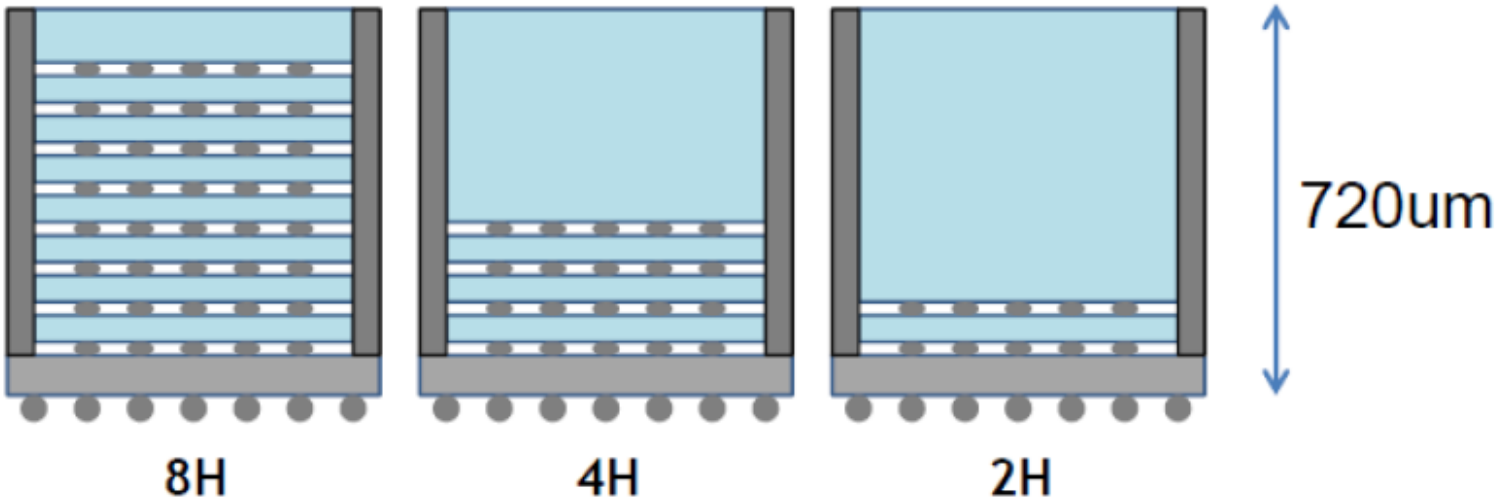
Classification of 3D/2.5D ICs

Type	TSV	Processing	Layer stacking	Application	
				Present	Future
Hybrid 3D	TSV	Wafer level	Bonding	Image Sensor	Image Sensor DRAM
		Chip level	Bonding	DRAM FPGA	DRAM FPGA MEMs/Sensor Analog IC
		Wafer+ Chip	Bonding		Image Sensor DRAM Processor
	Non-TSV	Wafer level	Bonding	Image Sensor (BSI)	Image Sensor Logic/SoC
Monolithic 3D	Non-TSV	Wafer level	Depo or Epi	NAND-Flash	NAND-Flash Logic/SoC
Monolithic + Hybrid	Non-TSV + TSV	Wafer level	Mixed	Image Sensor	NAND-Flash Logic/Memory

HBM (High Band Width Memory)

Commercialized 3D DRAM

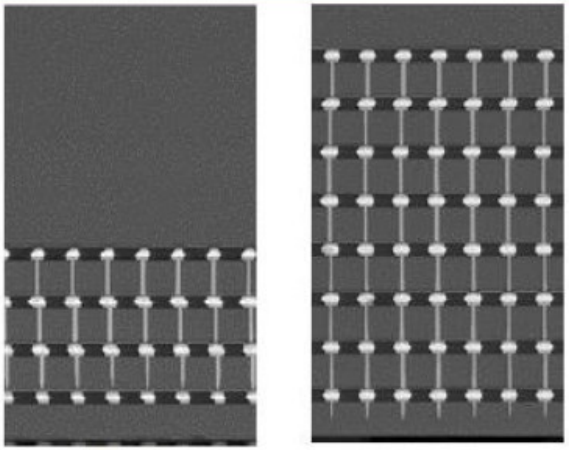




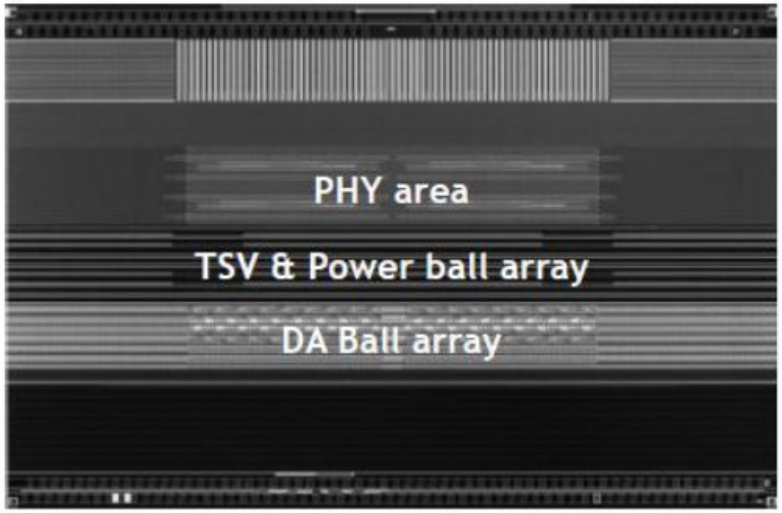
Source: Kyomin Sohn (Samsung), ISSCC2016

Cross-sectional View and Chip Photo of HBM

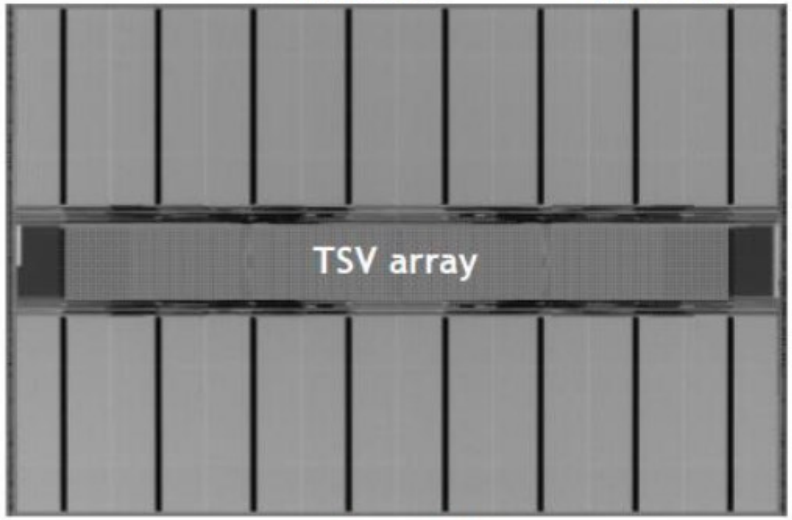
- Process: 20nm DRAM
- Capacity: 9Gb/core die
- Supply voltage: 1.2V/1.2V/2.5V
- Chip size: 12mm x 8mm (buffer die)



4H Case 8H Case



Buffer die



Core die

Source: Kyomin Sohn (Samsung), ISSCC2016

• Comparison table of GDDR5 and HBM Gen1.2

Items	GDDR5	HBM Gen1	HBM Gen2
Pin Data Rate	4~8Gbps	1Gbps	2Gbps
# of IO and CH	1CH, 32 IO	8CH, 128IO/CH	16pCH, 64IO/pCH
Bandwidth	16~32GB/s	128GB/s	**256GB/s**
Voltage (VDDC/VDDQ/VPPE)	1.35V~1.5V	1.2V/1.2V/2.5V	←
Interface	POD (VDDQ Term.)	CMOS (Un-term)	←
Banks	4banks/BG, 4BGs	←	←
Implemented new functions in this work			Pseudo channel, 2H/4H/8H, ECC storage, Implicit pre-charge, Lane remapping, …

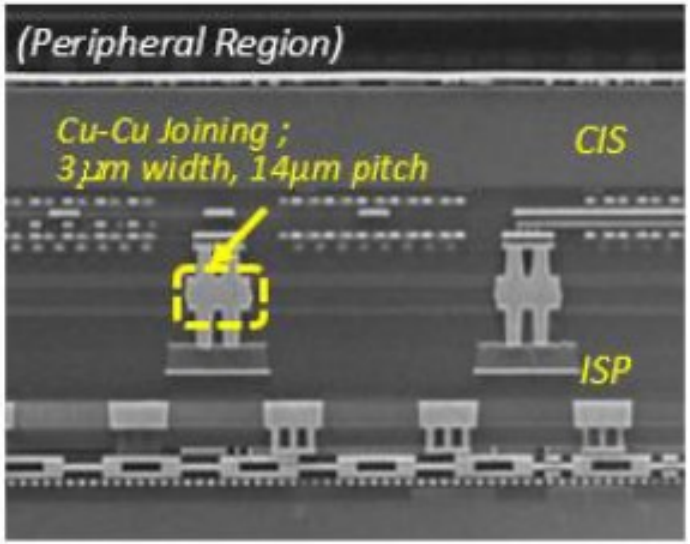
Source: Kyomin Sohn (Samsung), ISSCC2016

Sony / 3D-Stacked Image Sensor

Sony's first CIS module(IMX260) product with Cu-Cu Hybrid bonding

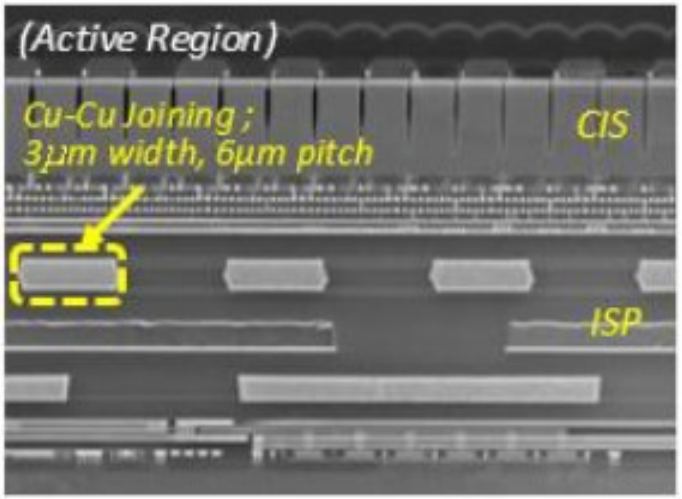
Cu-Cu Via

3um wide
14um pitch

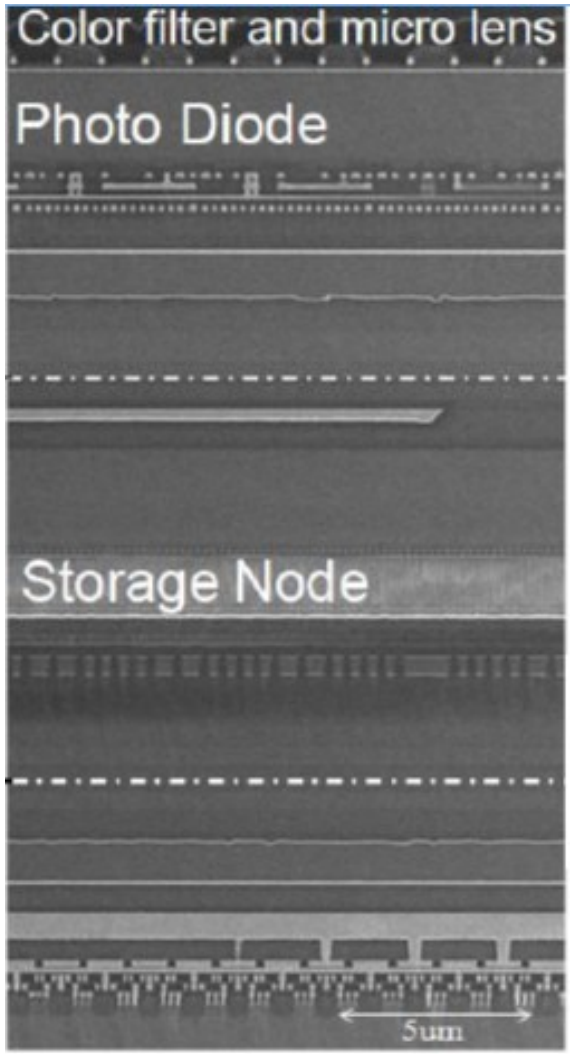


Cu-Cu Via

3um wide
6um pitch



Source: Chipworks, April, 2016



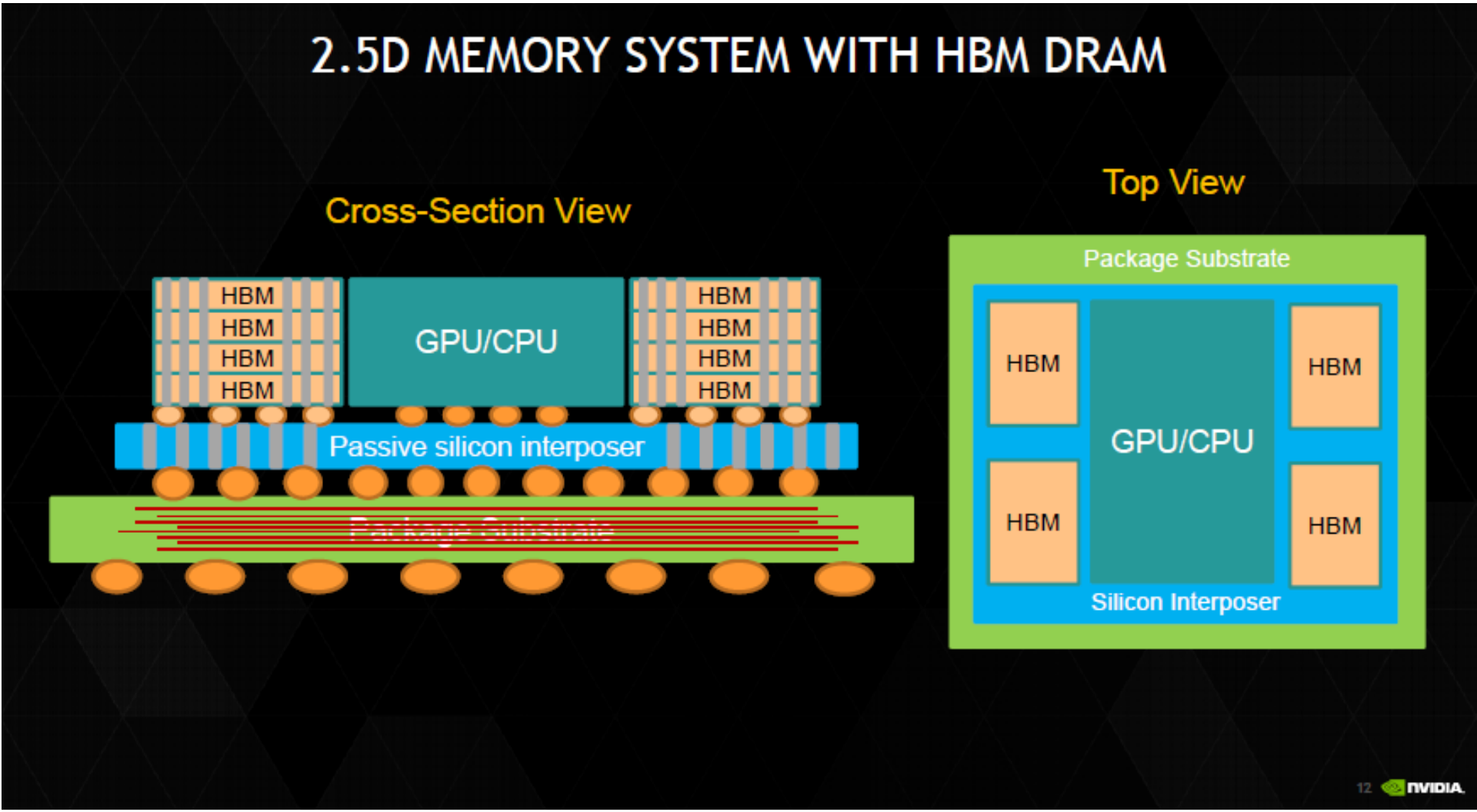
Top part
BI-CIS

Middle part
DRAM

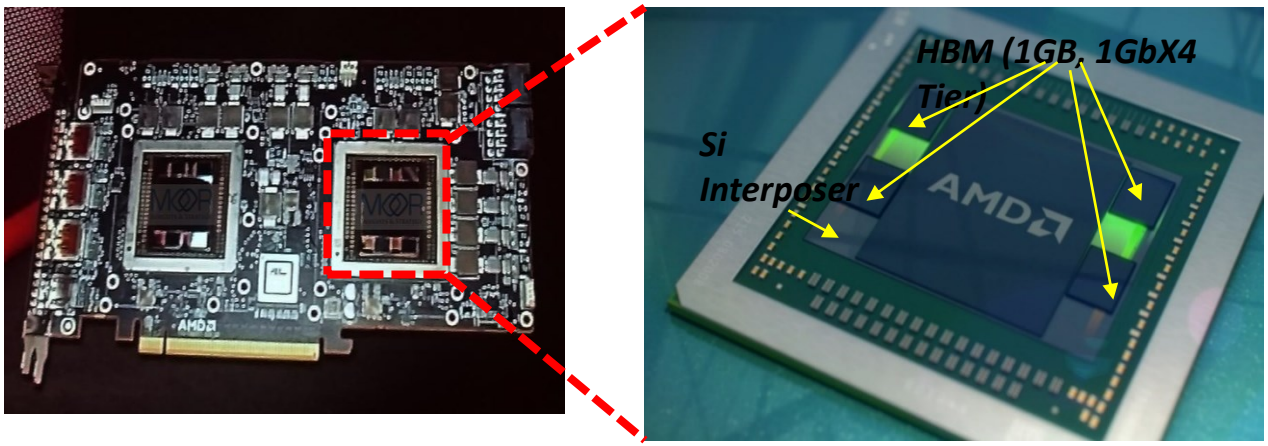
Bottom part
Logic

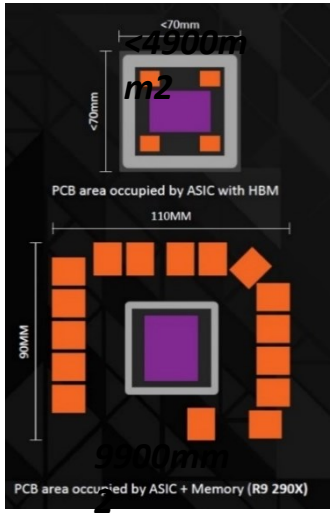
Source: T. Haruta (Sony) ISSCC2017

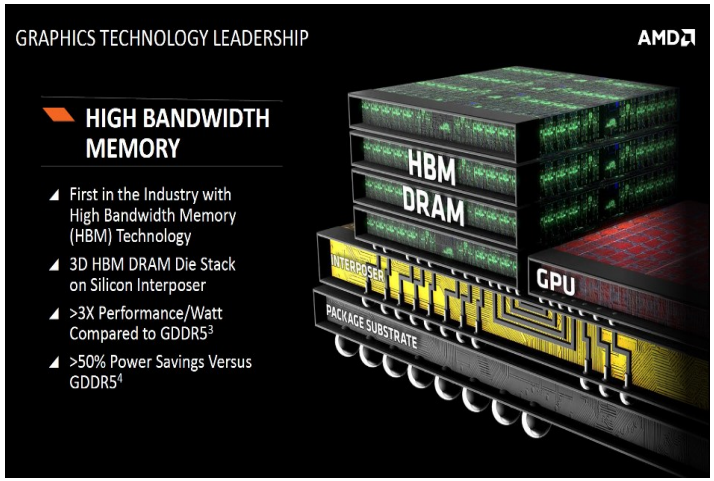
High Density Memory Systens using Si Interposer



AMD reveals HBM-powered Radeon Fury graphics cards, new R300-series GPUs



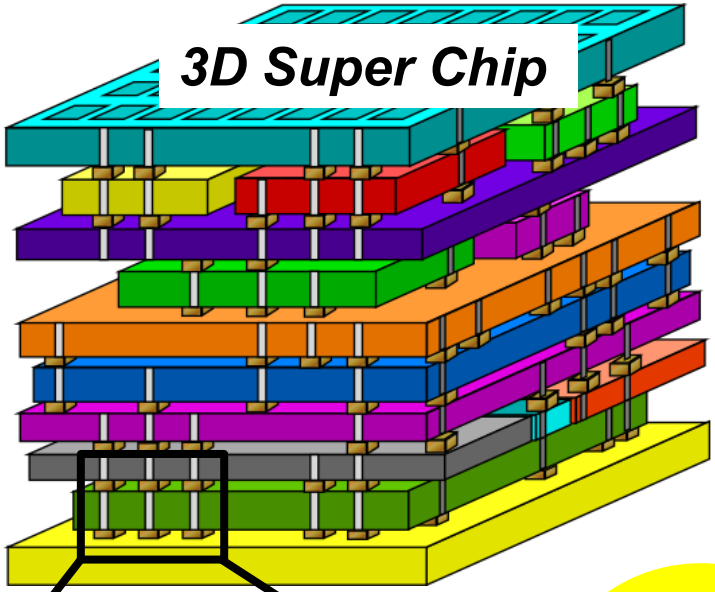




Fury graphics card : $649, June, 2015

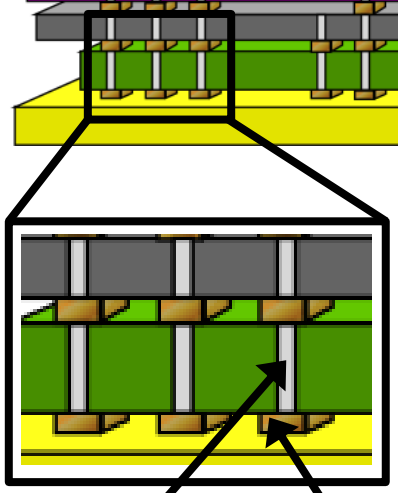
- ✓ *Memory Interface ; 4096bit*
- ✓ *Memory Bandwidth ; 512GB/s*

Highly Integrated Heterogeneous 3D Integrated System

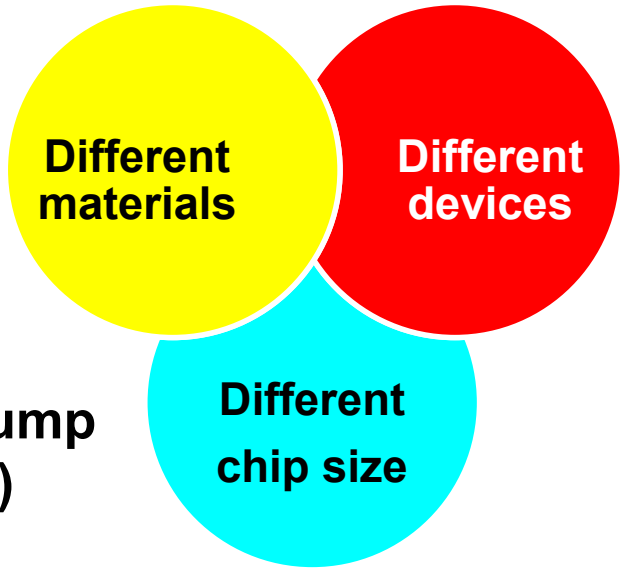


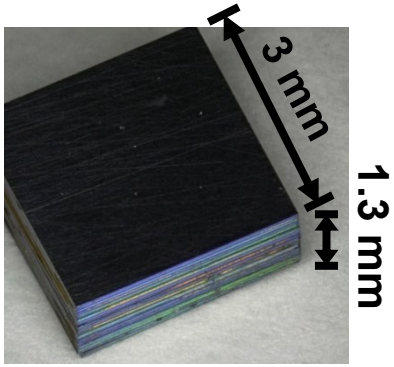
MEMS chip
Sensor chip
CMOS RF-IC
MMIC
Power IC
Control IC
Logic LSI
Flash memory
DRAM
SRAM
Microprocessor

New chip stacking technologies are required



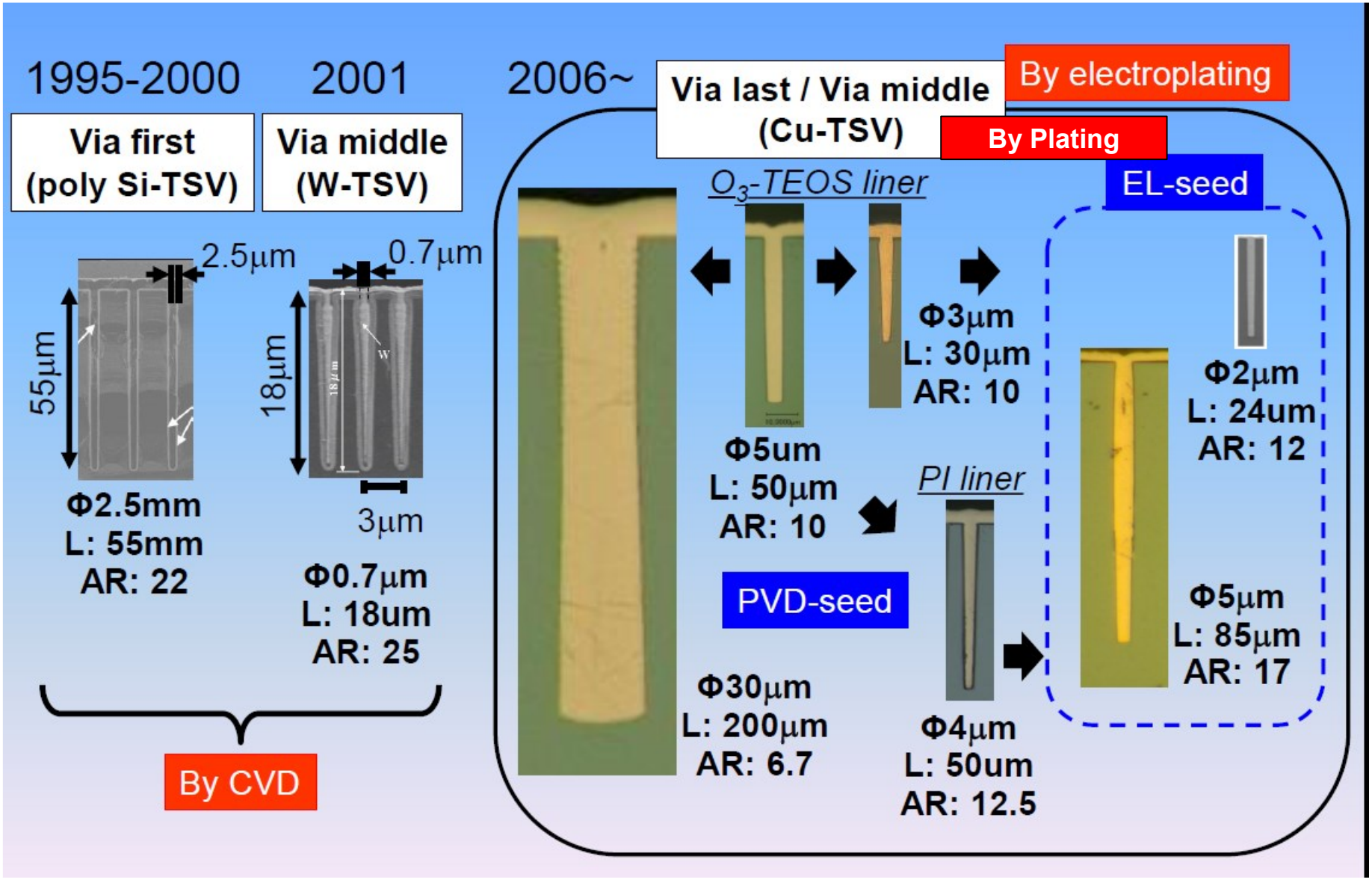
Metal microbump
Through-Si via (TSV)





38-layer chip stack

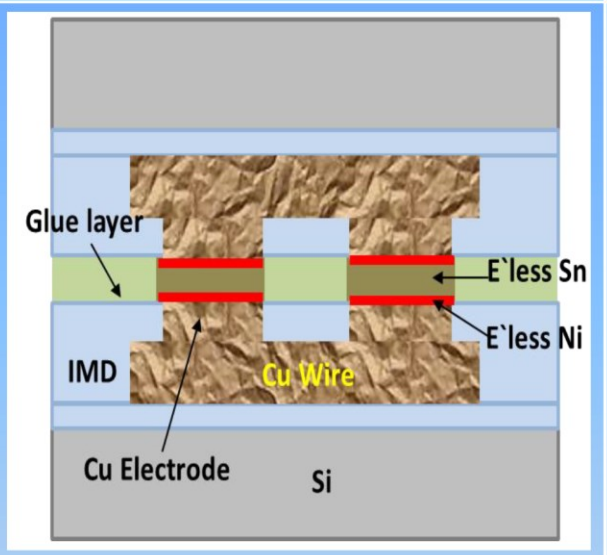
Fine Pitch TSV



T-Micro

Novel Hybrid Bonding Features for Ultra-High Density 3D/2.5D Integration

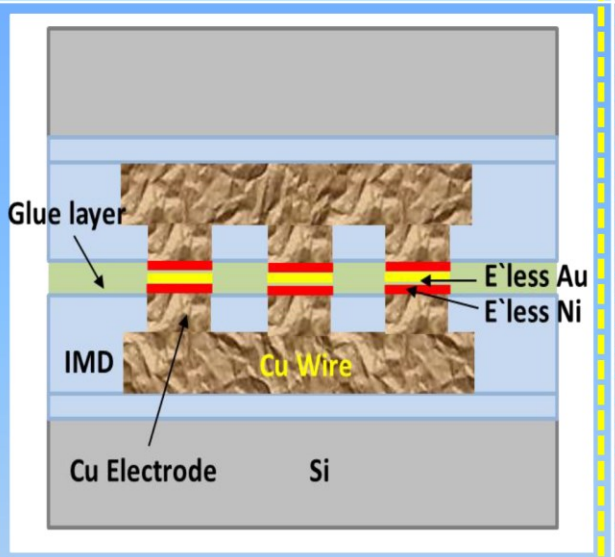
Gigascale



** Target Electrode*
- *Size ; 3um, Pitch ; 6um*
- *Density ; ~ million/die*

** Joining Structure*
- *Electro-less thin Ni/Sn layers on extruded Cu electrode*
- *Thin glue layer (below 1umt) containing flux composition*

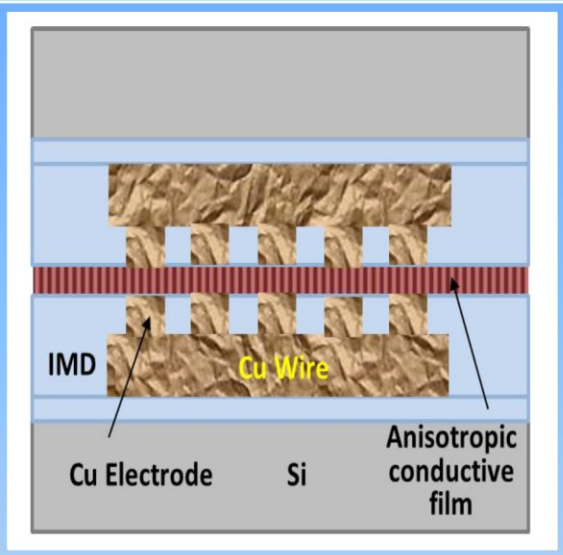
Terascale



** Target Electrode*
- *Size ; 2um, Pitch ; 4um*
- *Density ; ~ Ten millions/die*

** Joining Structure*
- *Electro-less thin Ni/Au layers on extruded Cu electrode*
- *Thin glue layer (below 1umt) w/o flux composition*

Exascale

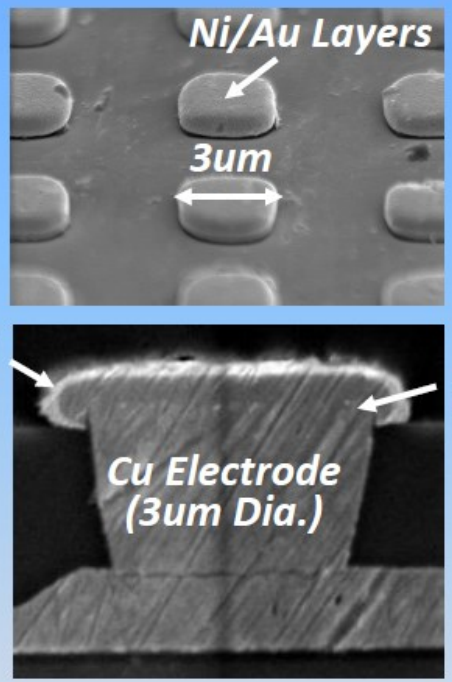


** Target Electrode*
- *Size ; < 1um, Pitch ; < 2um*
- *Density ; > Hundred millions/die*

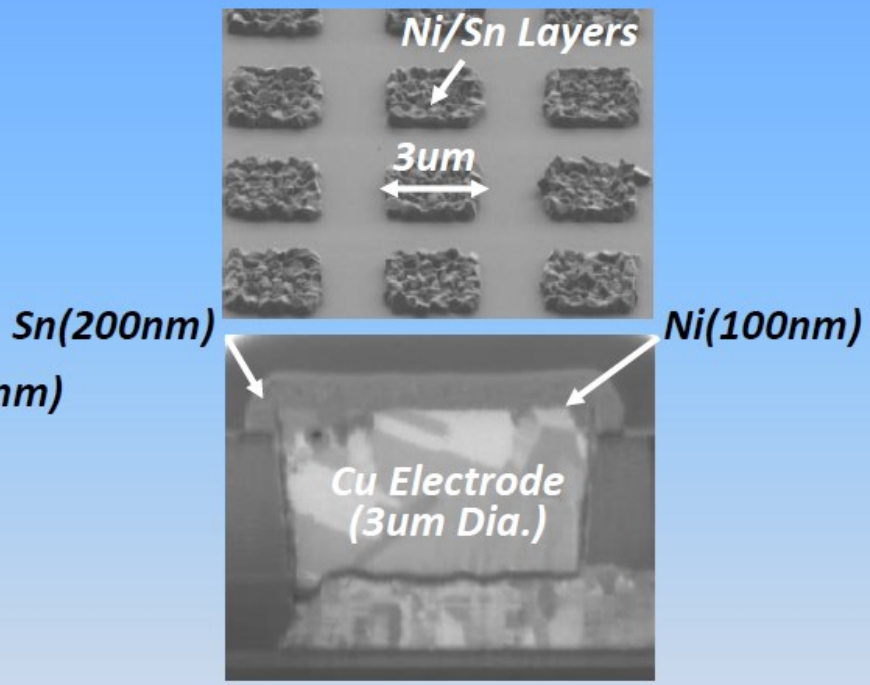
** Joining Structure*
- *Extruded Cu electrode*
- *Anisotropic conductive film compose of ultra-density nano-Cu filaments*

Novel Hybrid Bonding Features for Ultra-High Density 3D/2.5D Integration

- *SEM bird`s view and cross-sectional images of scaled Cu electrodes with thin Ni/Au (a) and Ni/Sn (b) capping layers by electro-less plating*



(a) Case 1

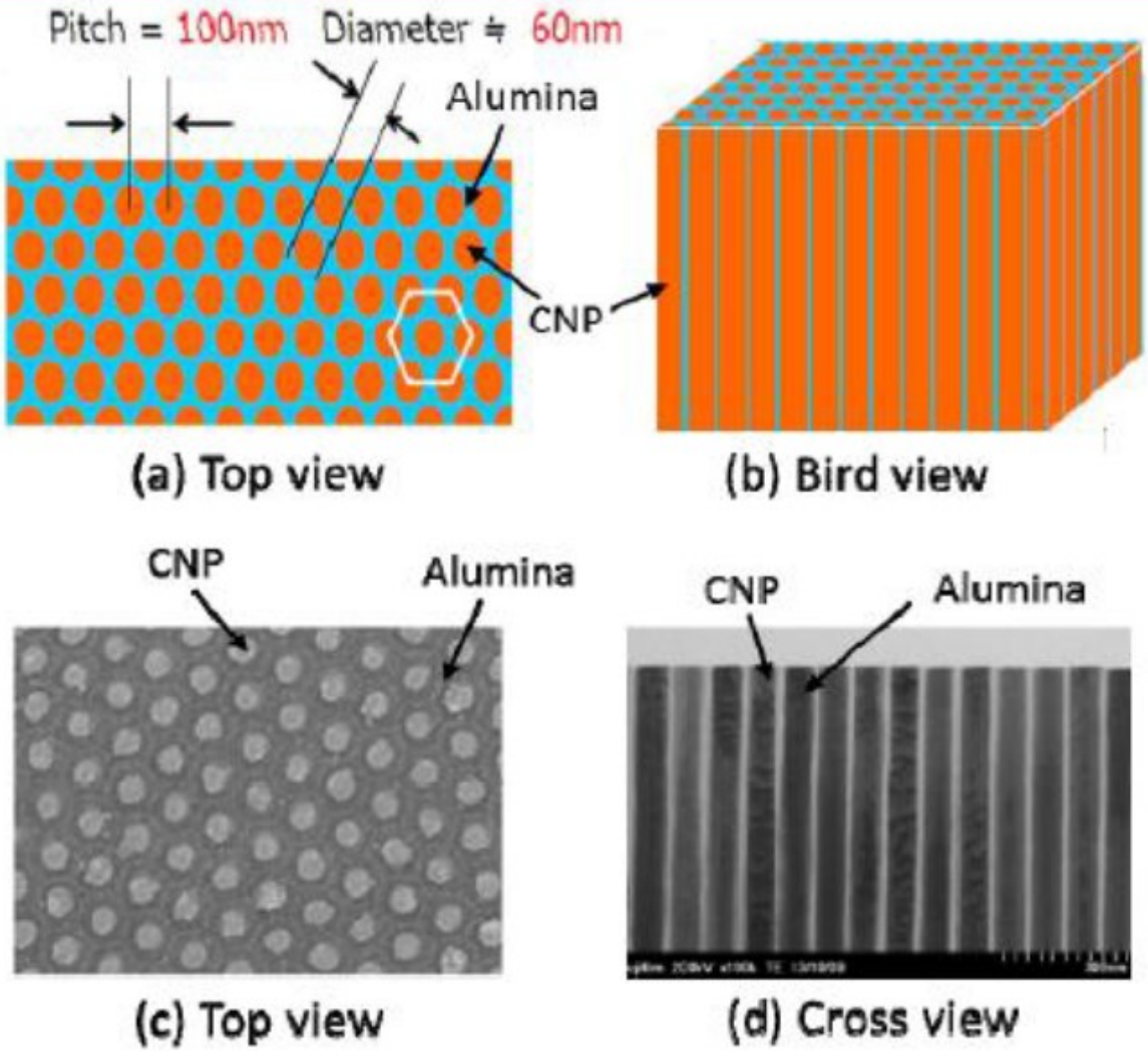


(b) Case2

- *Case (1) ; Au for anti-oxidation layer and Ni for buffer layer to compensate the variation of Cu electrode height and surface topography*
- *Case (2) ; Ni for barrier layer and Sn for buffer layer to compensate the variation of Cu electrode height and surface topography*

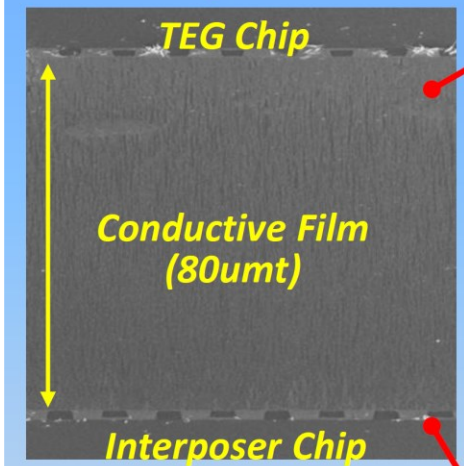
☞ *Require uniform thickness and morphology of electro-less plated capping layers along the wafer as much possible*

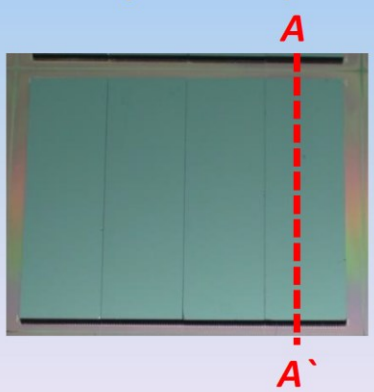
Inorganic Anisotropic Conductive Film

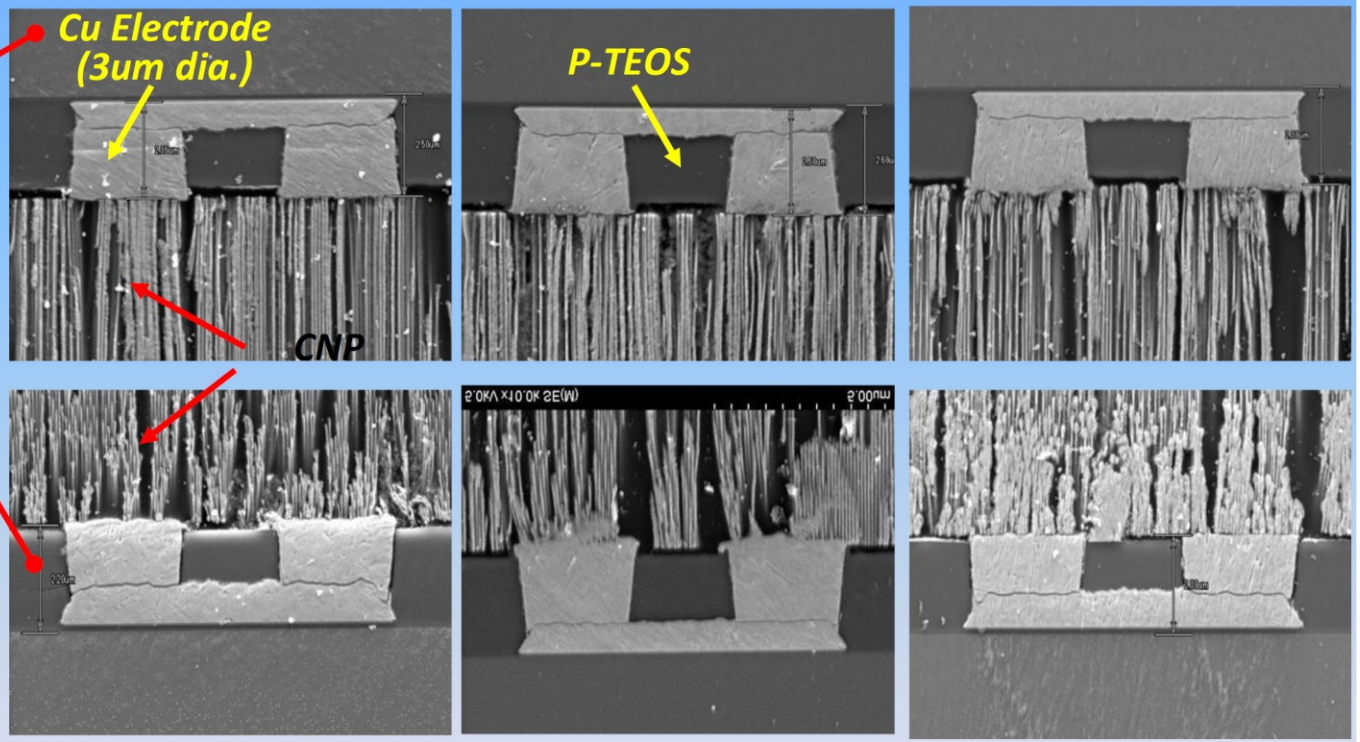


Hybrid Bonding using Cu Nano-Pillar

- *SEM cross-sectional images of fabricated TEG module using ultra-high density CNP*





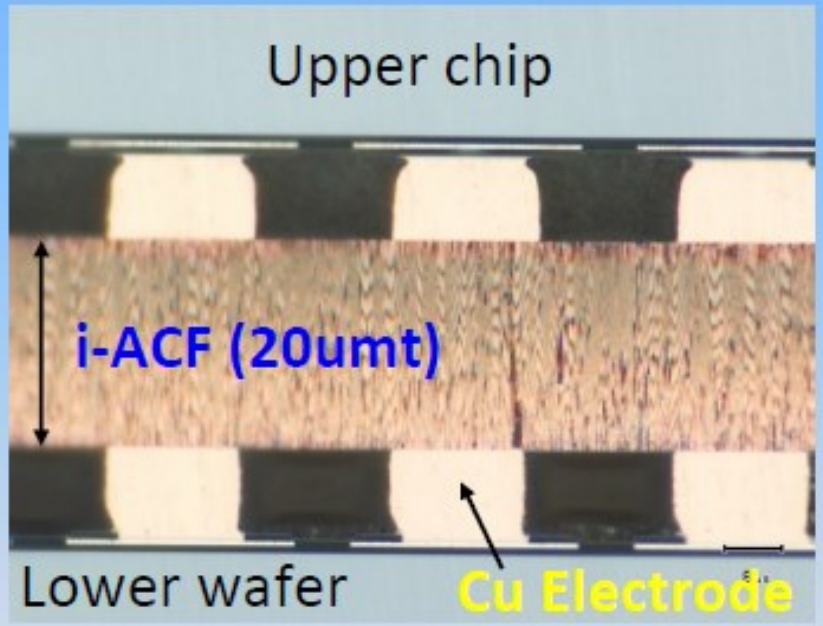


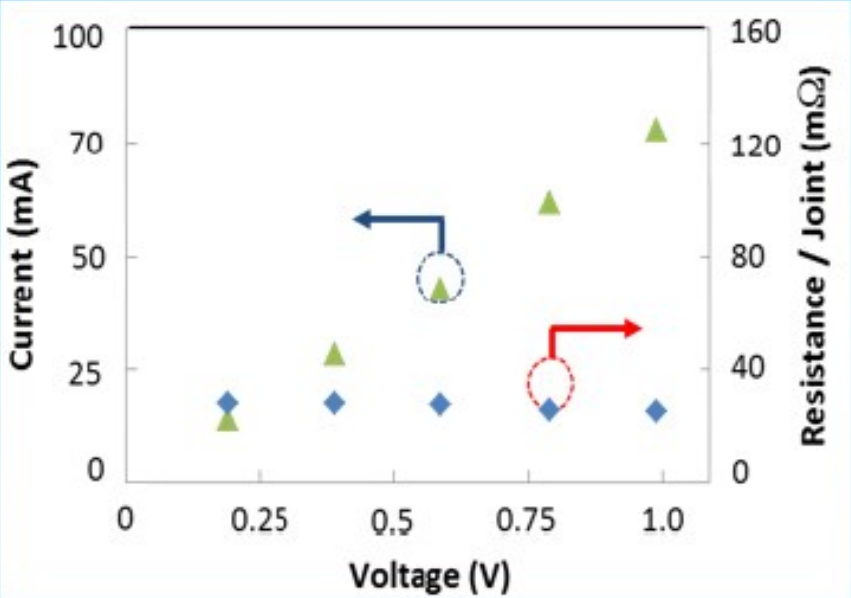
(Top area) (Center area) (Bottom area)

☞ *CNP give good intact bond with high stacking yield by minimizing the impacts of height variation of electrodes along chip/wafer, particles, and residuals on electrode surface*

Hybrid Bonding using Cu Nano-Pillar

- *I-V characteristics measured in the daisy chain bonded using high density CNP (after optimization)*



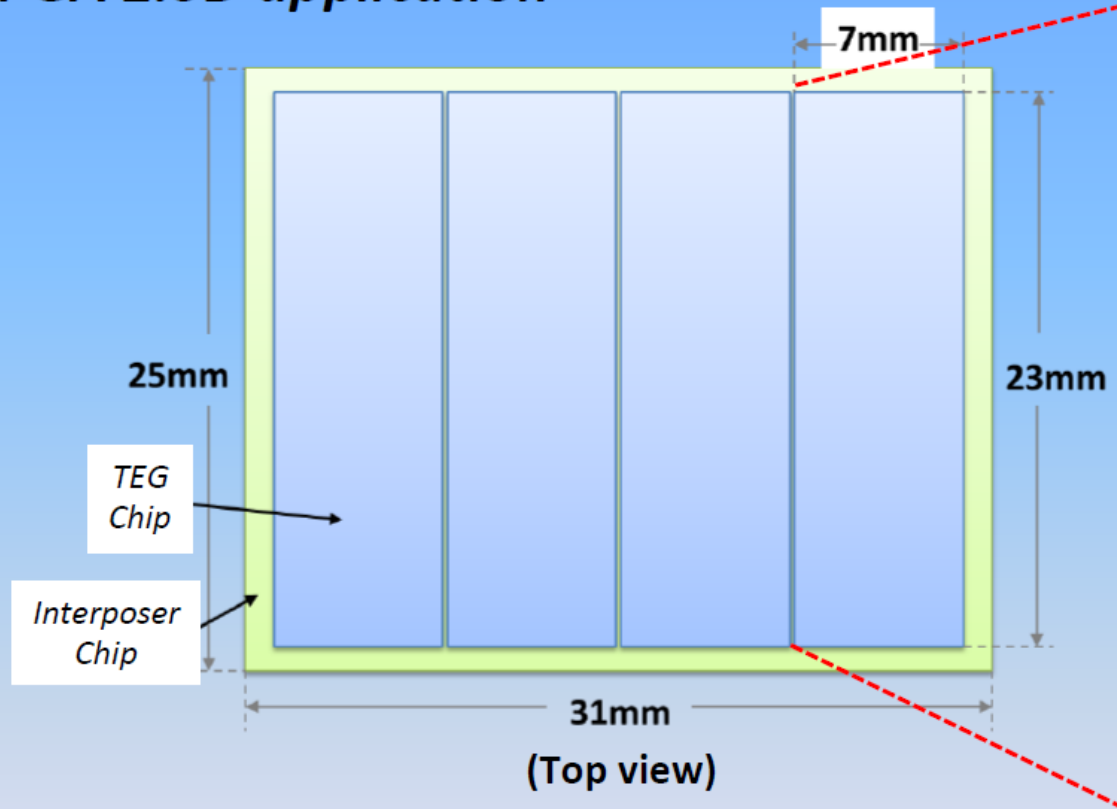


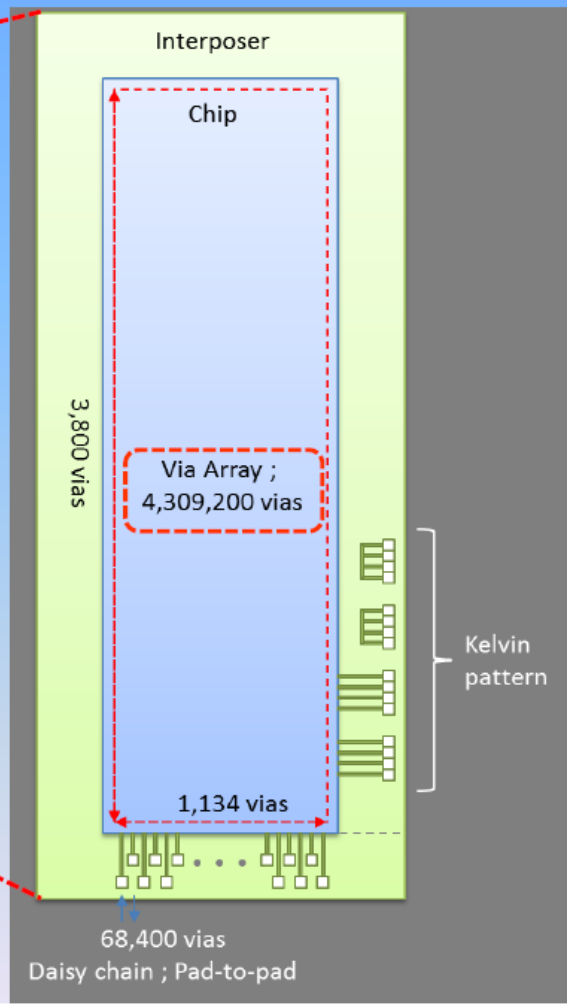
(10μm square Cu electrode is used to minimize the misalignment affect)

- *100% Joining Yield (100K per die)*
- *Joining resistance ; 30 mΩ/Joint (10μm dia. electrode)*

Multi-Chip FPGA TEG Modules

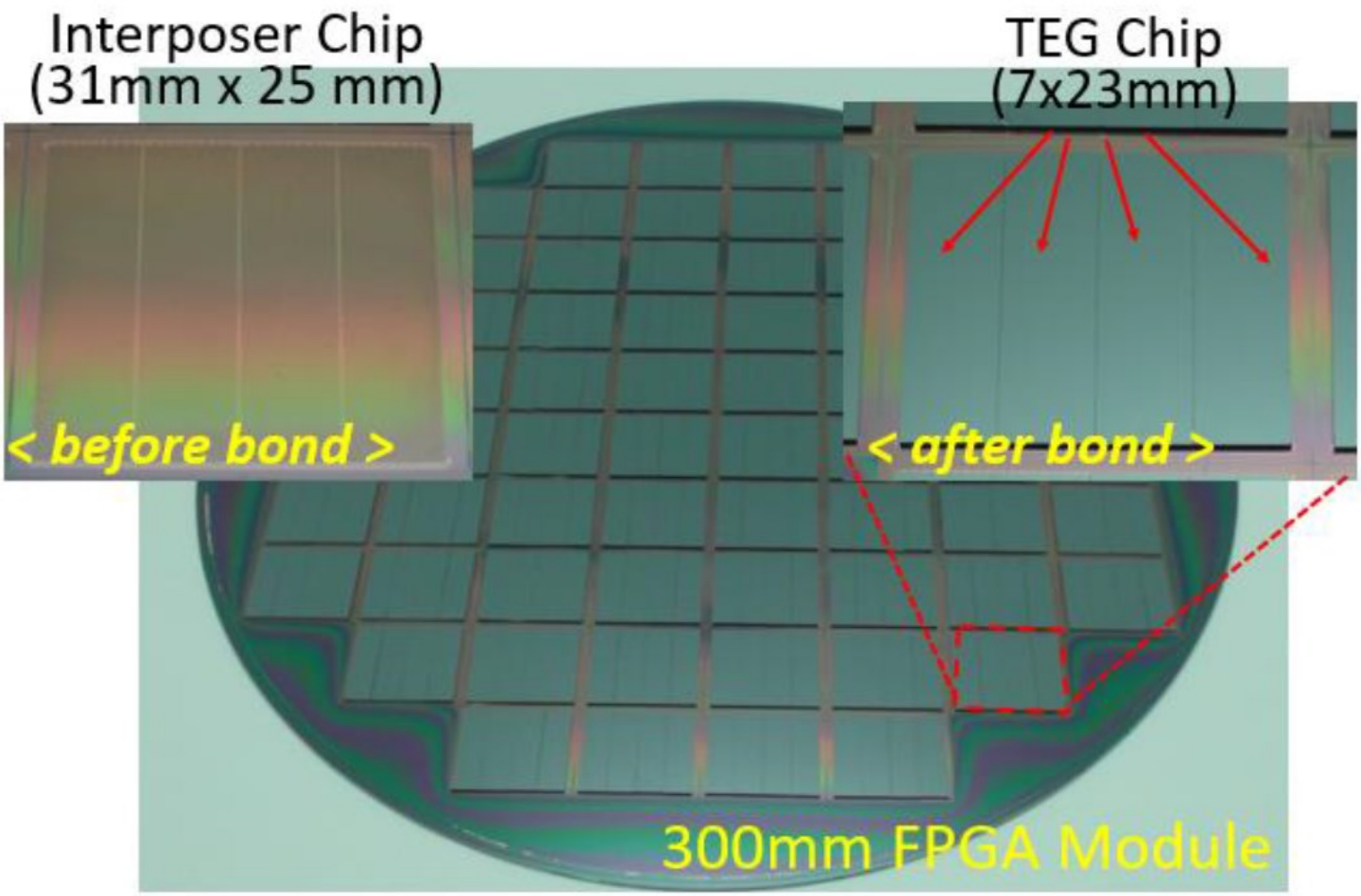
- *The configuration and the specification of TEG module for high-end FPGA 2.5D application*



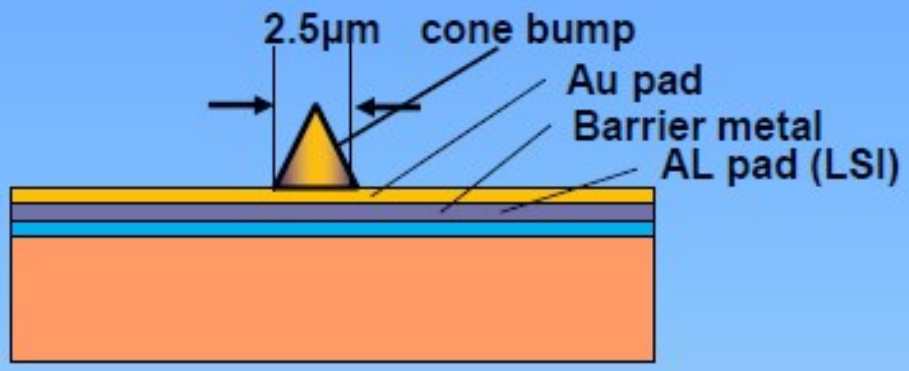


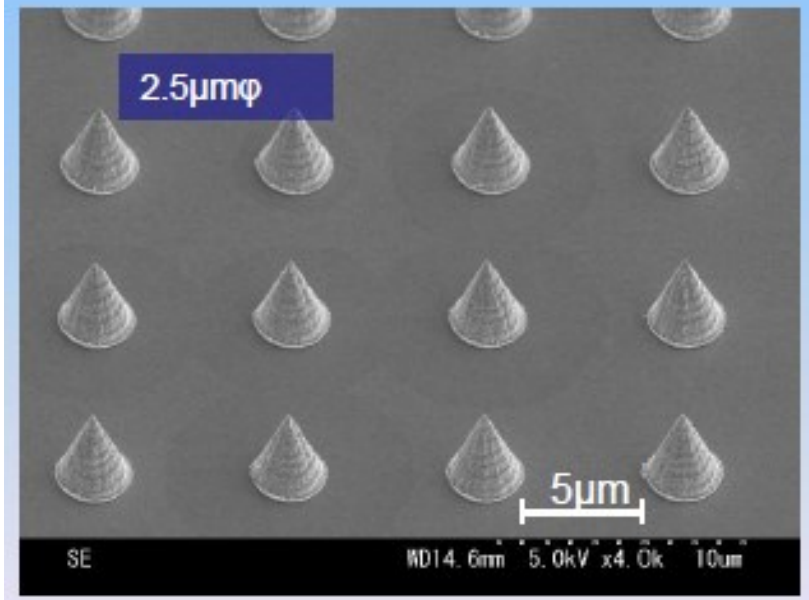
- *Die Size ;*
  - *-. Top TEG die ; 7mm x 23mm*
  - *-. Bottom interposer die ; 31mm x 25mm for 4 dies*

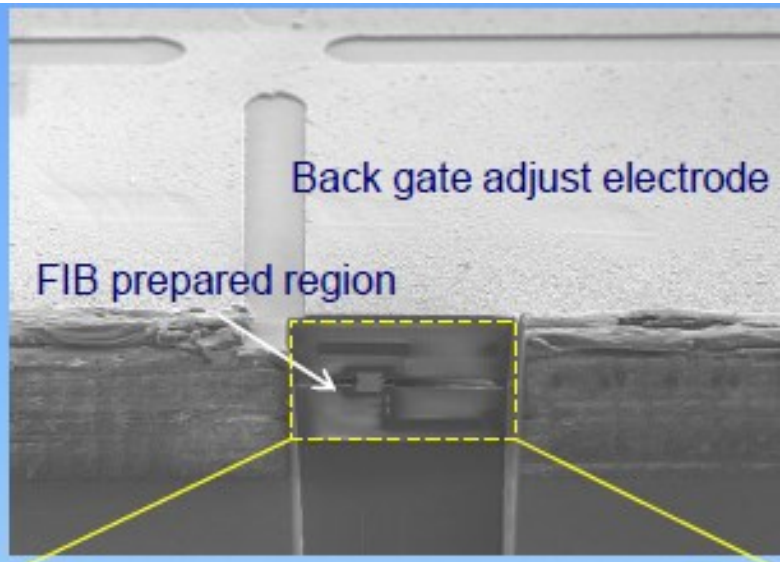
300mm FPGA TEG modules Fabricated by Multichip-to-Wafer 3D Stacking

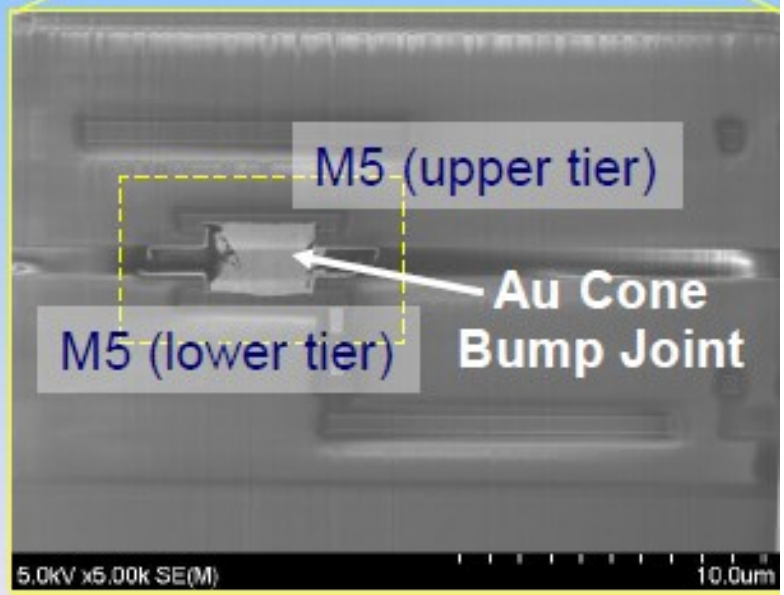


T-Micro Chip-to-chip,Chip-to-Wafer bonding using Au cone bump

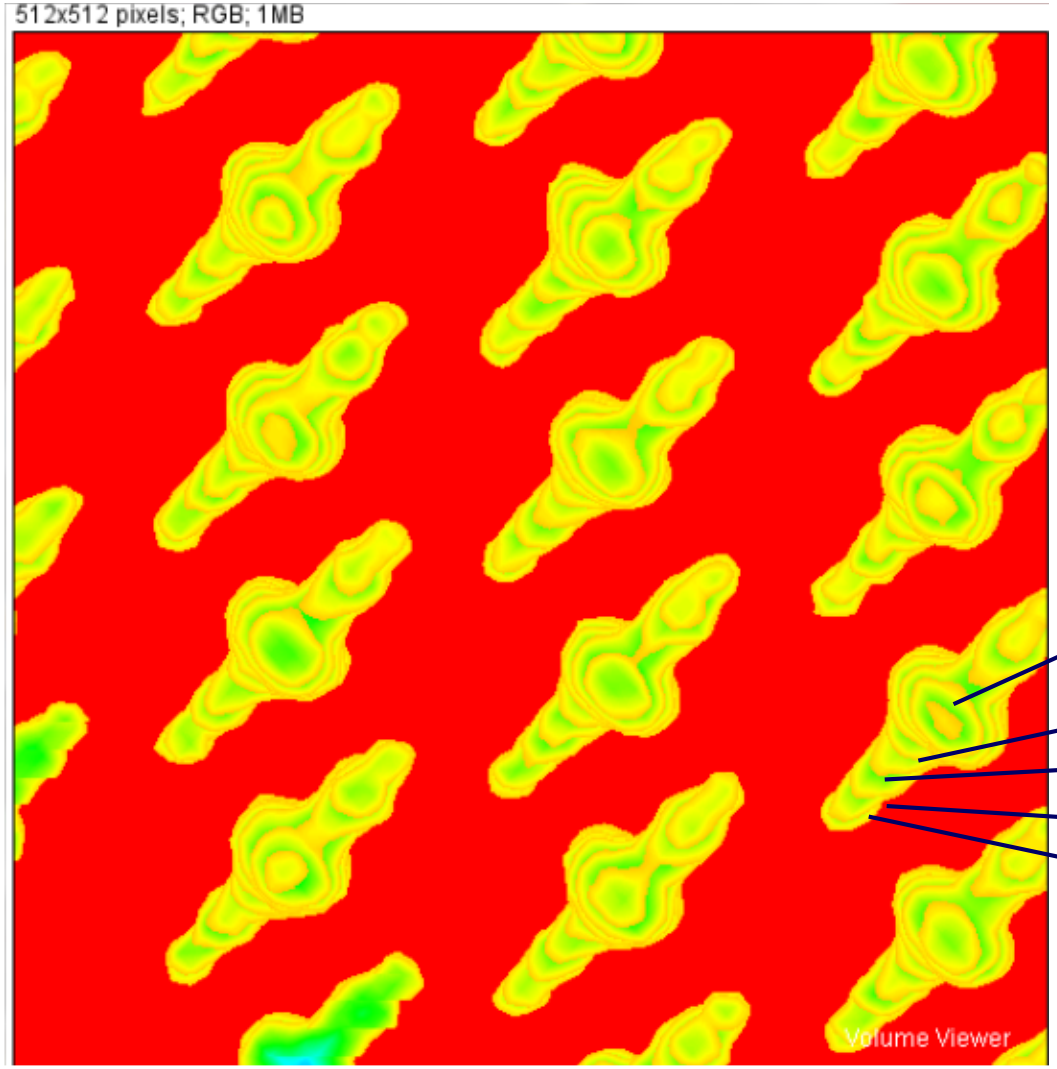


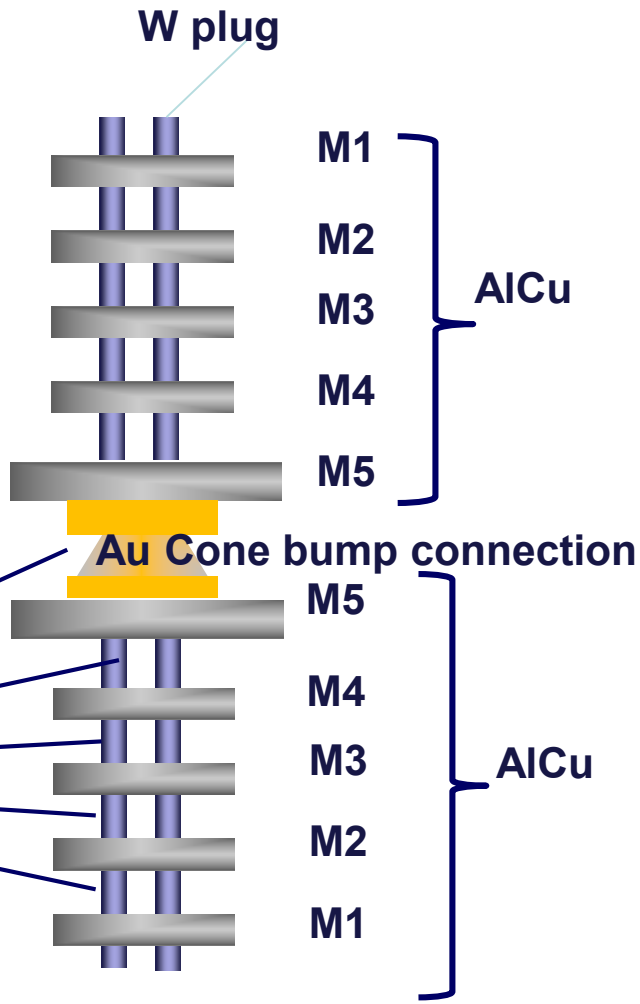






X-ray CT Image

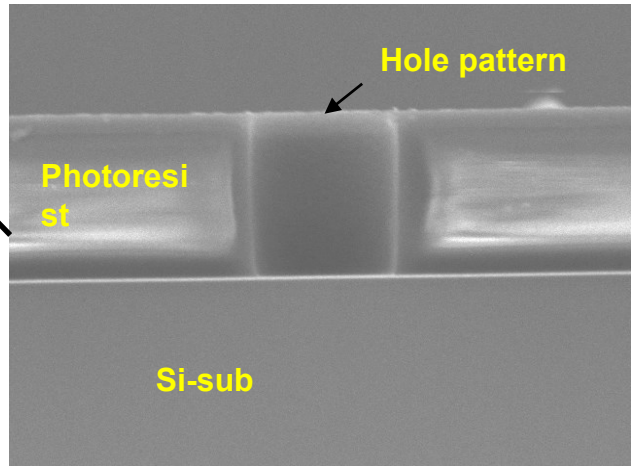




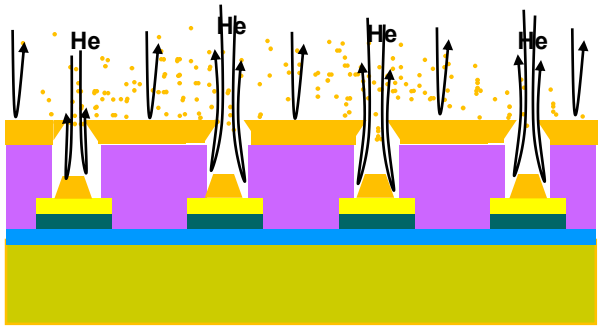
Au Cone bump formation

Au/barrier metal/SiO_2

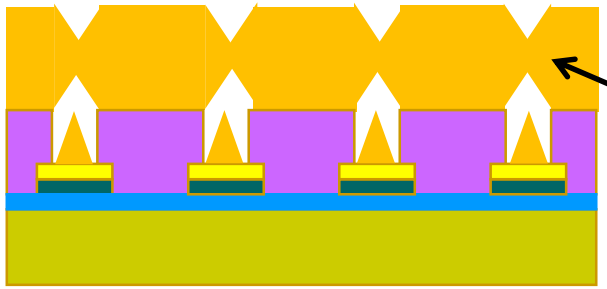
Bump litho.

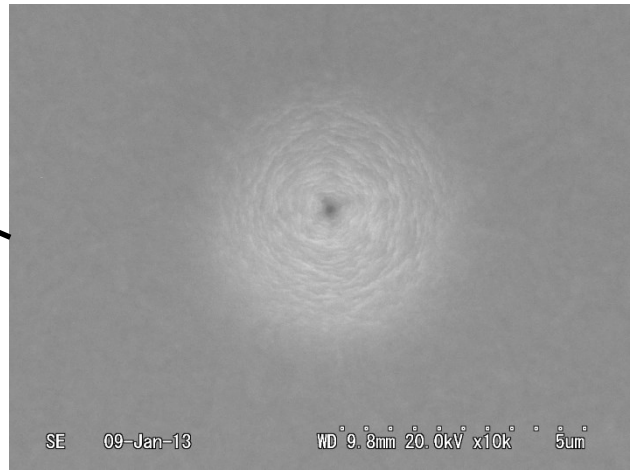


NpD

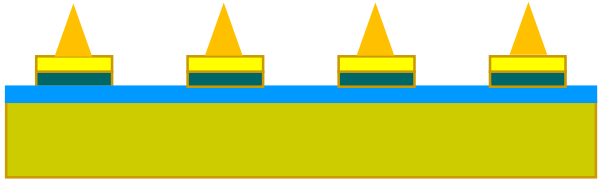


Close bump hole



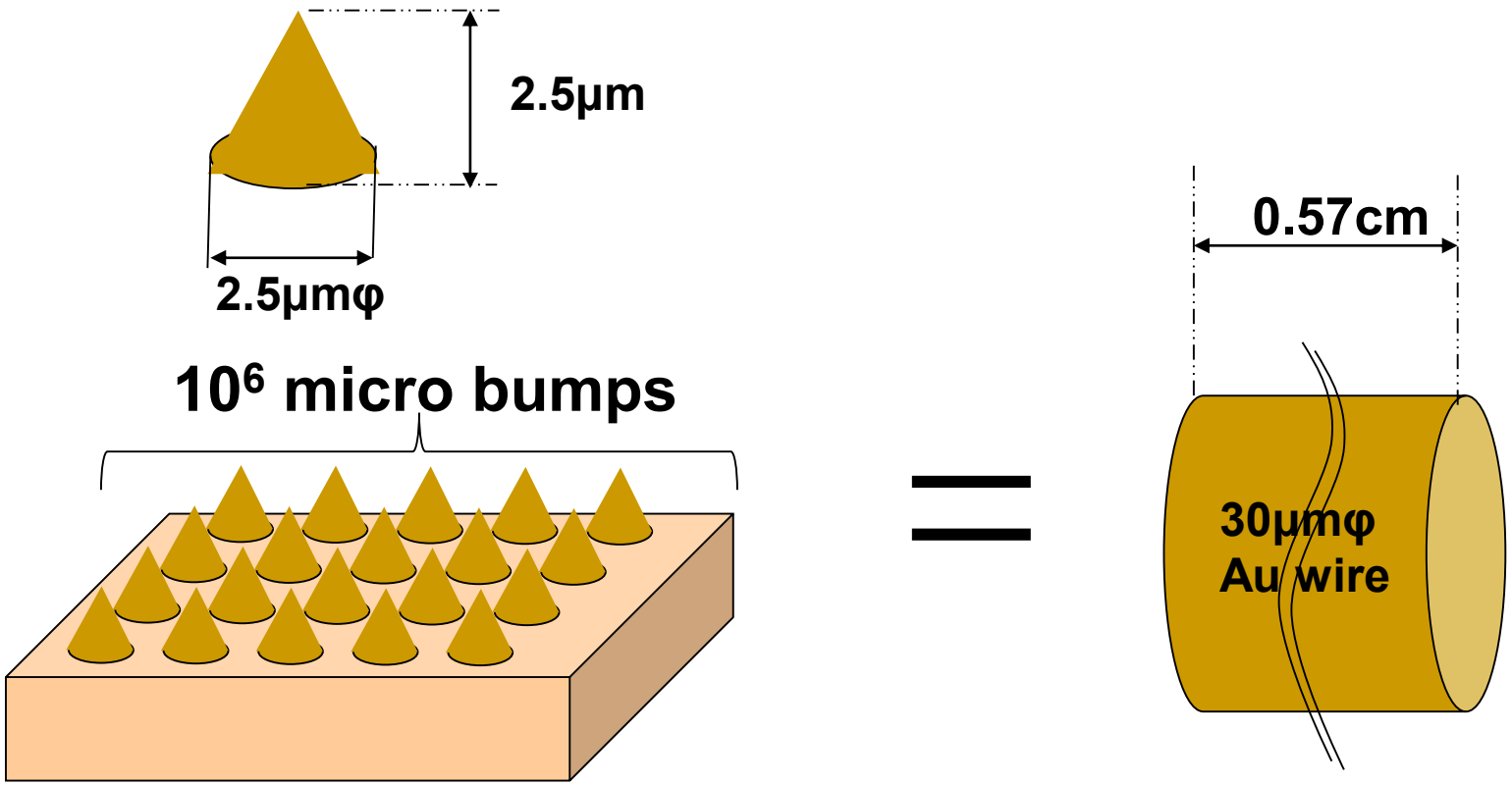


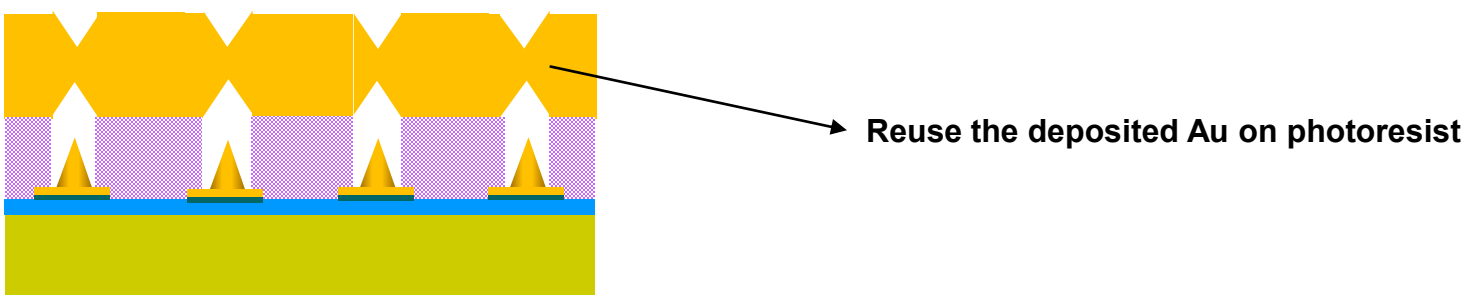
Top view after deposition



After resist lift-off

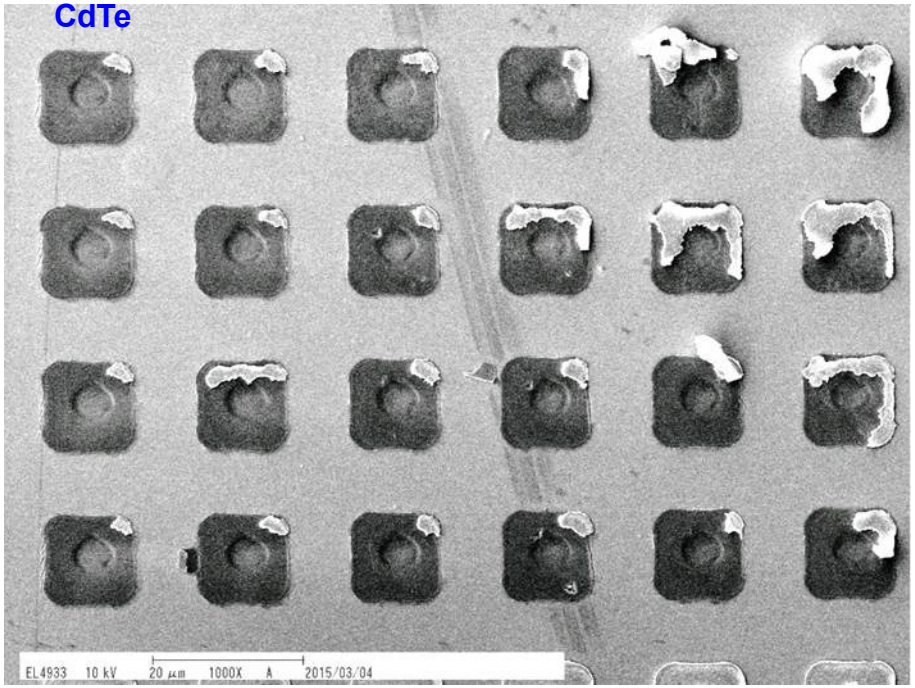
Material cost of Au bump

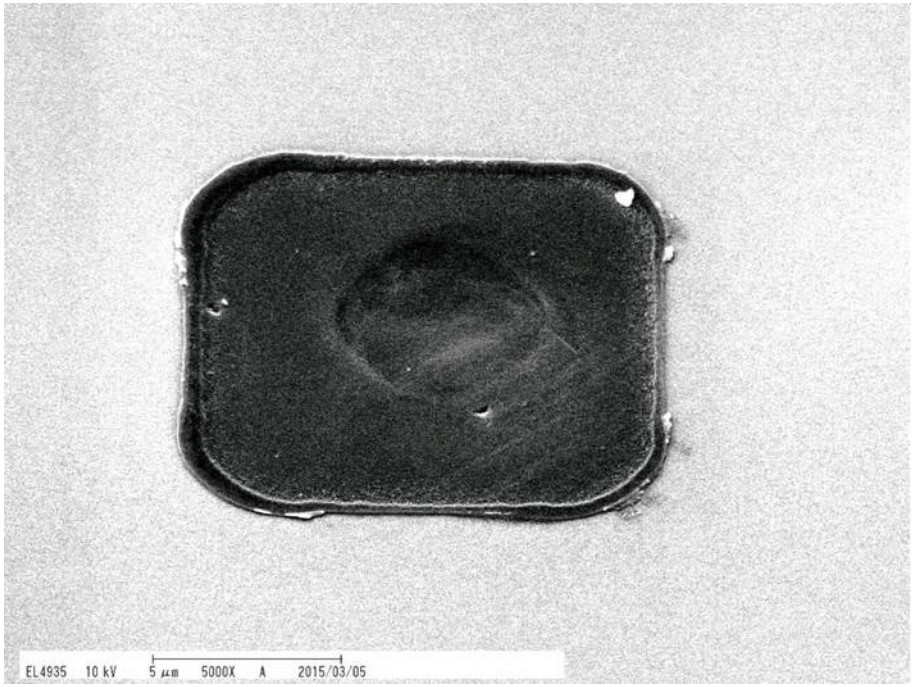




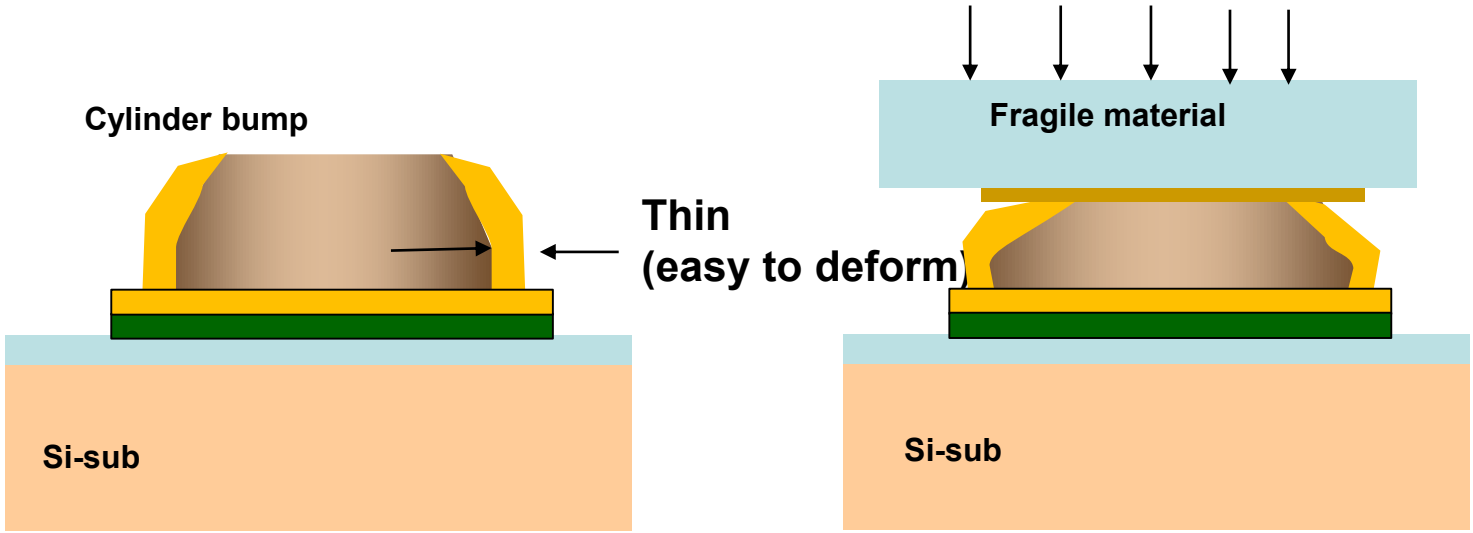
Cylinder Bump for fragile material

CdTe surface after CdTe/Si-ROIC bonding with Au bump



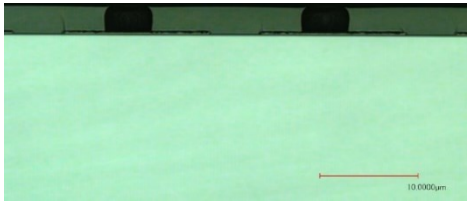


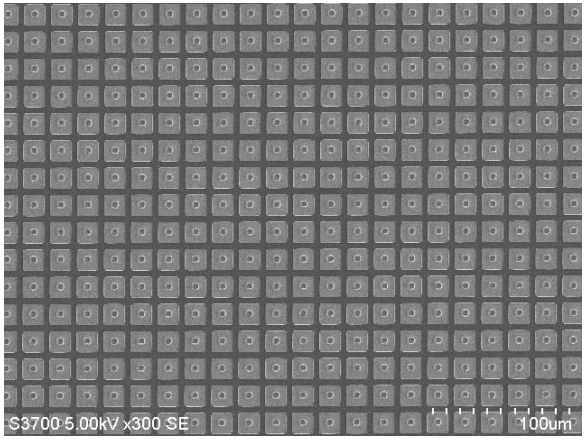
Bump bonding with cylinder Au bumps



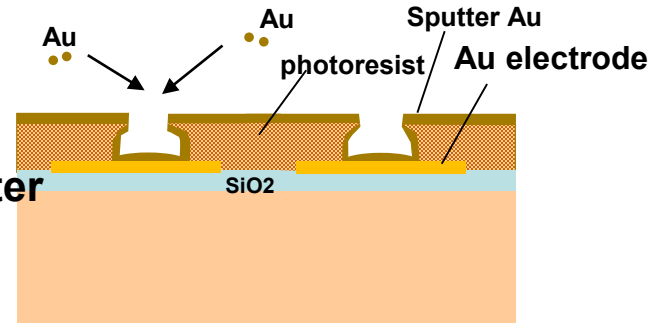
Bump bonding with cylinder Au bumps

Bump hole patterning

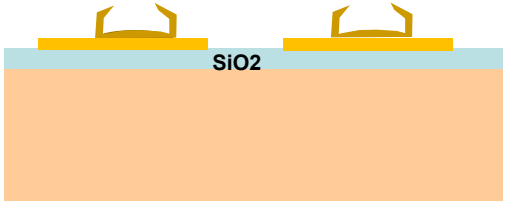


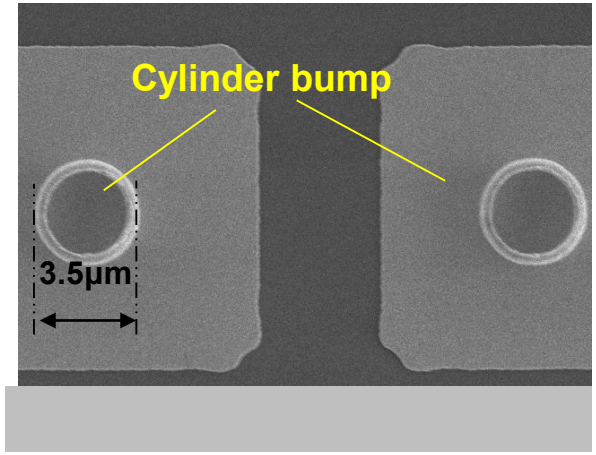


Short Throw（SL)Au spatter

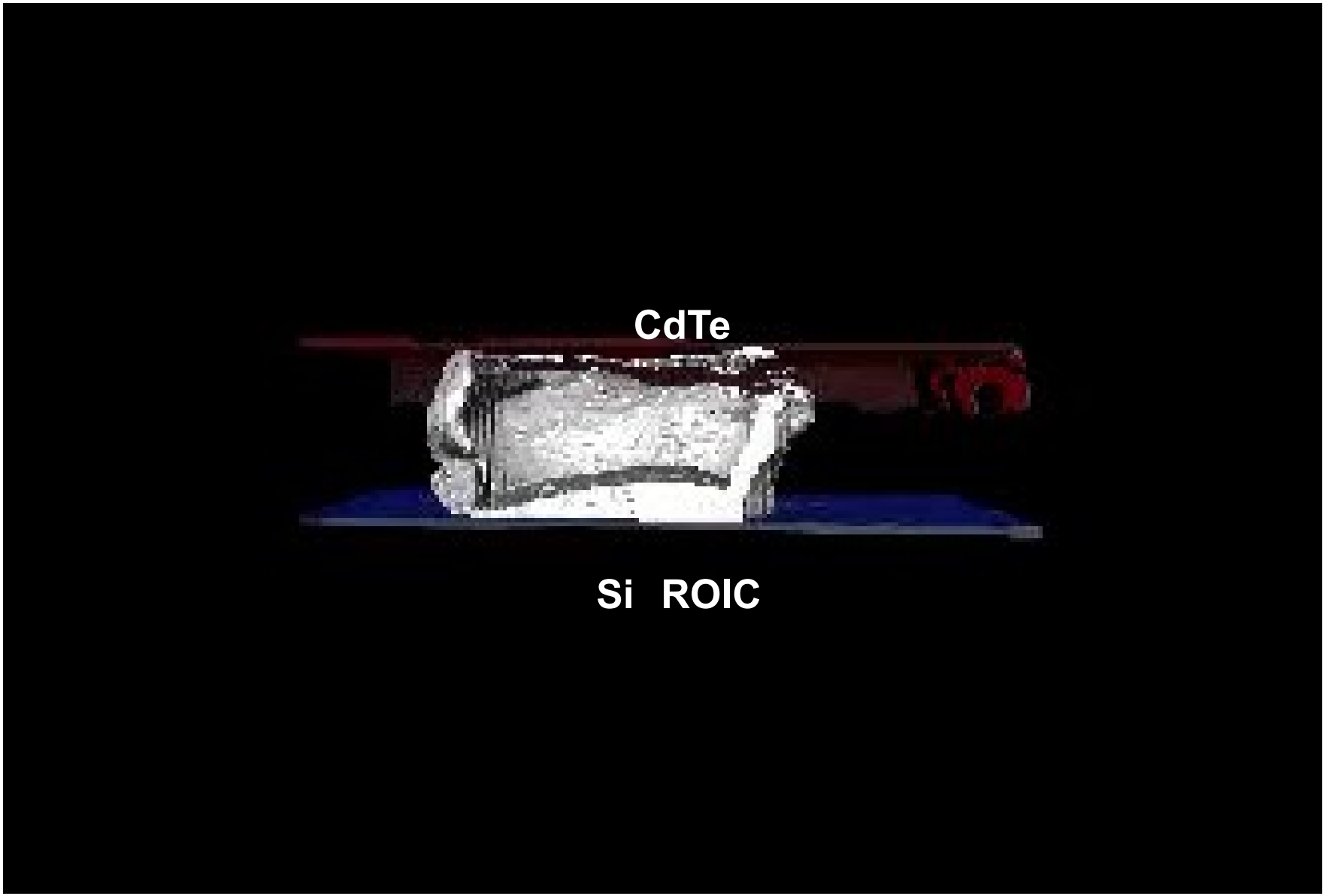


after photoresist lift-off





SEM cross sectional view



Process cost reduction for the Heterogeneous Integration

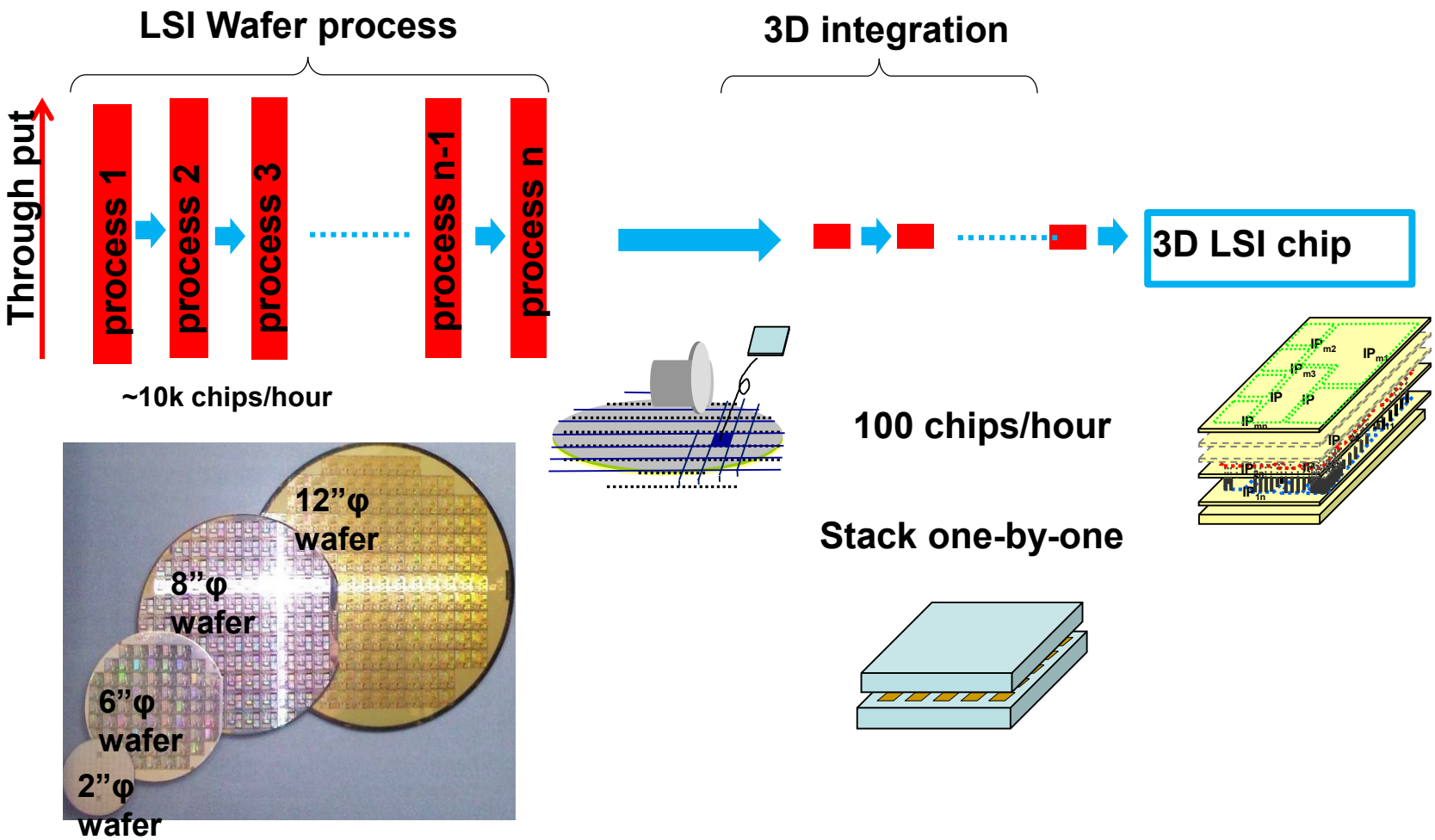
3D stack approaches

	CtC (chip to chip)	CtW (chip to wafer)	WtW (wafer to wafer)
	stack	dicing	dicing
Process cost	High	High ~ Middle	Low
Stack chips with different chip size	possible	possible	Impossible
Chip alignment accuracy <0.5μm (3σ)	Difficult from economical stand point		possible ?
Miscellaneous			Need high yield wafers $Y_{total}=Y_{W\#1} \times \cdots \times Y_{W\#n}$ Need same size wafers

Need a high speed COW technique with the high alignment accuracy and the practical process cost

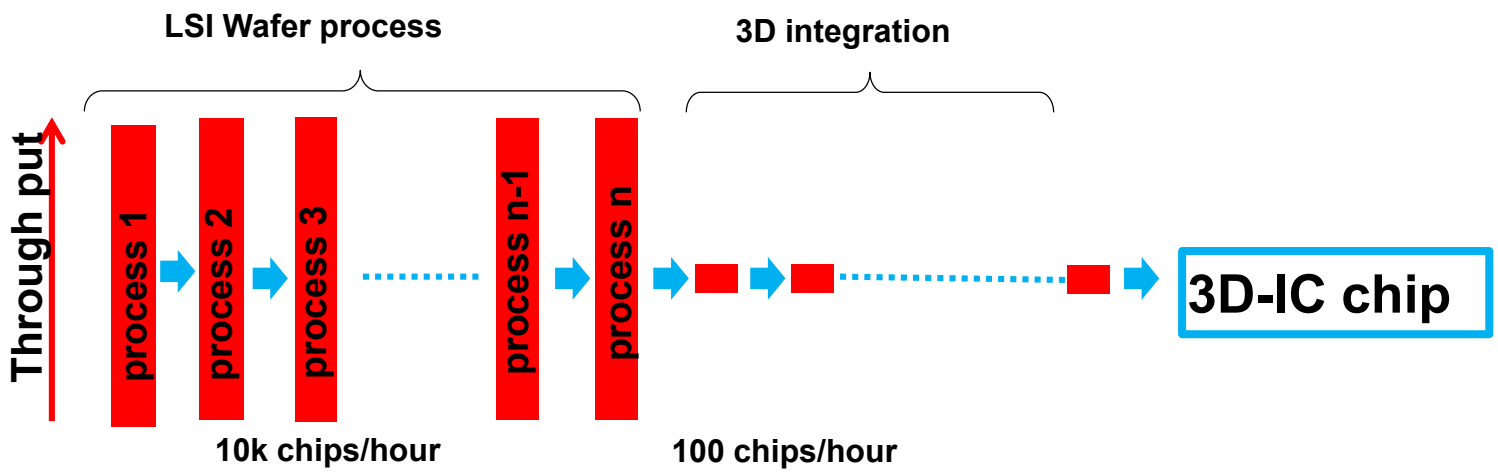
Economy of 3D LSI manufacturing

(a) Current 3D Production

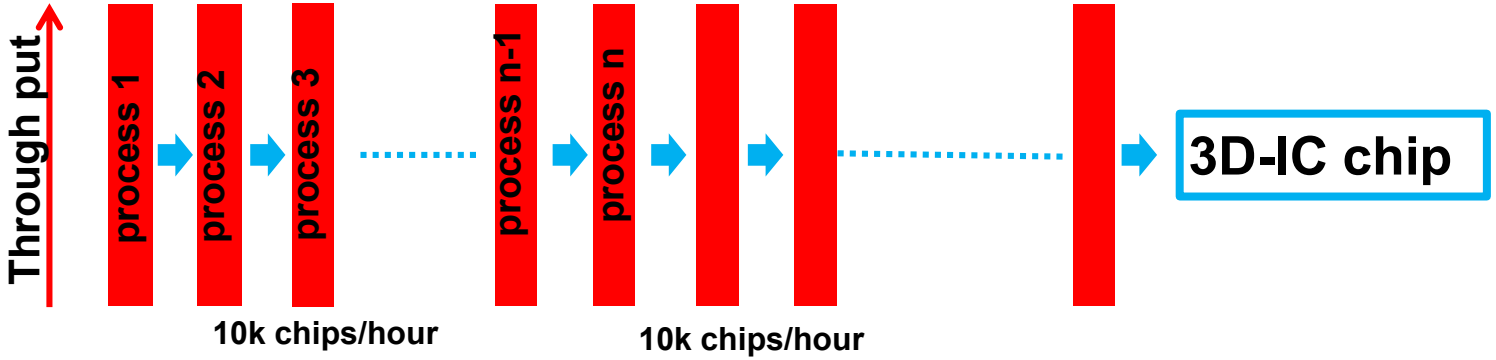


Economy of 3D LSI manufacturing

(a) Current 3D Production

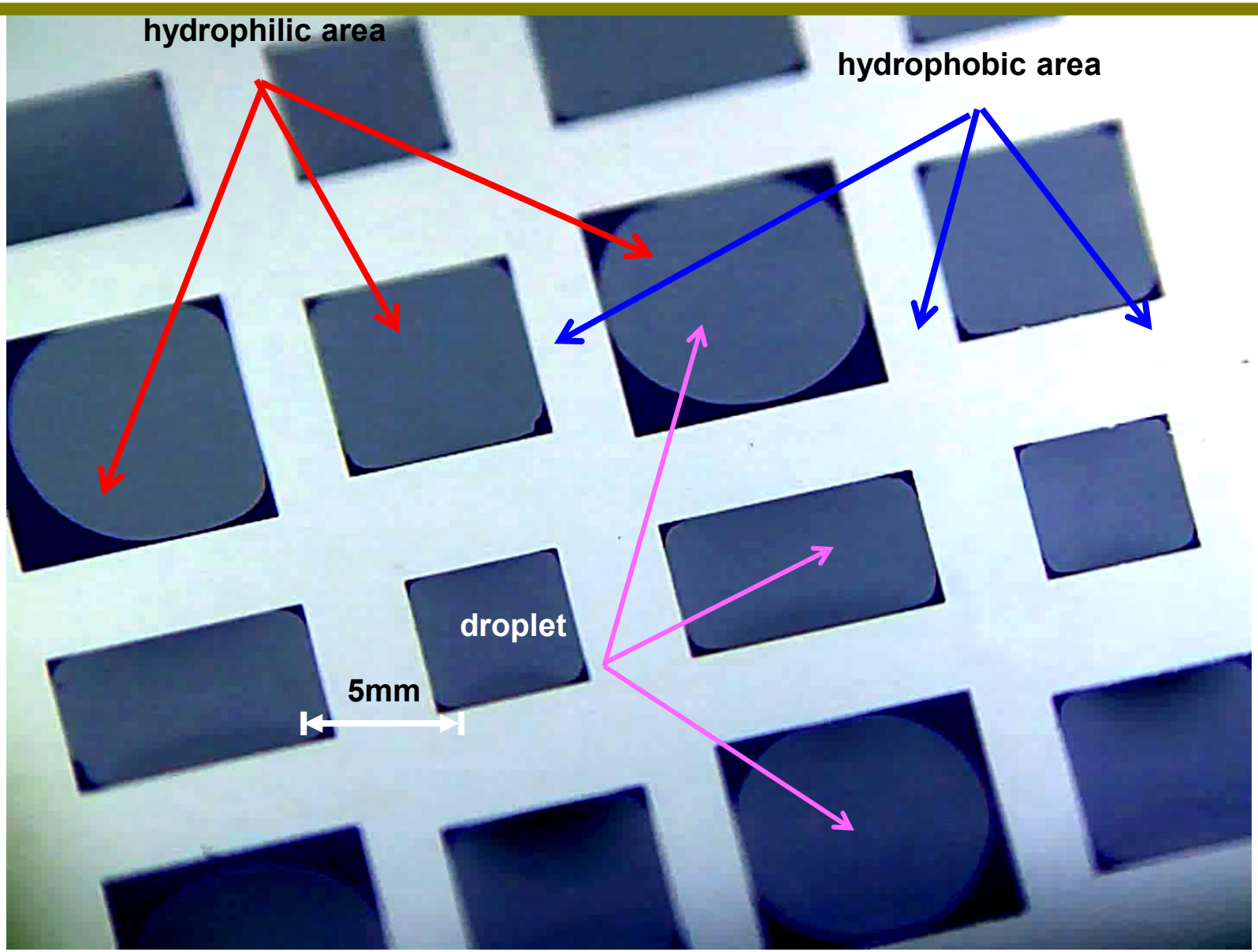


(b) Our Target

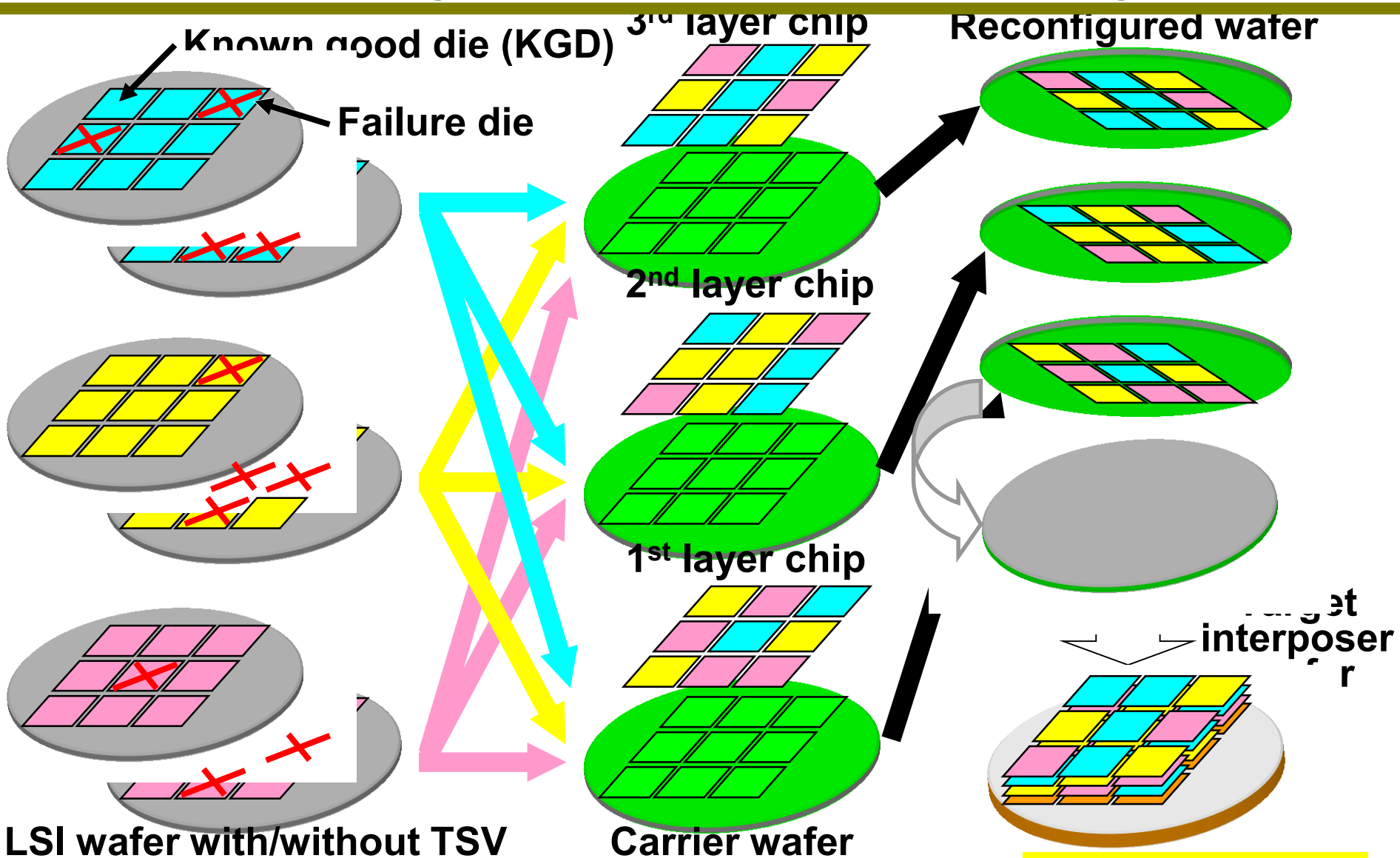


“Super Chip”
Self-assembly Technique

Self-assembly technique

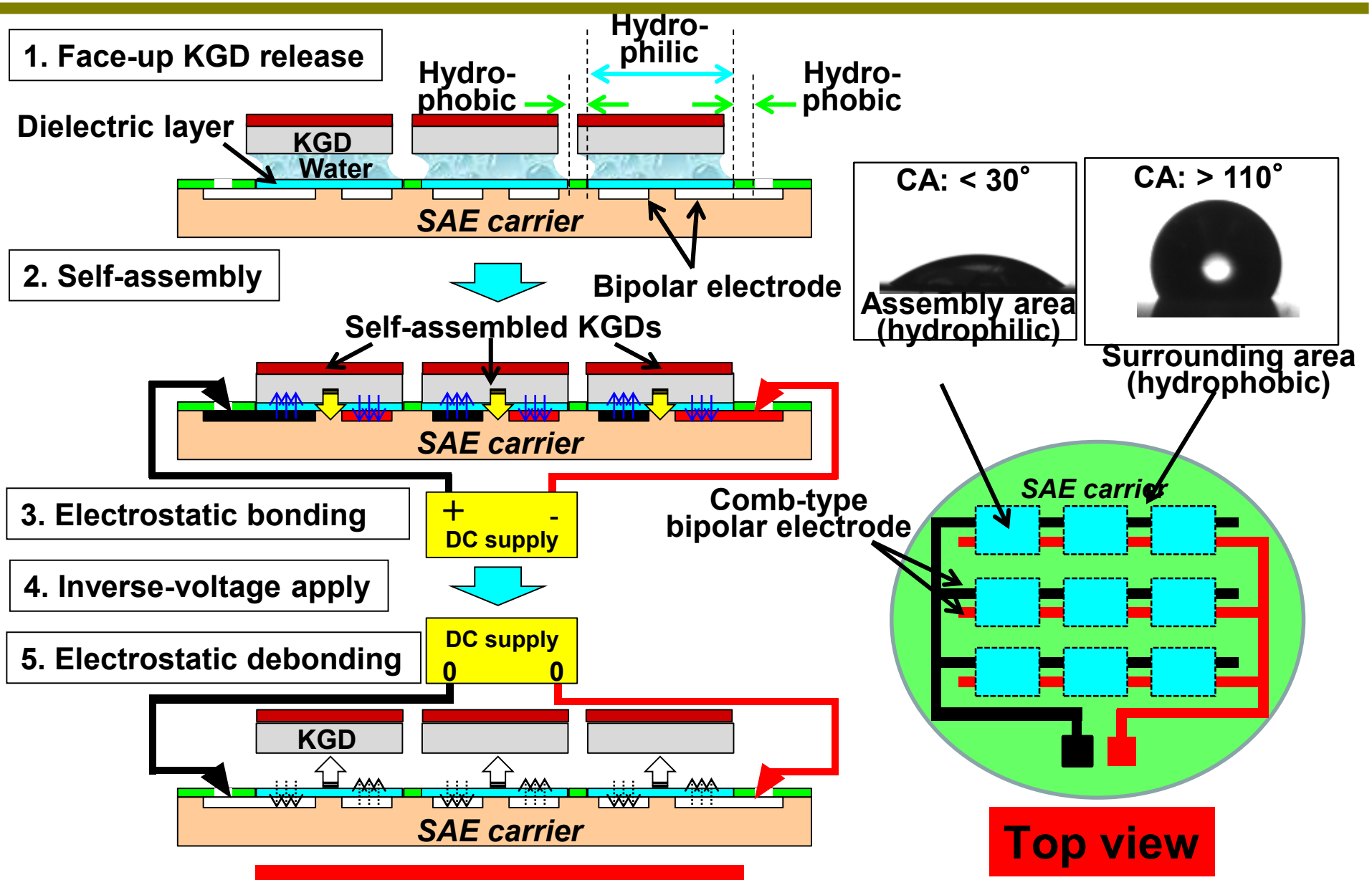


New Reconfigured Wafer-to-Wafer 3D Integration



3D super chip

Self-Assembly & Electrostatic (SAE) Bonding



Thank you for your kind attention.

If there's anything you are unclear on, please feel free to contact me. motoyoshi@t-microtec.com