Status and roadmap of hybridization technologies relevant to future pixel detectors

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3D-IC Technology ≠ LSI Technology

- unpredictable
  Application driven technology
- Need flexibility
  System technology
  Many integration methods

- Predictable
- Precise but inflexible
3DIC Supply chain

Base devices

- 4 inch Si wafer
- 6 inch Si wafer
- 8 inch Si wafer
- 12 inch Si wafer
- Shuttle service (LSI Chip)
- Compound Semiconductor (Chip/Wafer)

3D integration
Unique Points of 3D-LSI

Conventional SoC

- Long Global interconnect → large RC delay, large $C_P$
- Compound semiconductor
- Sync. clock

3D-SoC

- Short global interconnect → small RC delay, small $C_P$
- High band width
- Small form factor

- Repartitioning Die
- Length of TSV: 1-50μm

1. Increase of electrical performances
2. Increase of circuit density
3. New Architecture (Hyper-parallel processing, Multifunction, etc)
4. Heterogeneous integration
5. Better yield

TSV: Through Silicon Via
Semiconductor Market Forecast


- 3D-IC
- MEMS device
- DRAM, Flash
- Sensor / Detector

CAGR: 4%
Chip & System Integration Trends for better PPA & System Performance

Source: Cliff Hou (TSMC), ISSCC 2017 (Plenary)
Key technologies of 3D-IC Integration

- Wafer thinning: 775μm → 50~10μm
- Chip Alignment
- Micro bump
- TSV (Through Silicon Via)
- Pch-MOSFET
- Nch-MOSFET
- Over coat
- Top tier
- Middle tier
- Bottom tier
- Si Substrate
- NWELL
- PWell
- Pch-MOSFET
- Nch-MOSFET
- SiO2
- Over coat
- Metal
- P+ - MOSFET
- N+ - MOSFET
- Satisfy LSI reliability test

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TSV process classification

- **Before MOS**: Well Isolation
- **After MOS**: MOS, Interlayer
- **After 1st Interlayer**: FEOL
- **After BEOL**: BEOL
- **Front Via**: After BEOL
- **Back Via**: Handle Wafer
- **SOI**: Handle glass
- **Stacking**: Handle Wafer

Max. process temperature:
- 1000°C > Well Isolation
- 600°C > FEOL
- 450~350°C > BEOL

Allowable max. process temperature: 1000°C

TSV step:
- Via First
- Via Middle
- Via Last

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Wafer Bonding Methods -1

Adhesive Bonding

Oxide Fusion Bonding

Metal (Cu) Fusion Bonding
Metal (Cu/SnAg) Eutectic Bonding
Wafer Bonding Methods -2

Adhesive/ Metal Bonding

Oxide/ Metal Bonding (Hybrid bonding)
<table>
<thead>
<tr>
<th>Type</th>
<th>TSV</th>
<th>Processing</th>
<th>Layer stacking</th>
<th>Application</th>
<th>Present</th>
<th>Future</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hybrid 3D</td>
<td>TSV</td>
<td>Wafer level</td>
<td>Bonding</td>
<td>Image Sensor</td>
<td>Image Sensor DRAM</td>
<td>DRAM FPGA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Chip level</td>
<td>Bonding</td>
<td>DRAM FPGA</td>
<td></td>
<td>MEMs/Sensor Analog IC</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Wafer + Chip</td>
<td>Bonding</td>
<td>Image Sensor</td>
<td>Image Sensor DRAM Processor</td>
<td></td>
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<tr>
<td>Non-TSV</td>
<td></td>
<td>Wafer level</td>
<td>Bonding</td>
<td>Image Sensor (BSI)</td>
<td>Image Sensor Logic/SoC</td>
<td></td>
</tr>
<tr>
<td>Monolithic 3D</td>
<td>Non-TSV</td>
<td>Wafer level</td>
<td>Depo or Epi</td>
<td>NAND-Flash</td>
<td>NAND-Flash Logic/SoC</td>
<td></td>
</tr>
<tr>
<td>Monolithic + Hybrid</td>
<td>Non-TSV + TSV</td>
<td>Wafer level</td>
<td>Mixed</td>
<td>Image Sensor</td>
<td>NAND-Flash Logic/Memory</td>
<td></td>
</tr>
</tbody>
</table>

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HBM (High Band Width Memory)

Commercialized 3D DRAM

Source: Kyomin Sohn (Samsung), ISSCC2016
Cross-sectional View and Chip Photo of HBM

- Process: 20nm DRAM
- Capacity: 9Gb/core die
- Supply voltage: 1.2V/1.2V/2.5V
- Chip size: 12mm x 8mm (buffer die)

Source: Kyomin Sohn (Samsung), ISSCC2016
### Comparison table of GDDR5 and HBM Gen1.2

<table>
<thead>
<tr>
<th>Items</th>
<th>GDDR5</th>
<th>HBM Gen1</th>
<th>HBM Gen2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pin Data Rate</td>
<td>4~8Gbps</td>
<td>1Gbps</td>
<td>2Gbps</td>
</tr>
<tr>
<td># of IO and CH</td>
<td>1CH, 32 IO</td>
<td>8CH, 128IO/CH</td>
<td>16pCH, 64IO/pCH</td>
</tr>
<tr>
<td>Bandwidth</td>
<td>16~32GB/s</td>
<td>128GB/s</td>
<td>256GB/s</td>
</tr>
<tr>
<td>Voltage (VDDC/VDDQ/VPPE)</td>
<td>1.35V~1.5V</td>
<td>1.2V/1.2V/2.5V</td>
<td>←</td>
</tr>
<tr>
<td>Interface</td>
<td>POD (VDDQ Term.)</td>
<td>CMOS (Un-term)</td>
<td>←</td>
</tr>
<tr>
<td>Banks</td>
<td>4banks/BG, 4BGs</td>
<td>←</td>
<td>←</td>
</tr>
<tr>
<td>Implemented new functions in this work</td>
<td>←</td>
<td>Pseudo channel, 2H/4H/8H, ECC storage, Implicit pre-charge, Lane remapping, ...</td>
<td></td>
</tr>
</tbody>
</table>

Source: Kyomin Sohn (Samsung), ISSCC2016
Sony / 3D-Stacked Image Sensor

Sony's first CIS module (IMX260) product with Cu-Cu Hybrid bonding

Cu-Cu Via
3um wide
14um pitch

Top part BI-CIS

Middle part DRAM

Bottom part Logic

Source: Chipworks, April, 2016

Source: T. Haruta (Sony) ISSCC2017

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High Density Memory Systems using Si Interposer
AMD reveals HBM-powered Radeon Fury graphics cards, new R300-series GPUs

Fury graphics card: $649, June, 2015

Memory Interface; 4096bit
Memory Bandwidth; 512GB/s
Highly Integrated Heterogeneous 3D Integrated System

New chip stacking technologies are required

3D Super Chip
- MEMS chip
- Sensor chip
- CMOS RF-IC
- MMIC
- Power IC
- Control IC
- Logic LSI
- Flash memory
- DRAM
- SRAM
- Microprocessor

Different materials
Different devices
Different chip size

Metal microbump
Through-Si via (TSV)

38-layer chip stack

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Fine Pitch TSV

1995-2000
Via first (poly Si-TSV)
Φ2.5mm L: 55μm AR: 22

2001
Via middle (W-TSV)
Φ0.7μm L: 18μm AR: 25

2006~
Via last / Via middle (Cu-TSV)
Φ3μm L: 30μm AR: 10

By electroplating
By Plating
EL-seed
Φ2μm L: 24μm AR: 12

O3-TEOS liner
PVD-seed
Φ5μm L: 30μm AR: 10

Pi liner
Φ5μm L: 85μm AR: 17

PVD-seed

By CVD

55μm 2.5μm 0.7μm
18μm
Novel Hybrid Bonding Features for Ultra-High Density 3D/2.5D Integration

**Gigascale**
- Target Electrode: Size; 3um, Pitch; 6um
- Density; ~ million/die
- Joining Structure: Electro-less thin Ni/Sn layers on extruded Cu electrode
- Thin glue layer (below 1umt) containing flux composition

**Terascale**
- Target Electrode: Size; 2um, Pitch; 4um
- Density; ~ Ten millions/die
- Joining Structure: Electro-less thin Ni/Au layers on extruded Cu electrode
- Thin glue layer (below 1umt) w/o flux composition

**Exascale**
- Target Electrode: Size; < 1um, Pitch; < 2um
- Density; > Hundred millions/die
- Joining Structure: Extruded Cu electrode
- Anisotropic conductive film compose of ultra-density nano-Cu filaments
Novel Hybrid Bonding Features for Ultra-High Density 3D/2.5D Integration

Case (1); Au for anti-oxidation layer and Ni for buffer layer to compensate the variation of Cu electrode height and surface topography

Case (2); Ni for barrier layer and Sn for buffer layer to compensate the variation of Cu electrode height and surface topography

Require uniform thickness and morphology of electro-less plated capping layers along the wafer as much possible
Inorganic Anisotropic Conductive Film

Pitch = 100nm
Diameter = 60nm

(a) Top view
(b) Bird view
(c) Top view
(d) Cross view
Hybrid Bonding using Cu Nano-Pillar

SEM cross-sectional images of fabricated TEG module using ultra-high density CNP

CNP give good intact bond with high stacking yield by minimizing the impacts of height variation of electrodes along chip/wafer, particles, and residuals on electrode surface.
Hybrid Bonding using Cu Nano-Pillar

I-V characteristics measured in the daisy chain bonded using high density CNP (after optimization)

- 100% Joining Yield (100K per die)
- Joining resistance; 30 mΩ/Joint (10μm dia. electrode)

(10μm square Cu electrode is used to minimize the misalignment affect)
Multi-Chip FPGA TEG Modules

The configuration and the specification of TEG module for high-end FPGA 2.5D application

- **Die Size**
  - Top TEG die: 7mm x 23mm
  - Bottom interposer die: 31mm x 25mm for 4 dies
300mm FPGA TEG modules Fabricated by Multichip-to-Wafer 3D Stacking
Chip-to-chip, Chip-to-Wafer bonding using Au cone bump
X-ray CT Image

- W plug
- M1
- M2
- M3
- M4
- M5

Au Cone bump connection

- AlCu
Au Cone bump formation

Au/barrier metal/SiO₂

Bump litho.

Si

NpD

He

Close bump hole

Si-sub

Hole pattern

Top view after deposition

After resist lift-off

Photoresist
Material cost of Au bump

- 10^6 micro bumps
- 2.5μm
- 2.5μm
- 30μm ϕ Au wire

Reuse the deposited Au on photoresist

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Cylinder Bump for fragile material
CdTe surface after CdTe/Si-ROIC bonding with Au bump
Bump bonding with cylinder Au bumps

Cylinder bump

Thin (easy to deform)

Fragile material

Si-sub
Bump bonding with cylinder Au bumps

Bump hole patterning

Short Throw (SL) Au spatter

after photoresist lift-off

Cylinder bump

3.5μm

Au electrode

Sputter Au

photoresist

Au

SiO₂
SEM cross sectional view

CdTe

Si ROIC
Process cost reduction for the Heterogeneous Integration
# 3D stack approaches

<table>
<thead>
<tr>
<th></th>
<th>CtC (chip to chip)</th>
<th>CtW (chip to wafer)</th>
<th>WtW (wafer to wafer)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Process cost</strong></td>
<td>High</td>
<td>High ~ Middle</td>
<td>Low</td>
</tr>
<tr>
<td><strong>Stack chips with different chip size</strong></td>
<td>possible</td>
<td>possible</td>
<td>Impossible</td>
</tr>
<tr>
<td><strong>Chip alignment accuracy &lt;0.5μm (3σ)</strong></td>
<td>Difficult from economical stand point</td>
<td>possible ?</td>
<td></td>
</tr>
<tr>
<td><strong>Miscellaneous</strong></td>
<td></td>
<td>Need high yield wafers</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$Y_{total} = Y_{W#1} \times \cdots \times Y_{W#n}$</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Need same size wafers</td>
<td></td>
</tr>
</tbody>
</table>

Need a high speed COW technique with the high alignment accuracy and the practical process cost
Economy of 3D LSI manufacturing

(a) Current 3D Production

LSI Wafer process

Through put

process 1 → process 2 → process 3 → process n-1 → process n

~10k chips/hour

3D integration

3D LSI chip

100 chips/hour

Stack one-by-one

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Economy of 3D LSI manufacturing

(a) Current 3D Production

LSI Wafer process

Through put

process 1 → process 2 → process 3 → process n-1 → process n

10k chips/hour → 100 chips/hour → 3D-IC chip

3D integration

(b) Our Target

Through put

process 1 → process 2 → process 3 → process n-1 → process n → 3D-IC chip

10k chips/hour → 10k chips/hour
“Super Chip”
Self-assembly Technique
Self-assembly technique

- hydrophilic area
- hydrophobic area
- droplet
- 5mm
New Reconfigured Wafer-to-Wafer 3D Integration

Known good die (KGD) 3rd layer chip  Reconfigured wafer

Failure die 2nd layer chip

LSI wafer with/without TSV 1st layer chip  Carrier wafer  interposer  

3D super chip

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Self-Assembly & Electrostatic (SAE) Bonding

1. Face-up KGD release

2. Self-assembly

3. Electrostatic bonding

4. Inverse-voltage apply

5. Electrostatic debonding

CA: < 30°
Assembly area (hydrophilic)

CA: > 110°
Surrounding area (hydrophobic)

Cross-sectional view

Top view
Thank you for your kind attention.

If there’s anything you are unclear on, please feel free to contact me. motoyoshi@t-microtec.com