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Status and road map of hybridization technologies relevant to future pixel detectors

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A 3D-IC is an effective solution for reducing the manufacturing costs of advanced 2D LSI while ensuring equivalent device performance and functionalities. This technology allows for a new device architecture of stacked detectors/sensor devices with a small dead sensor area and facilitates hyper-parallel data processing. In pixel sensors and detectors, many transistors must be accommodated per pixel area to improve the space and time resolutions without increasing the pixel size. Currently, many methods to realize 3D-LSI devices have been developed by focusing on the unit processes of 3D-LSI technology: (1) through-silicon via (TSV) formation, (2) bump formation, (3) wafer thinning, (4) chip/wafer alignment, and (5) chip/wafer bonding. However, these unit processes are incompatible in terms of various device and process requirements such as process temperature, device structure, TSV and bump dimensions, yield, reliability, and supply chain. In this paper, recent 3D-IC technology and market trend are introduced. And Current development status, design rule, 3D structure, yield issues and the cost reduction method for stacked pixel detectors will be presented.

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