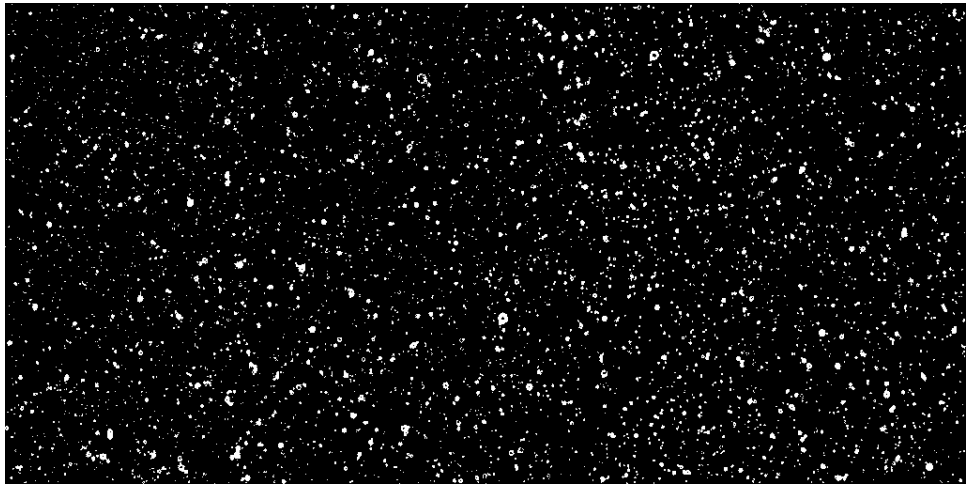
Okinawa, December 11, 2017

Monolithic CMOS sensors for high energy physics

W. Snoeys, CERN



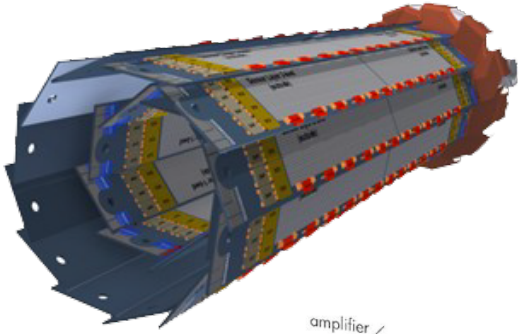
p-ALPIDE3 chip: 200 MeV p at PSI

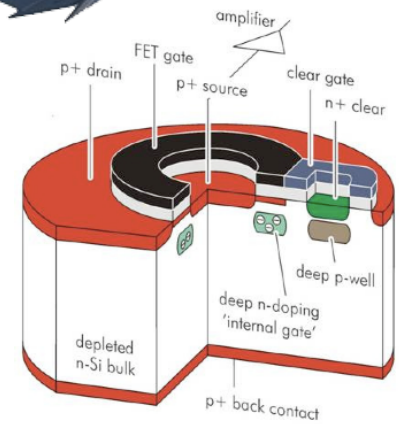
Acknowledgements

- The workshop organizers
- T. Kugathasan, G. Aglieri, H. Pernegger, L. Musa, P. Riedler
- G. Anelli, F. Anghinolfi, P. Aspell, R. Ballabriga, S. Bonacini, M. Campbell, J. Christiansen, R. De Oliveira, F. Faccio, P. Farthouat, E. Heijne, P. Jarron, J. Kaplon, K. Kloukinas, A. Kluge, T. Kugathashan, X. Llopart, A. Marchioro, S. Michelis, P. Moreira, K. Wyllie, M. Mager, M. Keil, D. Kim, A. Dorokhov, A. Collu, C. Gao, P. Yang, X. Sun, H. Hillemanns, S. Hristozkov, A. Junique, M. Kofarago, M. Keil, A. Lattuca, M. Lupi, C. Marin Tobon, D. Marras, M. Mager, P. Martinengo, G. Mazza, H. Mugnier, H. Pham, J. Rousset, F. Reidt, P. Riedler, J. Van Hoorne, P. Yang, D. Gajanana, A. Sharma, B. Blochet, C. Sbarra, C. Solans Sanchez, C. Riegel, C. Buttar, D. Michael Schaefer, D. Maneuski, I. Berdalovic, K. Moustakas, M. Dalla, N. Wermes, N. Egidos Plaja, R. Bates, R. Cardella, T. Wang, T. Hemperek, T. Hirono, W. Wong, G. Iacobucci, M. Barbero, P. Pangaud, A. Habib, S. Bhat, I. Peric, R. Casanova, S. Grinstein, Y. Degerli, F.Guilloux, P. Schwemling…

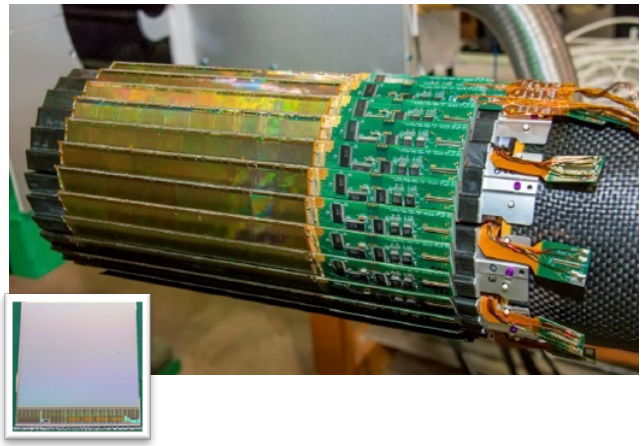
and other collegues from CERN and the ALICE ITS upgrade and ATLAS ITk

Monolithic sensors in HEP move into mainstream technology





DEPFET in Belle



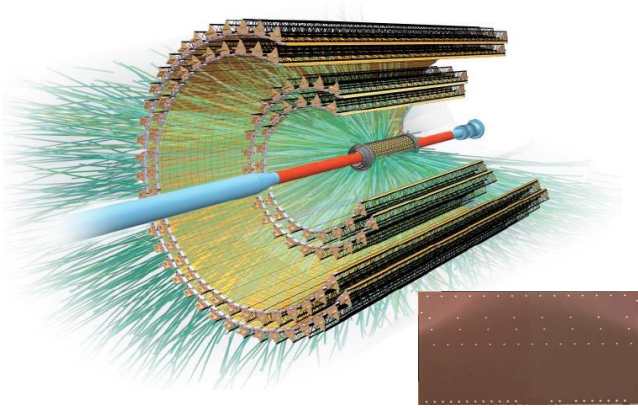
MIMOSA28 (ULTIMATE) in STAR

IPHC Strasbourg

First MAPS system in HEP

Twin well 0.35 µm CMOS

- Integration time 190 µs
- No reverse bias -> NIEL few 10^{12} 1 MeV n_{eq}/cm^2
- Rolling shutter readout



ALPIDE in ALICE

First MAPS in HEP with sparse readout similar to hybrid sensors

Quadruple well 0.18 µm CMOS

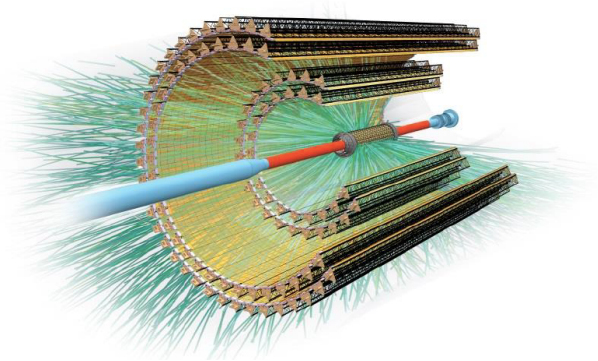
- Integration time <10 µs
- Reverse bias but no full depletion -> NIEL ~10^{14} 1 MeV n_{eq}/cm^2

Commercial deep submicron CMOS technology evolved "naturally" towards

- Very high tolerance to ionizing radation (even if there are some caveats)

  see F. Faccio's presentation
- Availability of substrates compatible with particle detection

ALICE ITS upgrade



Motivation

- 3x better impact parameter resolution
- Better tracking efficiency and momentum resolution at low pT
- Faster readout
- Fast removal and insertion

Technical Design Report for the Upgrade of the ALICE Inner Tracking System
J. Phys. G 41 (2014) 087002
CERN-LHCC-2013-024 ; ALICE-TDR-017

Sensor chip requirements

Parameter	Inner Barrel	Outer Barrel
Chip size (mm x mm)	15 x 30	
Chip thickness (μm)	50	100
Spatial resolution (μm)	5	10 (5)
Detection efficiency	> 99%	
Fake hit rate	$< 10^{-5}$ evt^{-1} pixel^{-1} (ALPIDE $<< 10^{-5}$)	
Integration time (μs)	< 30 (< 10)	
Power density (mW/cm^2)	< 300 (~35)	< 100 (~20)
TID radiation hardness (krad) (**)	2700	100
NIEL radiation hardness (1 MeV n_{eq}/cm^2) (**)	1.7×10^{13}	1.7×10^{12}
Readout rate, Pb-Pb interactions (kHz)	100	
Hit Density, Pb-Pb interactions (cm^{-2})	18.6	2.8

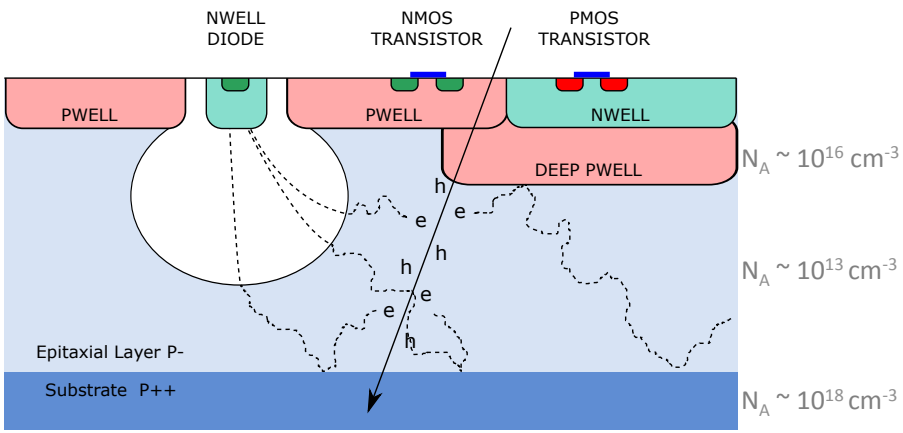
(*) In color: ALPIDE performance figure where above requirements
(**) 10x radiation load integrated over approved program (~ 6 years)

Thin sensors (50 μm), high granularity (~30 x 30 μm^2), large area (10 m^2)
moderate radiation (TID 2.7 Mrad & NIEL 1.7 10^{13} 1 MeV n_{eq}/cm^2)

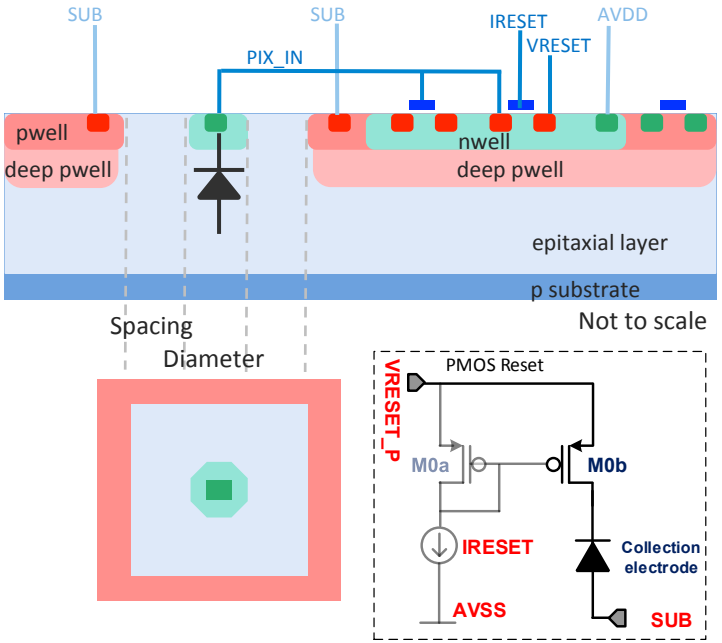
→ Monolithic Active Pixel Sensors

Standard Pixel Sensor imaging Process (TowerJazz)

CMOS 180nm
3 nm thin gate oxide, 6 metal layers

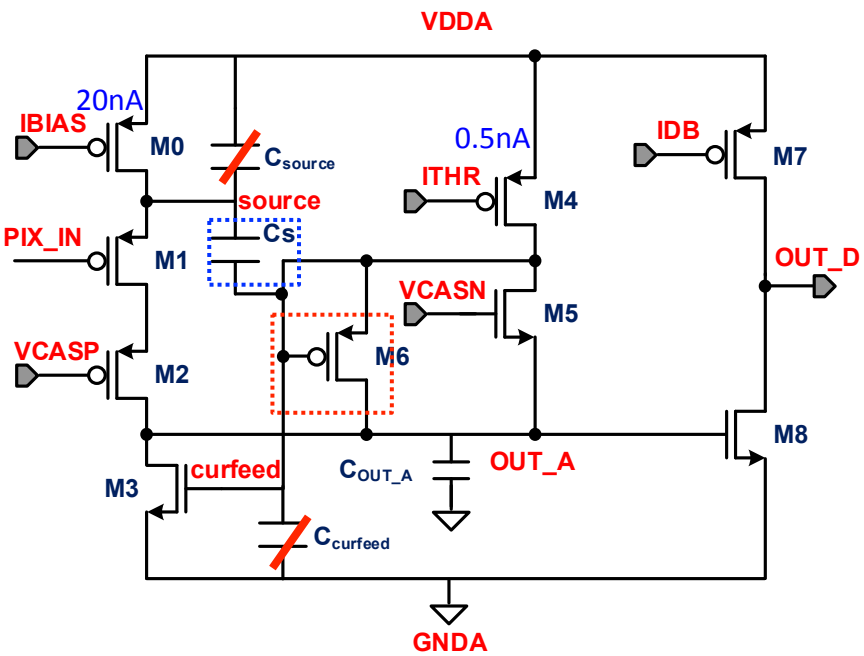


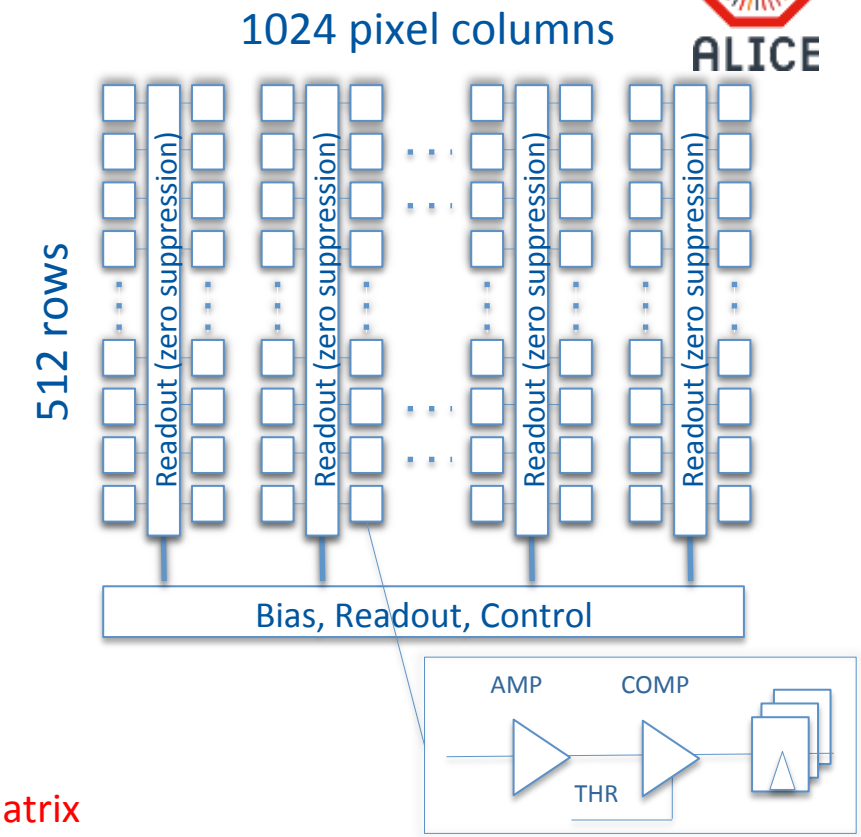
Not to scale



- High-resistivity (> 1kΩ cm) p-type epitaxial layer (18 μm to 30 μm) on p-type substrate
- Deep PWELL shielding NWELL allowing PMOS transistors (full CMOS within active area)
- Small n-well diode (2 μm diameter), ~100 times smaller than pixel and reverse substrate bias => low capacitance (2fF) => large S/N => better analog performance at lower power.

ALPIDE





Front end (40 nW, continuously active)

D. Kim et al. TWEPP 2015,

DOI 10.1088/1748-0221/11/02/C02042

- Analog power ~ $(Q/C)^{-2}$ NIM A 731 (2013) 125
- C(sensor+circuit) < 5 fF, Q/C ~ 50 mV in ALPIDE
- Used with increased current for ATLAS development

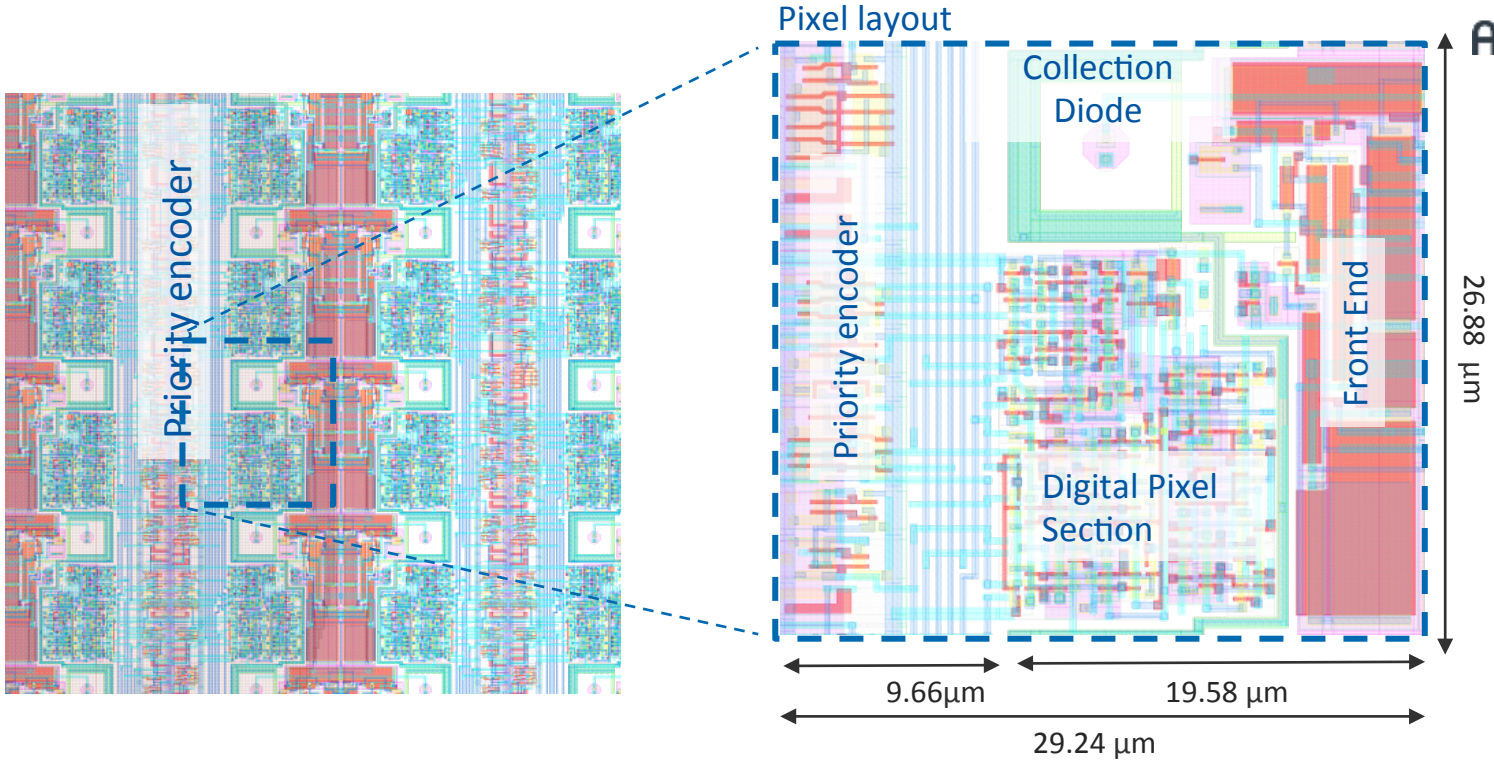
Matrix

G. Aglieri et al. NIM A 845 (2017) 583-587

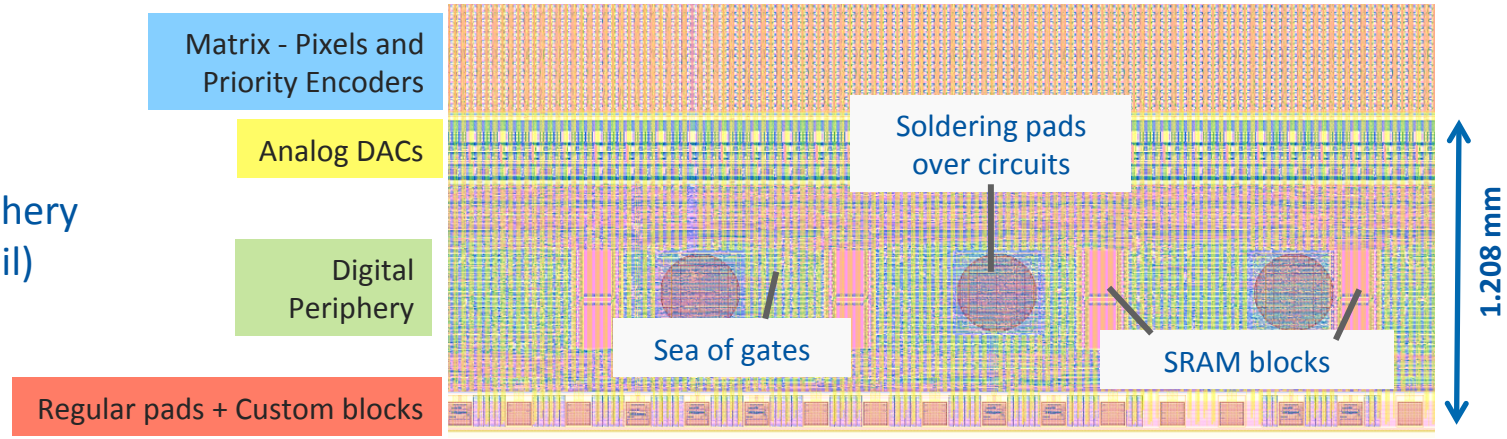
- 29 μm x 27 μm pixel pitch
- In pixel amplification and discrimination and 3 data registers
- Global shutter, triggered or continuous readout
- Zero suppressed readout, no hits no power

ALPIDE Layout features

Matrix (detail)



Periphery (detail)



ALPIDE Development

Design team: G. Aglieri, C. Cavicchioli, Y. Degerli, C. Flouzat, D. Gajanana, C. Gao, F. Guilloux, S. Hristozkov, D. Kim, T. Kugathasan, A. Lattuca, S. Lee, M. Lupi, D. Marras, C.A. Marin Tobon, G. Mazza, H. Mugnier, J. Rousset, G. Usai, A. Dorokhov, H. Pham, P. Yang, W. Snoeys
(Institutes: CERN, INFN, CCNU, YONSEI, NIKHEF, IRFU, IPHC) and comparable team for test

2012 — Explorer

20μm x 20μm and 30μm x 30μm pixels (analogue readout)
pixel geometry, starting material, sensitivity to radiation

2013 — pALPIDEss-0

Matrix with 64 columns x 512 rows
22 μm x 22 μm pixels
In-pixel discrimination and buffering
Zero suppression within pixel matrix

2014 — pALPIDE-1

First full-scale prototype
Pixel pitch: 28 μm x 28 μm
4 sectors with pixel variants
1 register/pixel, no final interface

Apr 2015 — pALPIDE-2

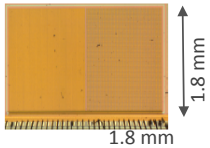
4 sectors with pixel variants
Optimization of circuits
Allowing integration in ITS modules
No high-speed serial output

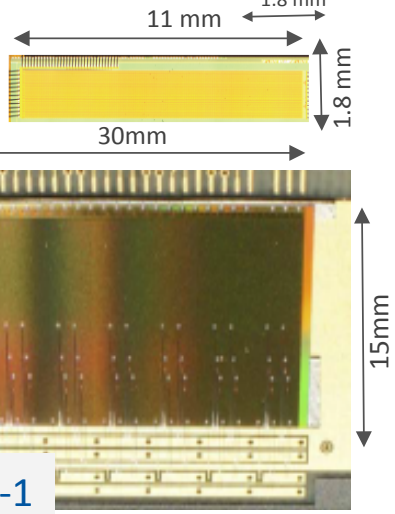
Oct 2015 — pALPIDE-3

8 sectors with pixels variant
All Communication Features
(no ADC, no Temp Sens)

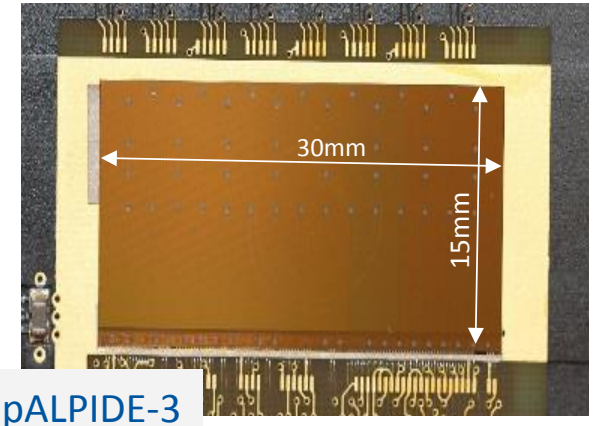
Aug 2016 — ALPIDE

Single pixel variant
All features and optimization





pALPIDE-1

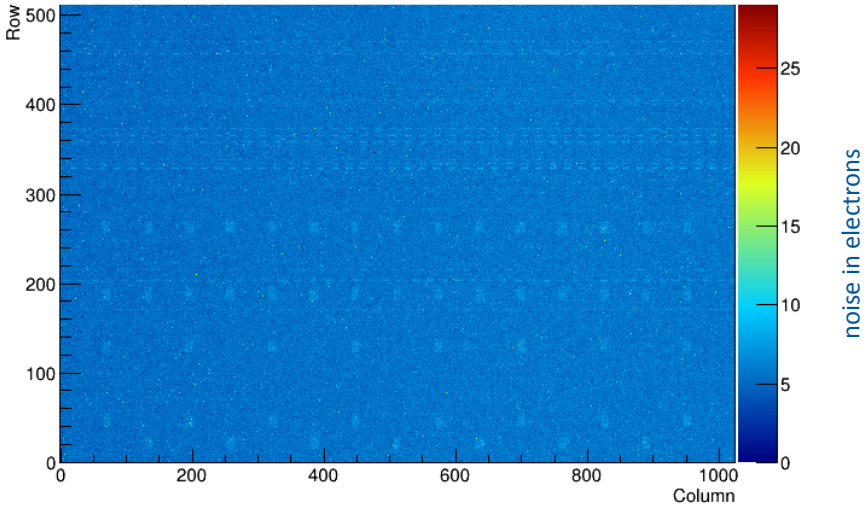


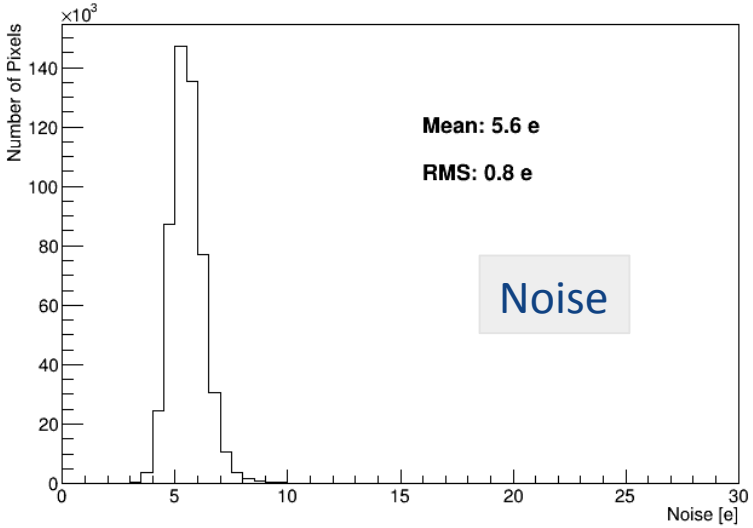
pALPIDE-3

ALPIDE – Some Results

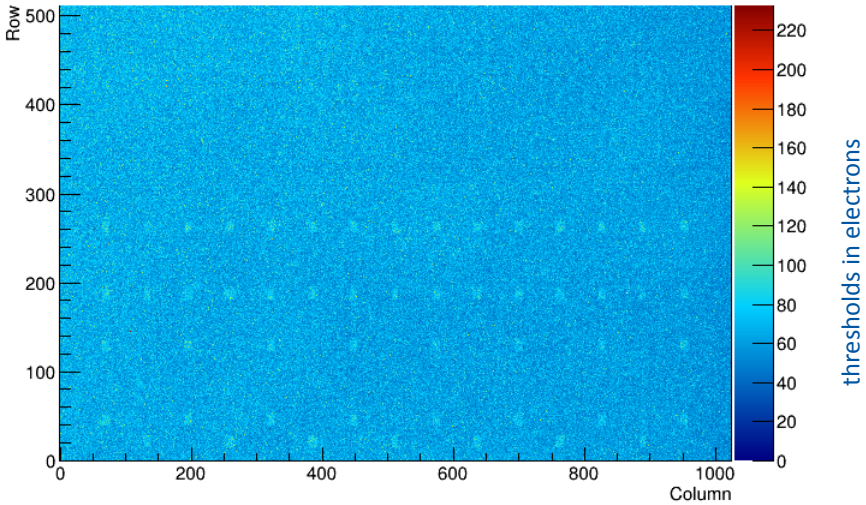
Charge threshold and Noise

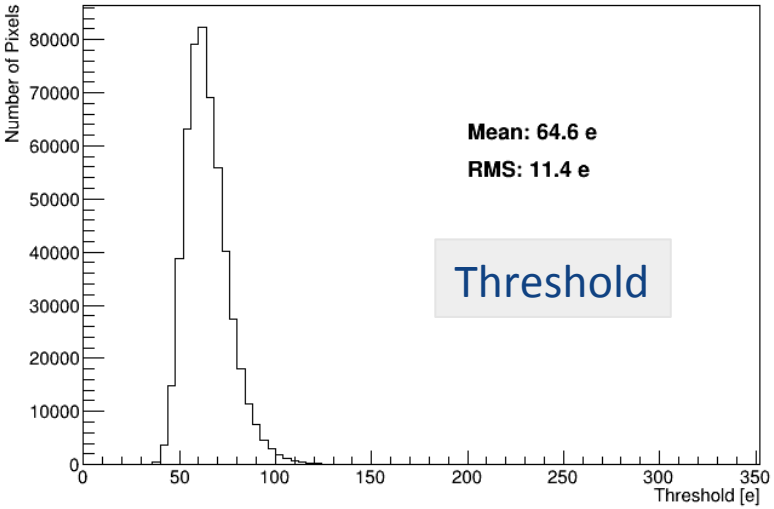
Noise Map



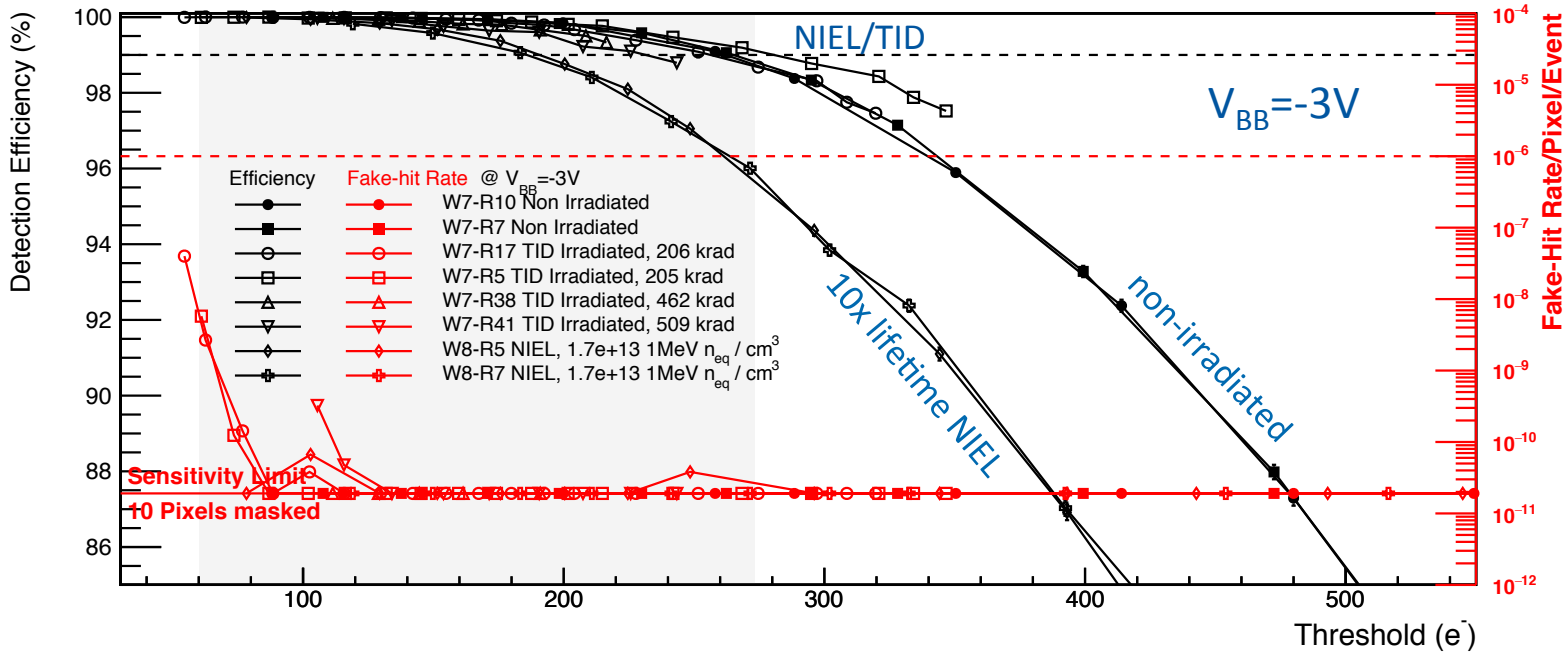


Threshold MAP





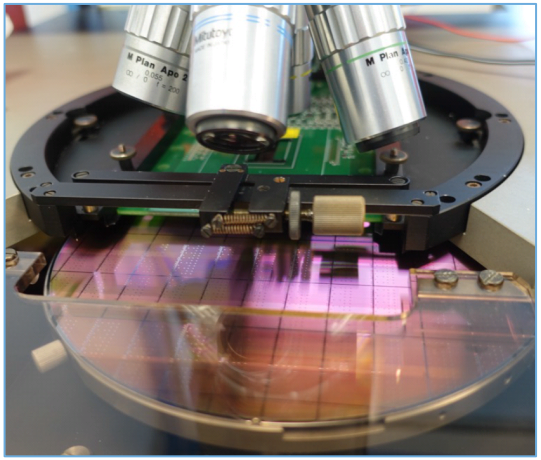
Detection Efficiency and Fake Hit Rate



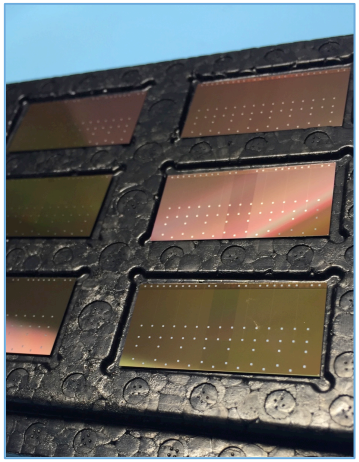
- Large operational margin with only 10 masked pixels (0.002%)
- Chip-to-chip fluctuations negligible
- Non-irradiated and NIEL/TID chips show similar performance
- Sufficient operational margin after 10x lifetime NIEL dose

ALPIDE & ITS Upgrade status

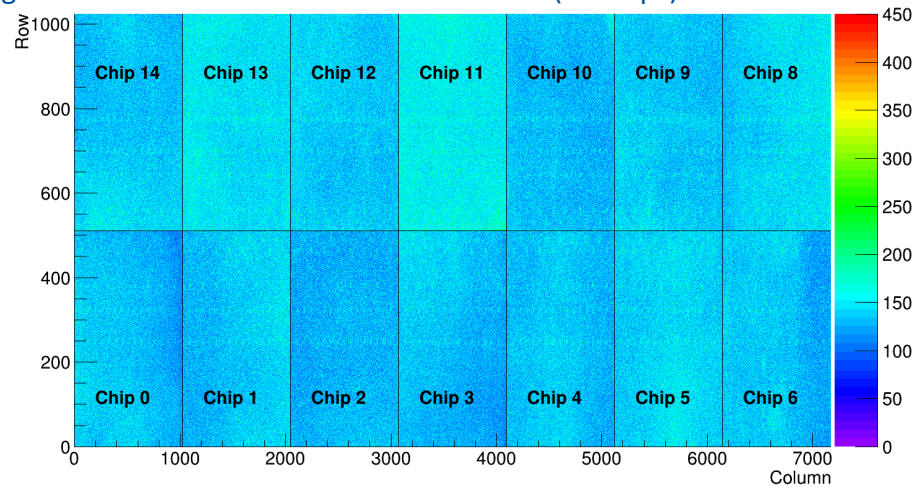
Wafer probe testing

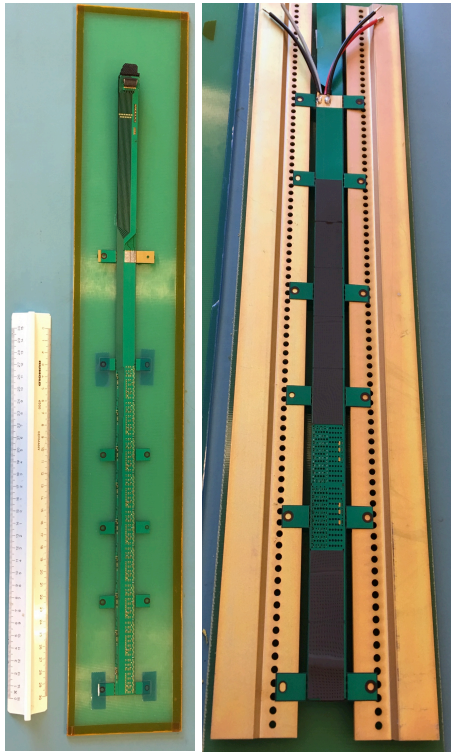


Single chips after thinning & dicing



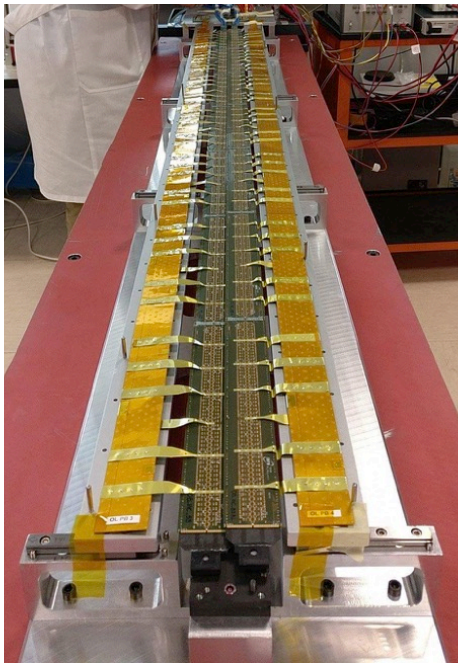
Threshold scan outer Barrel Module (14 chips)





Inner Barrel Module (9 chips)

Over 500 wafers produced



Outer Barrel Stave (~100 M pixels)

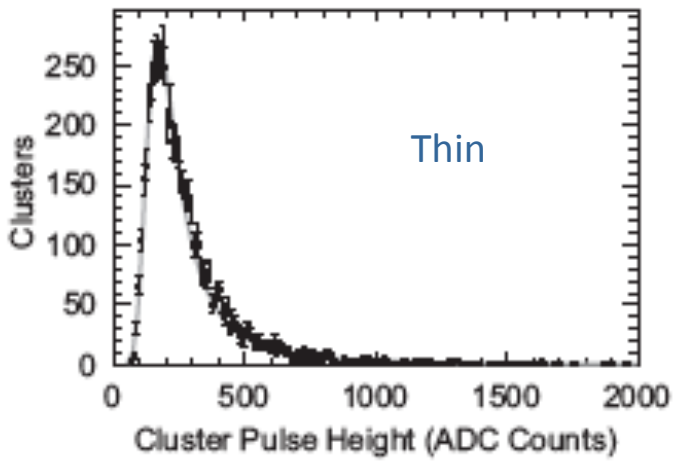
Requirements

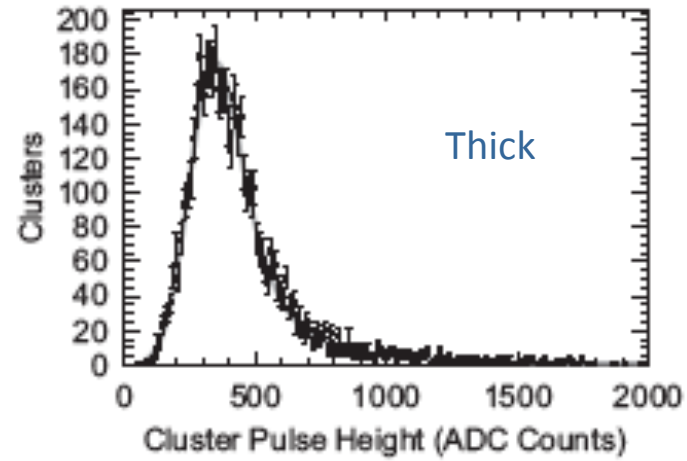
	Dose (Mgy)	Fluence (10^{16} 1MeVn_{eq}/cm^2)
ALICE ITS	0.01	10^{-3}
LHC	1	0.1…0.3
HL-LHC 3ab^{-1}	5	1.5
FCC	10-350	3-100

- Radiation tolerance
  - Ionizing radiation
  - Non-ionizing radiation (displacement damage)
  - Circuit typically more sensitive to ionizing radiation, sensor to non-ionizing radiation
- Single particle hits instead of continuously collected signal in visible imaging
  - Near 100% efficiency, full CMOS in-pixel needed
- Position resolution (~µm)
- Low power consumption as the key for low mass
  - Now tens of mW/cm^2 for silicon trackers and hundreds of mW/cm^2 for pixels
  - Even with enhanced detector functionality for upgrades, power consumption cannot increase too much because of the material penalty
- More bandwidth
- Time resolution
  - Time stamping ~ 25 ns or even lower, ... much lower (10s of ps)

Single point resolution: the importance of S/N

Pitch = 13.75 µm





SOI detector: thin=thinned to 70 µm, thick = 250 µm (only partially depleted)

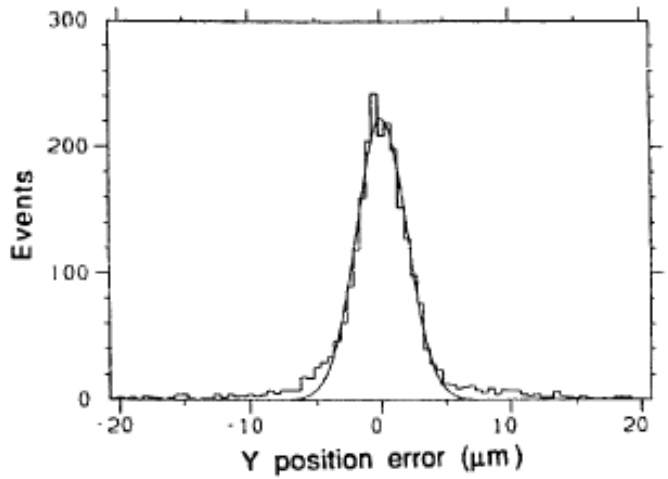
SOI sensor	V_d (V)	d (µm)	Cluster ⟨S/N⟩	Efficiency	σ_{point} (µm)
Thin	30	60 ± 5	25.0	0.90 ± 0.04	3.1 ± 0.80
	50	64 ± 3	28.2	0.94 ± 0.03	1.7 ± 0.50
	70	64 ± 3	28.8	0.96 ± 0.03	1.8 ± 0.60
	90	64 ± 3	31.2	0.98 ± 0.02	1.9 ± 0.70
Thick	30	60 ± 8	23.3	0.89 ± 0.03	1.36 ± 0.04
	50	103 ± 5	47.4	$0.98^{+0.02}_{-0.04}$	1.12 ± 0.03
	70	122 ± 5	52.7	$0.99^{+0.01}_{-0.05}$	1.07 ± 0.05

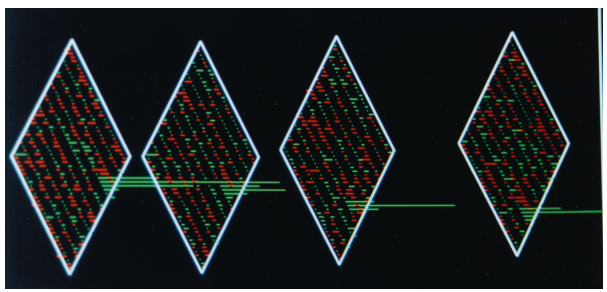
Better S/N
=>
Better point resolution

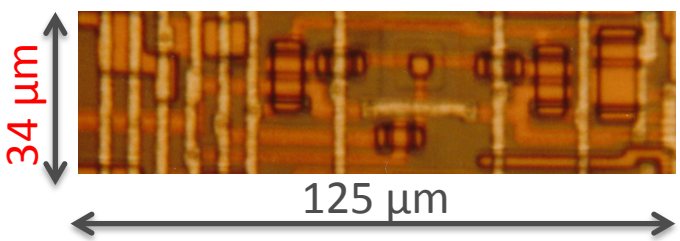
Due to capacitive pixel-to-pixel coupling, practically no single pixel clusters...

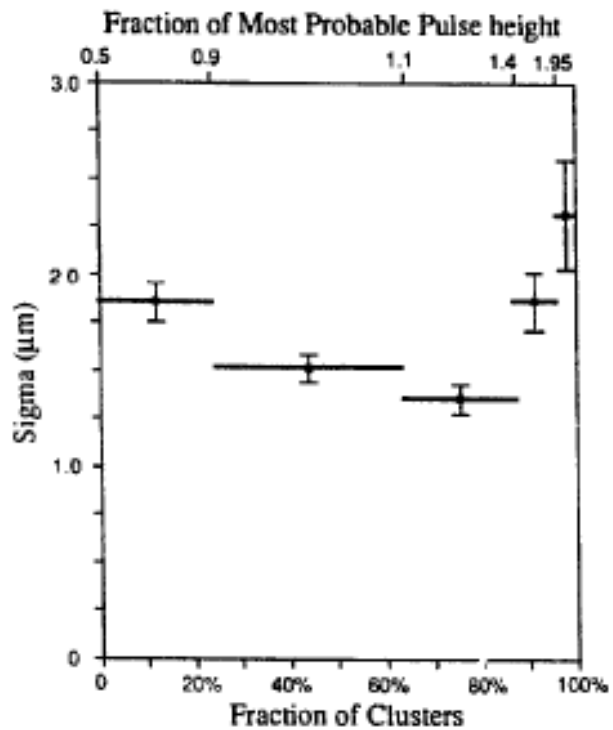
M. Battaglia et al. NIM A 654 (2011) 258-265, NIM A 676 (2012) 50-53

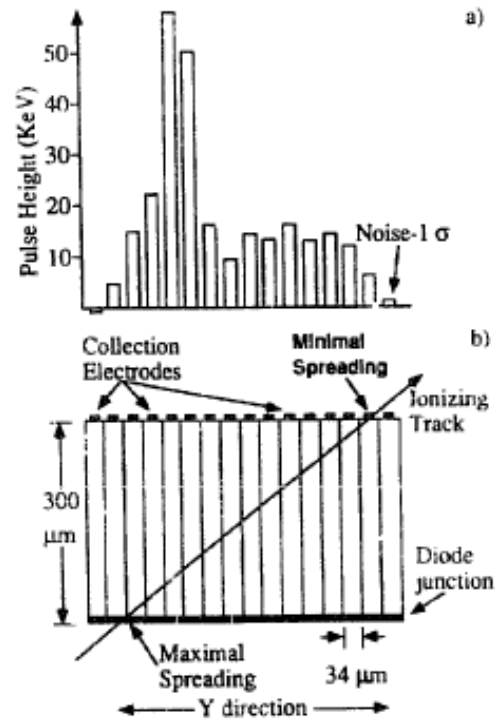
Point resolution at larger pixel pitches











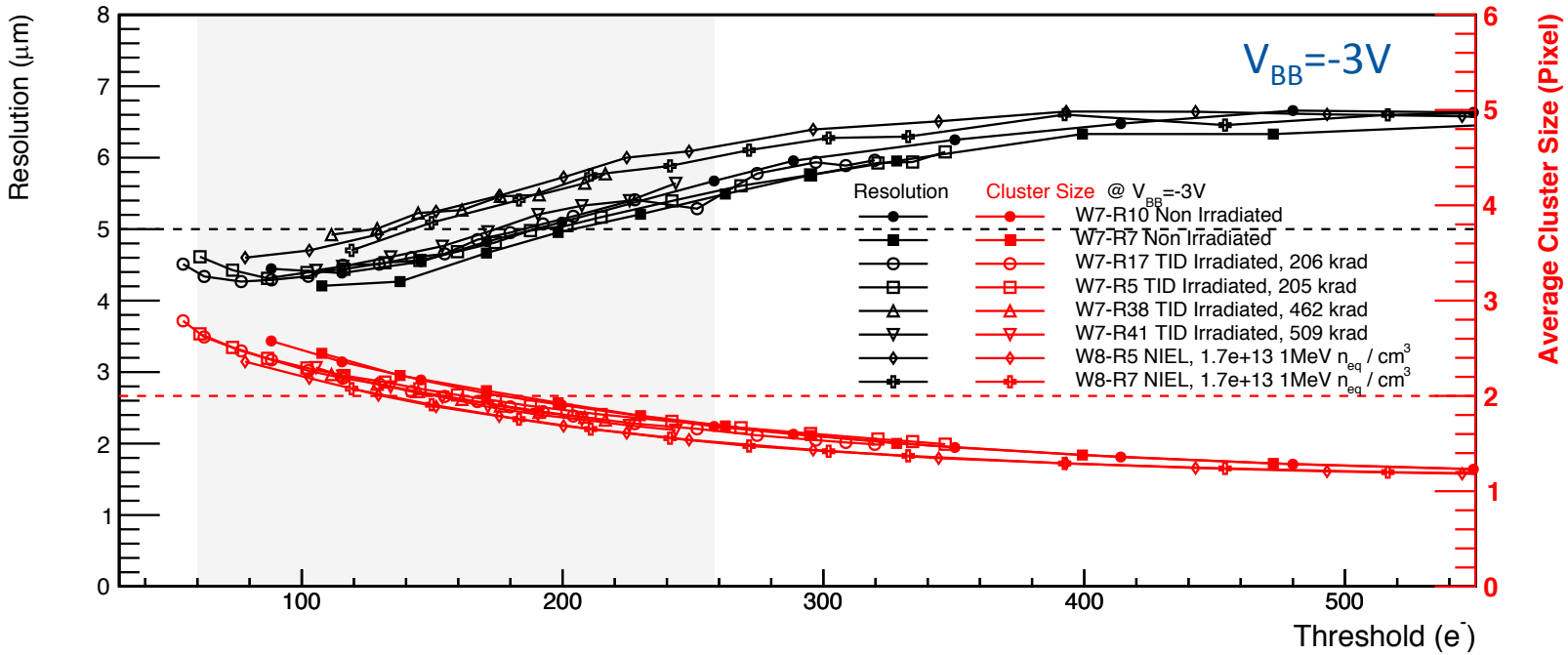
C. Kenney et al. NIM A (1994) 258-265

- Thickness 300 µm, Q = 4 fC, C=26fF, $S/N_{single\ ch}$ = 150/1
- S/N for tilted tracks very quickly much lower, better to take extremities.

Single point resolution

- Sensor can deliver ~ 1µm point resolution if granularity and S/N sufficient
- Unless S/N is very large, detector depth and pixel pitch should be comparable to avoid degradation in S/N and hence resolution for inclined tracks.
- Examples used analog interpolation with charge shared practically always between minimum 2 pixels. With binary readout, good single point resolution can be achieved as well. Need sufficient granularity, but also sufficient S/N.

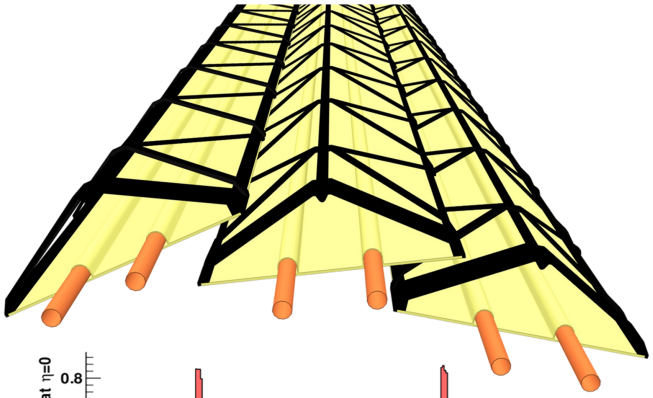
ALPIDE Position resolution and cluster size

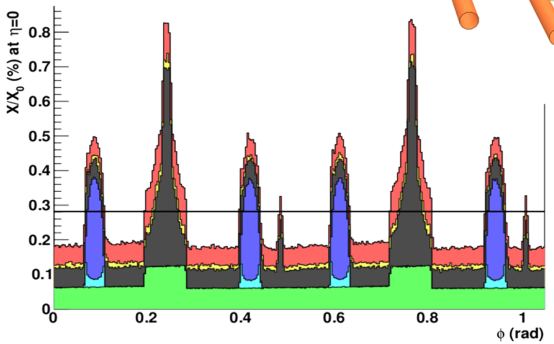


- Here digital interpolation
- Chip-to-chip fluctuations negligible
- Non-irradiated and TID/NIEL chips show similar performance
- Resolution of about 6μm at a threshold of 300 electrons
- Sufficient operational margin even after 10x lifetime NIEL dose

Low power consumption to reduce material budget

Inner Barrel



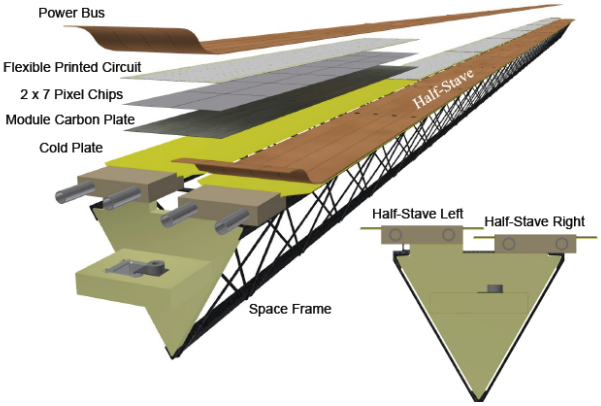


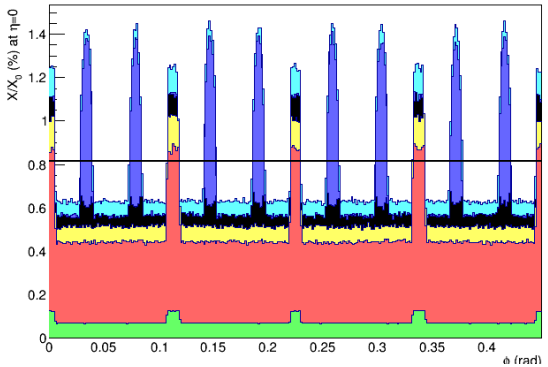
Flex Printed Circuit (22%)
Glue (5%)
Carbon Structure (33%)
Water(13%)
Cooling pipes wall (2%)
Pixel Chip (26%)

Mean X/X0 = 0.282%

Power density specification : <100 mW/cm^2

Outer Barrel



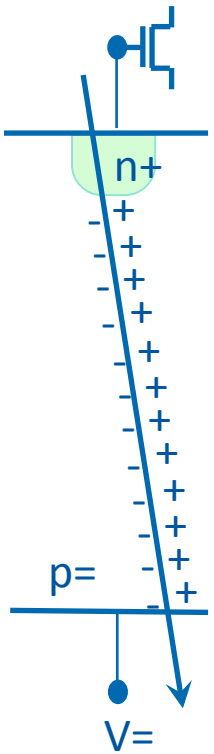


Carbon Structure (9.1%)
Water (14.2%)
Cooling Pipe Walls and Cold Plate (8.0%)
Glue (9.5%)
Flex Cable (50.1%)
Pixel Chip (9.2%)

50 %

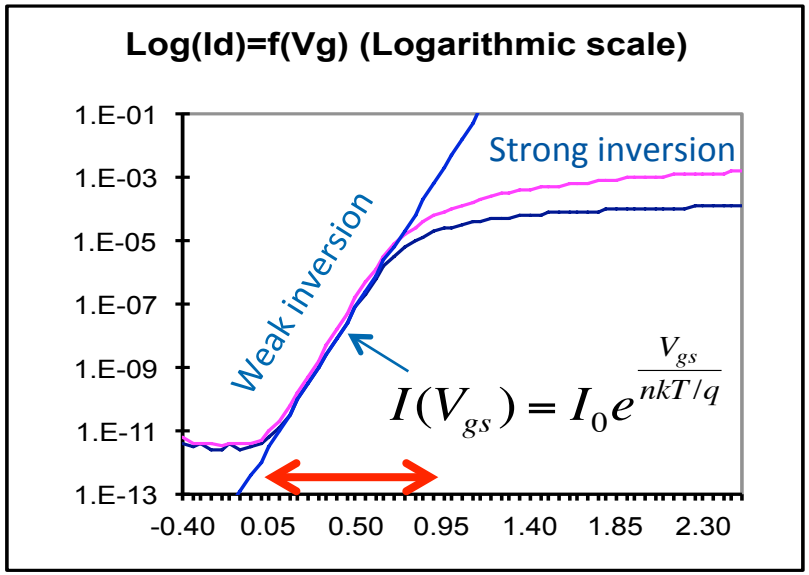
ALICE ITS Mechanics: C. Garguilo et al (see also his ECFA 2014 presentation)

Analog power



$$C_{spherical} = \frac{4\pi\varepsilon}{\frac{1}{R_1} - \frac{1}{R_2}} \approx 4\pi\varepsilon R_1$$

Add connection + circuit



Non-linearity in the weak inversion region

- From noise considerations : analog power ~ $(Q/C)^{-2}$ (NIM A 731 (2013) 125)
- Q/C = ~ 50 mV in ALPIDE (and MALTA/TJ MONOPIX)

  (Conventional 300 μm thick strip detector: Q/C = 4fC/20pF = 0.2mV)
- nkT/q = 40 mV @ Room Temperature

  => increase Q/C further to exploit the weak inversion non-linearity

Digital architecture: power (and bandwidth)

Energy per 1 cm toggled line at 1.8 V = CV^2 = 2 pF x $(1.8\ V)^2$ = **6.5 pJ**

Deeper submicron: 2 pF x $(1\ V)^2$ = **2 pJ !**

- Architecture choice: keep data in pixel until level 1 or transmit info immediately
  - Power trade-off between hit activity and clock distribution
  - No clock distribution often yields lower power but asynchronous circuit is less conservative
- Clock distribution over the matrix (needed if data kept in pixel) ?

  200 lines per cm (1 per double column) for 25 µm pixel pitch:

  200 x 6.5 pJ x 40 MHz = 50 mW/cm^2
- Hit activity
  - If 1 bit (or rather one line toggle) is sent to periphery for every pixel hit *before* trigger
  - Average power = hit rate x column height/2 x 6,5 pJ/cm^2 = R x H x 6,5 pJ/2 (see table next page)

Digital architecture: power (and bandwidth)

- Power per bit transmitted per hit as a function of hit rate

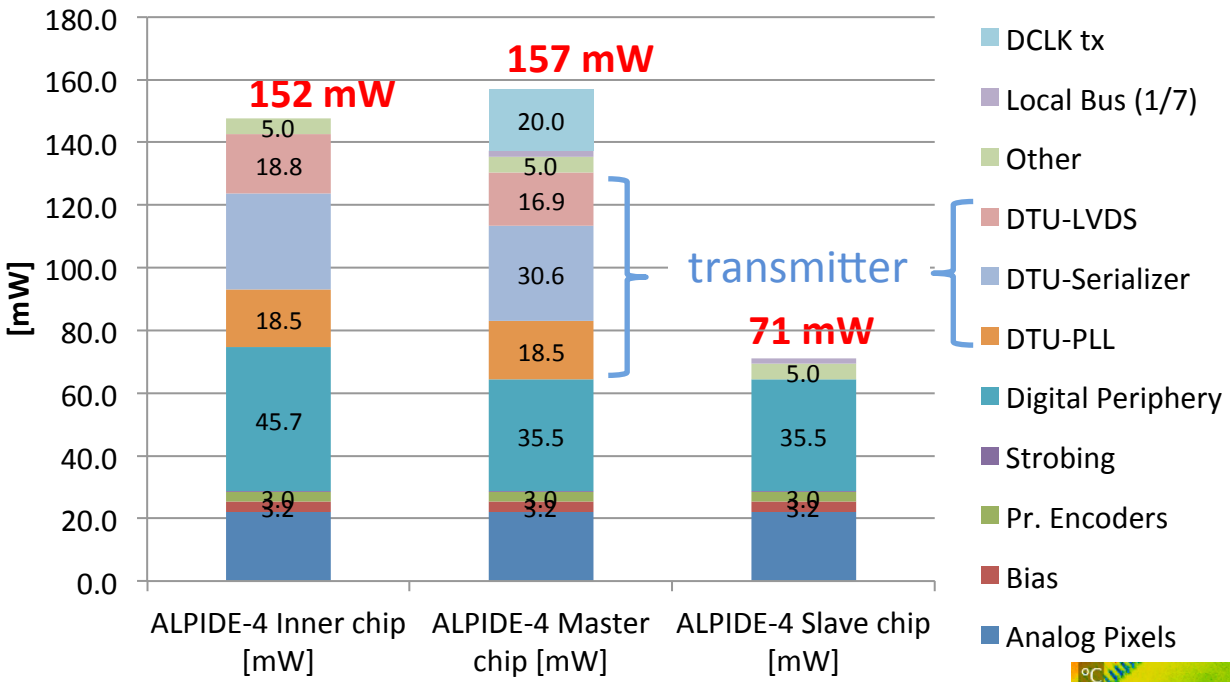
ATLAS	hit rate		Power/bit/cm^2 (H=2 cm)
Layer	hit/BC/mm^2	Mhit/mm^2/s	mW/cm^2
0	0,68	27,2	17,68
1	0,21	8,4	5,46
2	0,043	1,72	1,118
3	0,029	1,16	0,754
4	0,021	0,84	0,546

- Massive parallelism makes huge on-chip bandwidth available (Gb/s/µm !),

  but 1 GHz clock over 1 cm length takes 6.5 mW

  => need to keep activity down for low power

ALPIDE Power consumption:



Sensitive area: 4.12 cm^2

Inner Barrel: 36.9 mW/cm^2

Outer Barrel: 20.2 mW/cm^2

In the matrix:

(analog + digital)/area

(22.2 + 3.2)/4.12

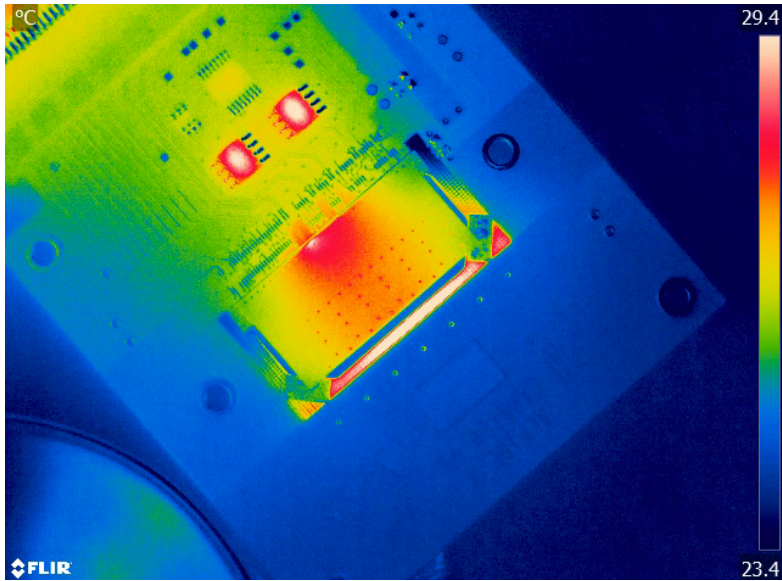
= 6.2 mW/cm^2

With 40 nW front-end and Q/C ≈ 80 mV analog power consumption still dominant within the matrix

Matrix readout only active if hit present

Clock gating in the digital periphery

For the future more work needed on Q/C, architecture periphery and transmitter for overall power consumption



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Off-detector data transmission

- Present developments for HEP: significant power penalty to be SEU robust
  - P. Moreira et al. : Low Power GBT :

    500mW for 9.6Gb/s (65nm) (GBT 2 W(130nm)) (including many features)
  - V. Gromov et al. : Velopix: (TWEPP2014)

    60 mW for 5.12 Gb/s transmission (+ PLL 30 mW) over 70 cm flex (130nm)
  - TDCpix (NA62):

    4*87mW (serializer) + 110 mW (PLL) for 3x3.2=12.8 Gb/s (130nm)
- Good progress in general R&D: going deeper submicron 1-2 pJ/bit at 10's of Gb/s

ISSCC 2013 / SESSION 2 / ULTRA-HIGH-SPEE

2.6 A 32-to-48Gb/s Serializing Transmitter Using Multiphase Sampling in 65nm CMOS

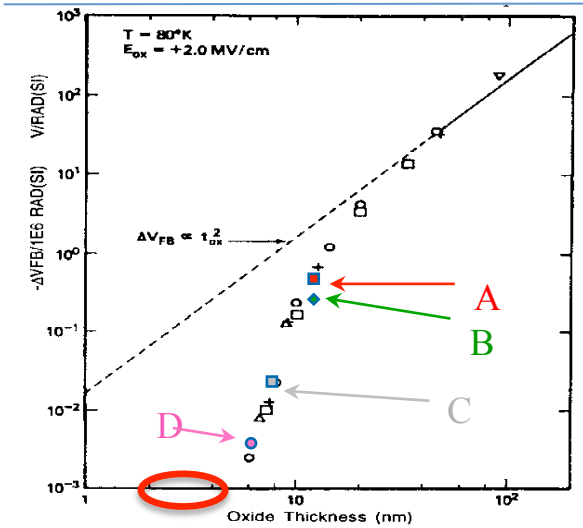
Amr Amin Hafez, Ming-Shuan Chen, Chih-Kong Ken Yang

University of California, Los Angeles, CA

Block	Power (mW)	Fraction (%)
VCO	26.6	30.2
Divider Chain	18	20.5
Buffer/PFD/CP	2	2.3
Predriver/Driver	26.4	30
Serializer	15	17
Total	88	100

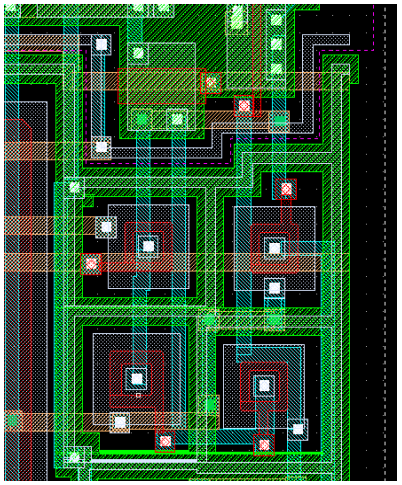
Important: data concentration & physical volume for material budget & technology

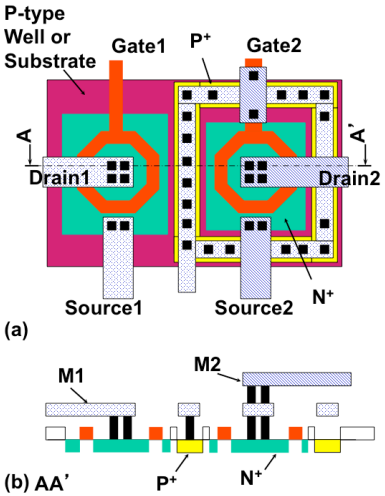
Transistor radiation tolerance



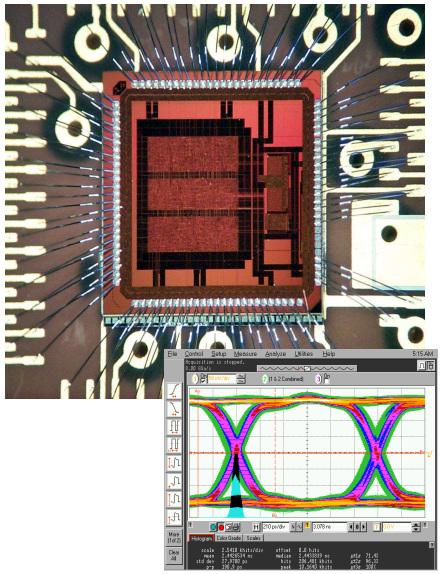
Now here

After N.S. Saks et al,
IEEE TNS, Vol. NS-31 (1984) 1249





G. Anelli et al., IEEE TNS-46 (6) (1999) 1690



P. Moreira et al.
http://proj-gol.web.cern.ch/proj-gol/

Total ionizing dose:

- Intrinsic transistor has become more and more radiation tolerant due to thinner gate oxide
- In LHC enclosed NMOS transistors and guard rings in 0.25 µm CMOS to avoid large leakage current
- In deeper submicron enclosed geometry usually no longer necessary for leakage, but for small dimensions parasitic effects dominate, **requires extensive measurement campaigns**

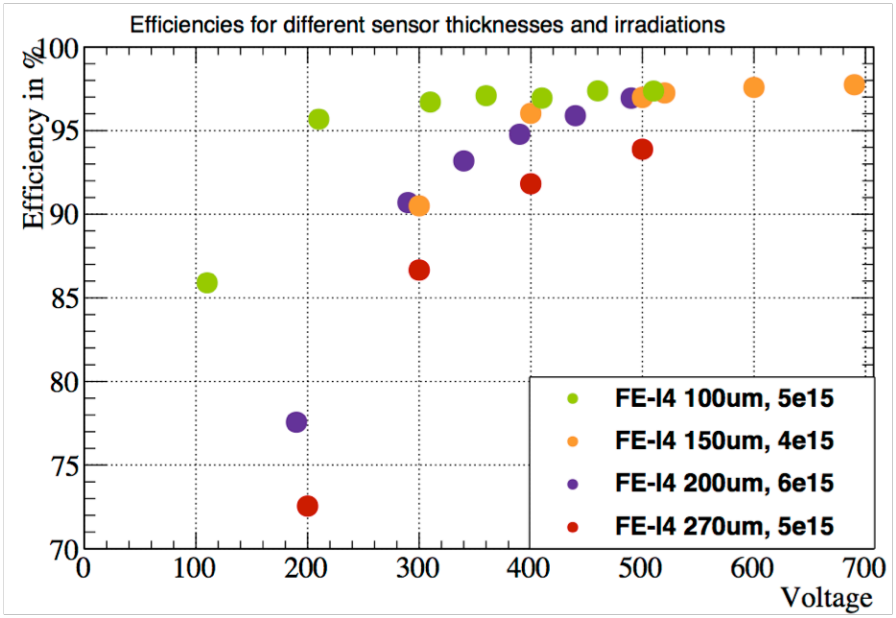
Single event effects:

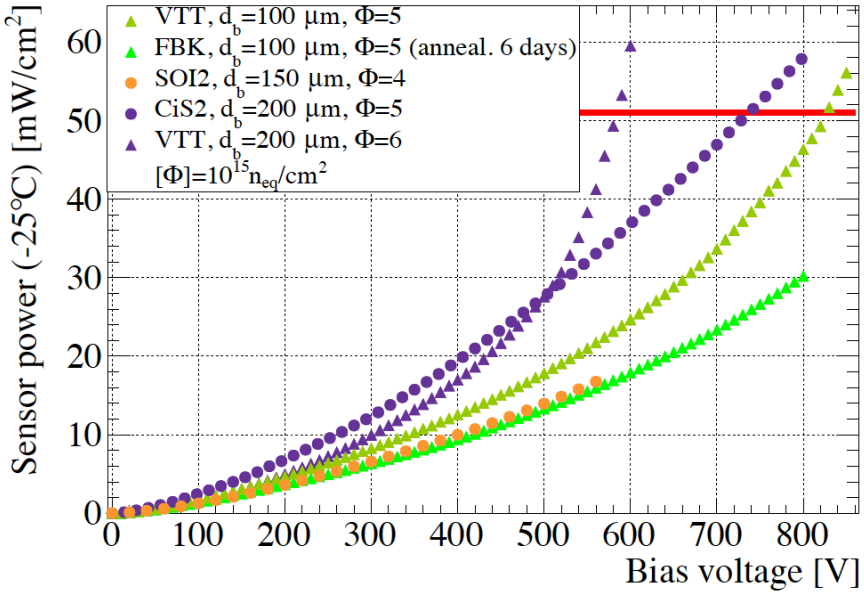
- Single Event Upset : triple redundancy with majority voting
- Latch-up not observed so far in LHC, but observed on MAPs at STAR, and in new technologies

=> **need attention in the design**

See F. Faccio's presentation

Sensor radiation tolerance



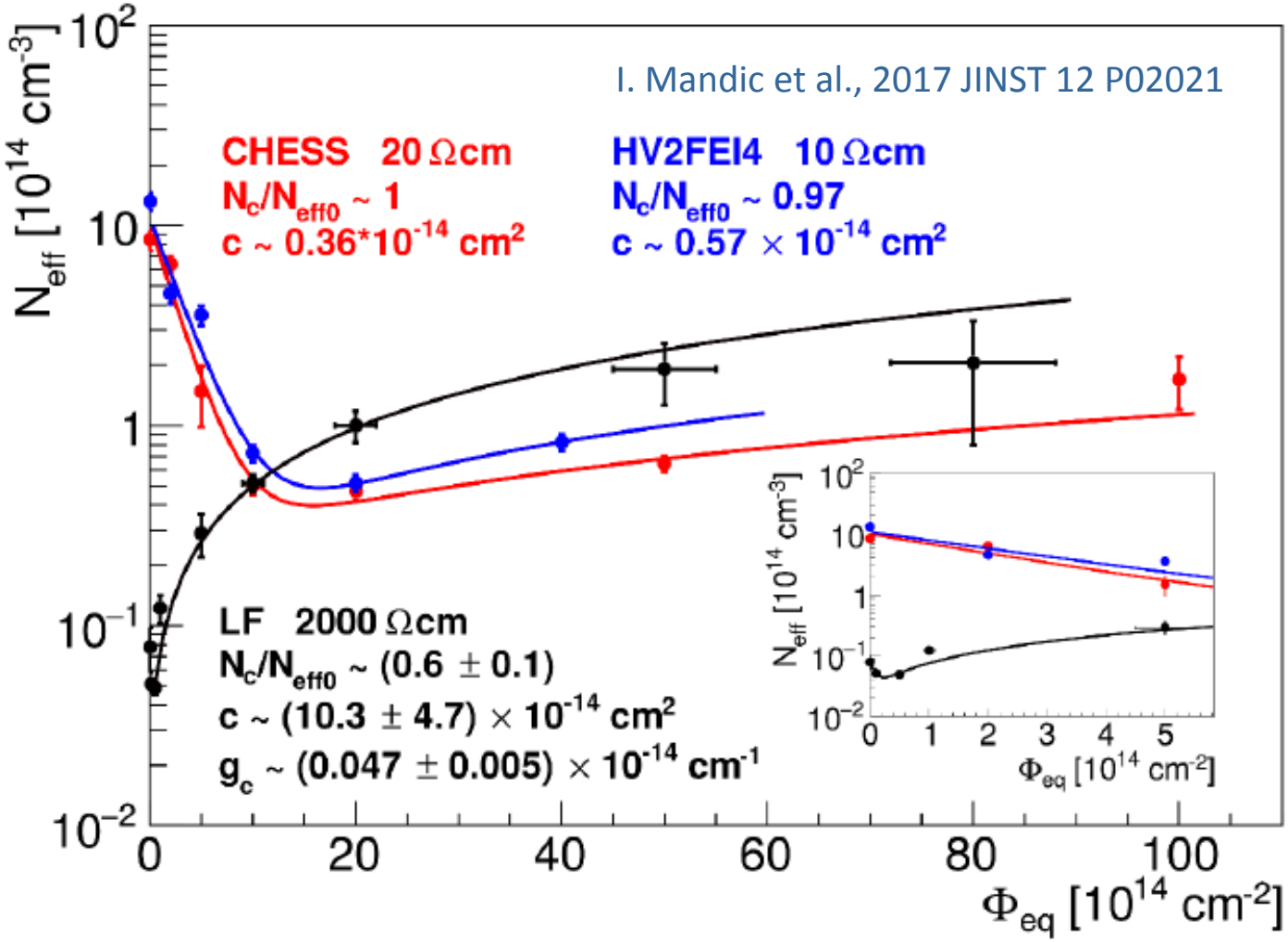


A. Macchiolo, R. Nisius, N. Savic, S. Terzo, 10th Hiroshima Symposium, X'iang, China, 2015
See also N. Savic et al. 27th RD50 workshop, CERN, 2015

Can no longer exploit thick sensitive layers:

- Need **depletion and drift field to collect signal charge fast** before it can be trapped.
- Need thin layer to contain power consumption from leakage current, and appropriate reset circuit
- Significant progress on study of microscopic defects to explain macroscopic behavior **(RD50)**
- **See G. Kramberger's presentation**

Sensor radiation tolerance



- Convergence for large fluences for different starting materials
- 1E14 => stay thin…

MONOLITHIC PIXEL DEVELOPMENT FOR ATLAS

- Concentrating on depleted MAPS for radiation tolerance
- Large effort on many technologies : AMS 350 nm, **AMS 180nm**, **Lfoundry 150 nm**, Global Foundry 130 nm, ESPROS 150 nm, **TowerJazz 180 nm**, IBM T3 130 nm, STM 180 nm, ON Semi 180 nm, SOI XFAB 180 nm

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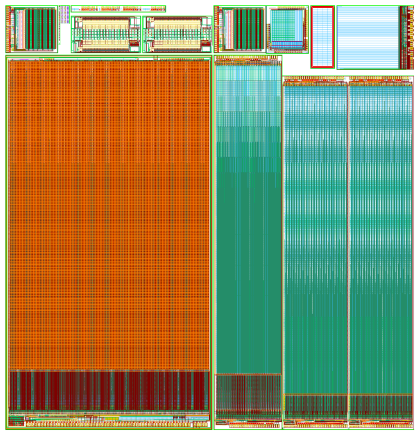
Large chips become available in several technologies

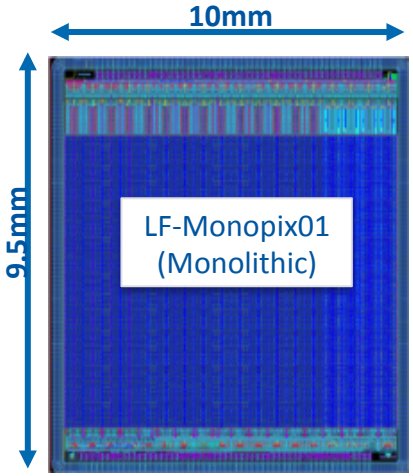
Chip name	Technology	CE Size*	Pixel size [µm²]	R/O architecture	Staust
aH18	AMS 180nm	Large	56 × 56	Asynchronous	Measurements
Malta	TowerJazz 180nm	Small	36 × 36	Asynchronous	Submitted Back after Xmas
TJ Monopix		Small	36 × 40	Synchronous	
LF Monopix	LFoundry 150 nm	Large	50 × 250	Synchronous	Measurements
Coolpix		Large	50 × 250	Synchronous	
LF2		Large	50 × 50	Synchronous	

* CE Size = Collection Electrode Size



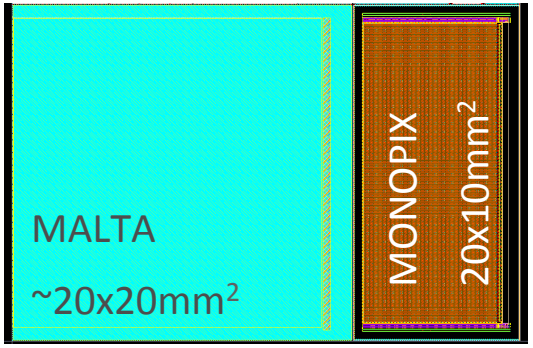
ATLAS Pix & MuPix

AMS 180 nm



MONOPIX, LF2 & COOLPIX

Lfoundry 150 nm



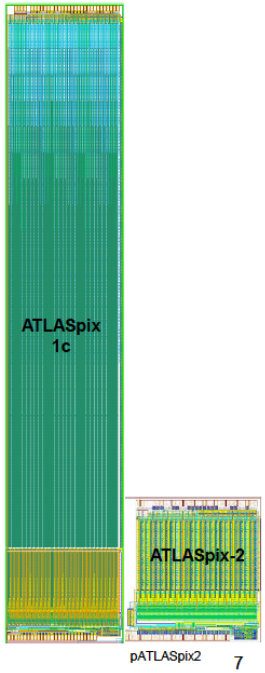
MONOPIX & MALTA

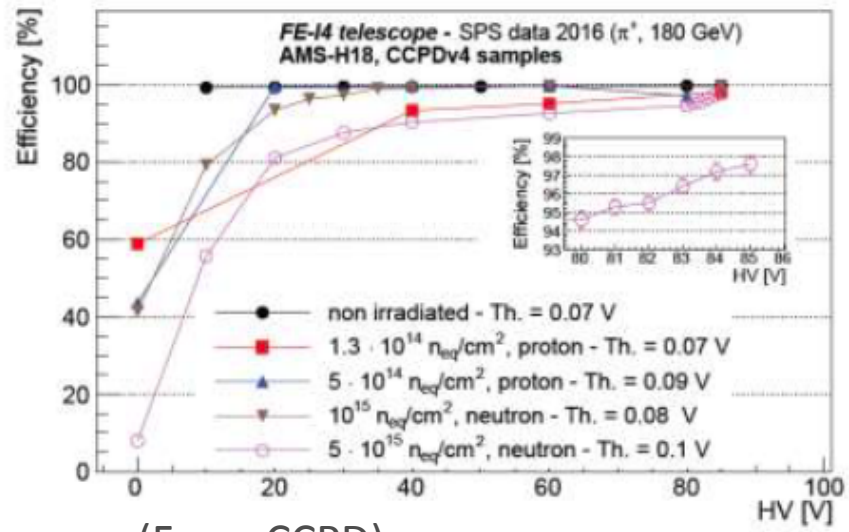
TowerJazz 180 nm

AMS 180nm

ATLASpix-1 Vs ATLASpix-2

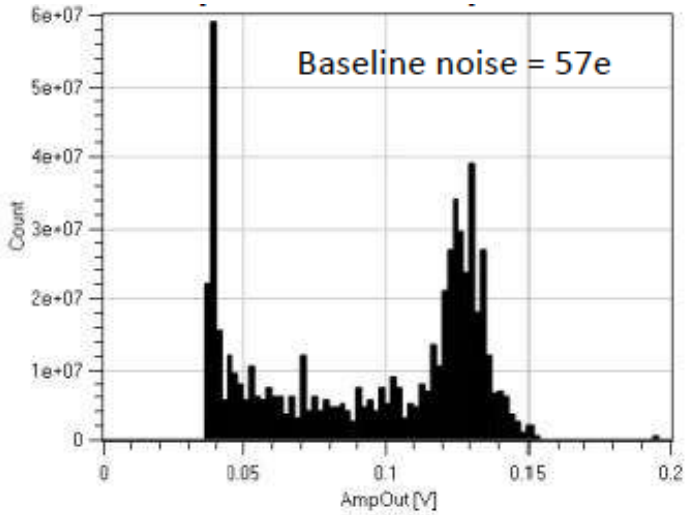
Feature	ATLASpix-1c	ATLASpix-2
Submission	January 2017	August 2017
Pixel size	60μmx50μm	128μmx50μm
Matrix size	56x320	24x36
Pixel grouping	8-bit address compression for 16 pixels in a group sharing 4 buffers	A dedicated bit to store hit information for 12 pixels in a group sharing 4 buffers
Readout scheme	Parallel pixel to buffer readout	Parallel pixel to buffer readout
Sorting of Hits	Unsorted hits	Sorting Enabled
Time over threshold	Not ToT information	6 bit ToT information
Time walk correction	X	Neighbor logic
SEU tolerance	No SEU tolerant memory	Uses SEU tolerant pixel memory
Data encoding in Digital control unit	8 to 10 bit pipelined encoder	Standard Aurora 8 to 10 bit transmitter





(From CCPD)

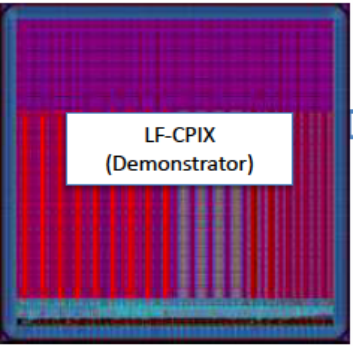
Arxiv : 1611.02669

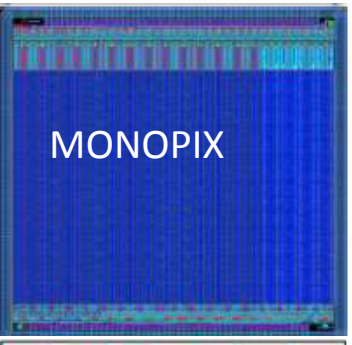


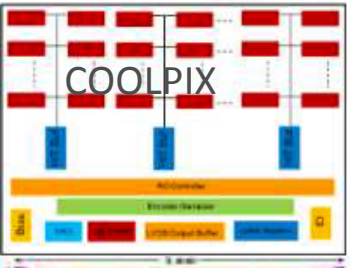
- High detection efficiency above 1E15 n_{eq}/cm^2
- Large pixel prototype (ATLASPIX being measured now)
- New ATLASPIX submitted

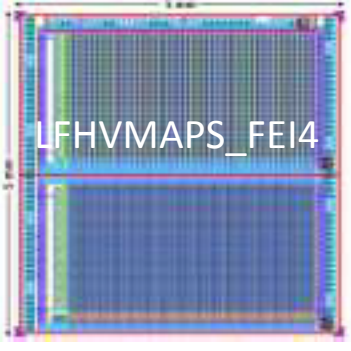
See I. Peric's presentation

Lfoundry 150nm

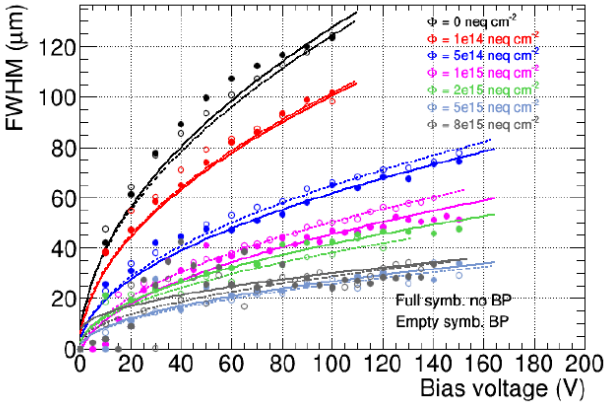






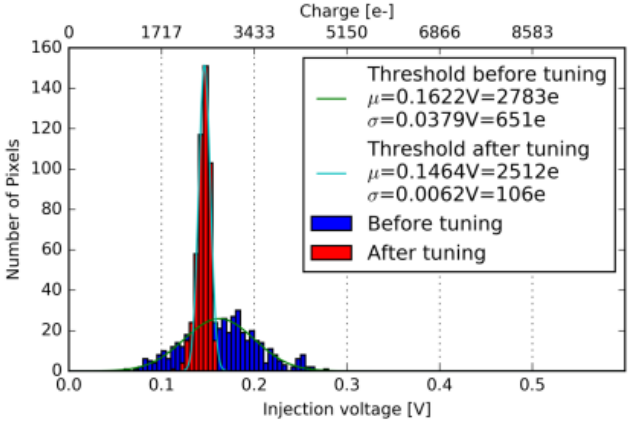


Depletion depth



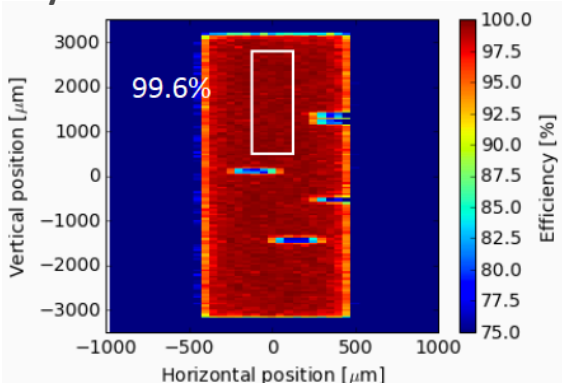
I. Mandic et al 2017 JINST 12 P02021

Threshold dispersion of MONOPIX

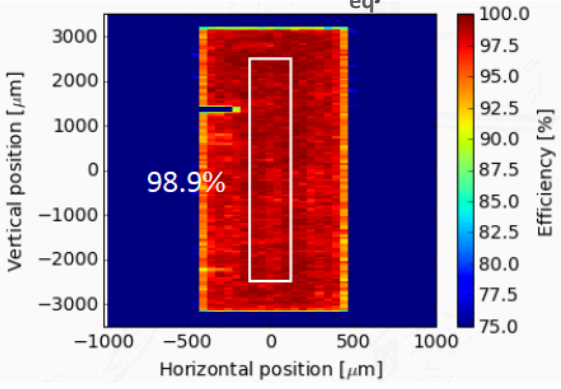


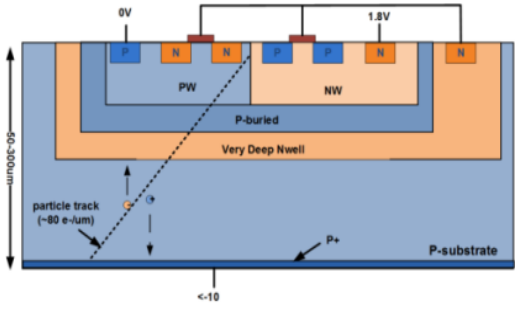
I. Caicedo, IEEE 2017

Efficiency non-irradiated



after 1.14 E15 n_{eq}/cm^2

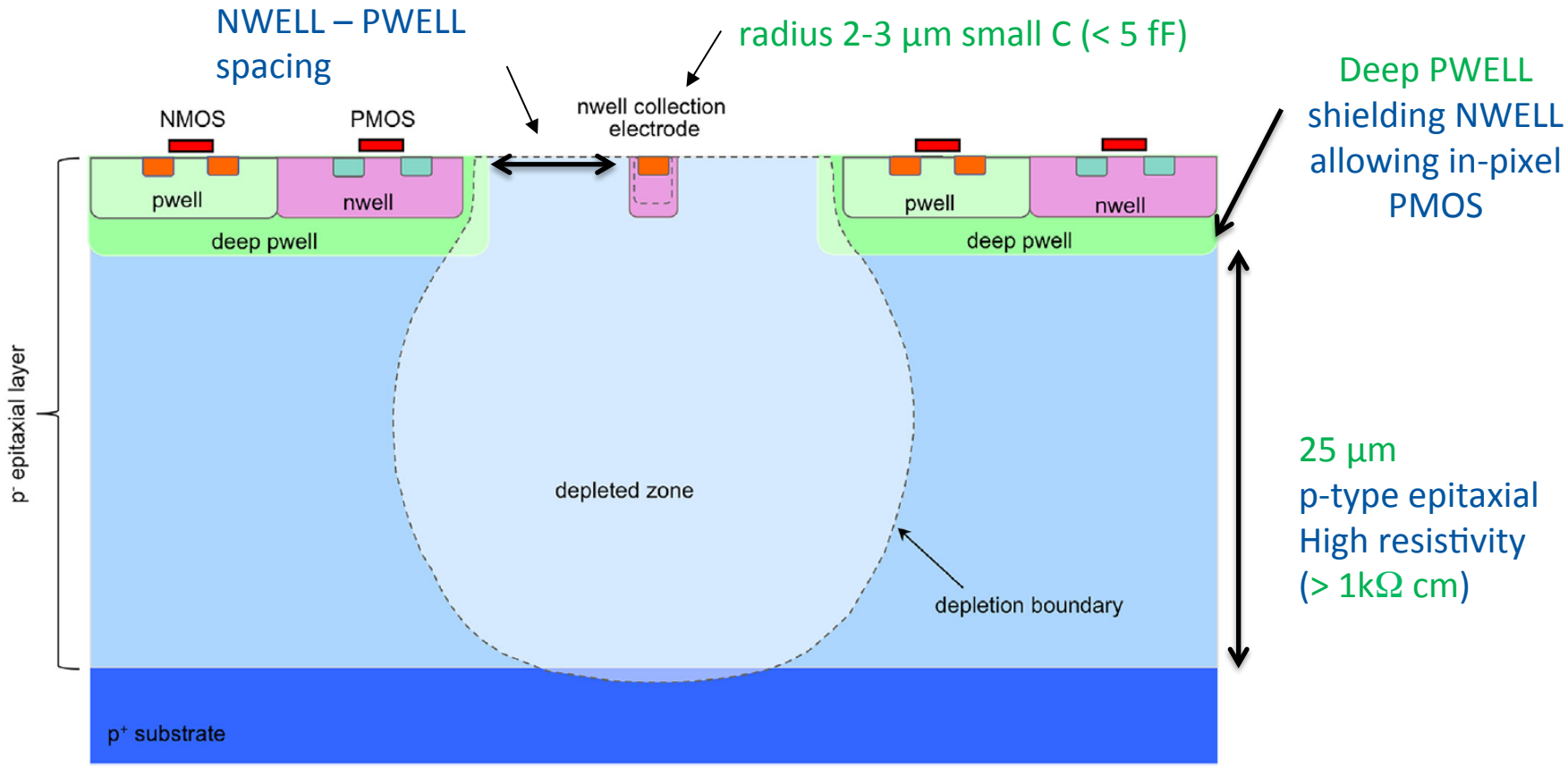




See T. Hirono's presentation

Standard TowerJazz 180 nm CMOS process

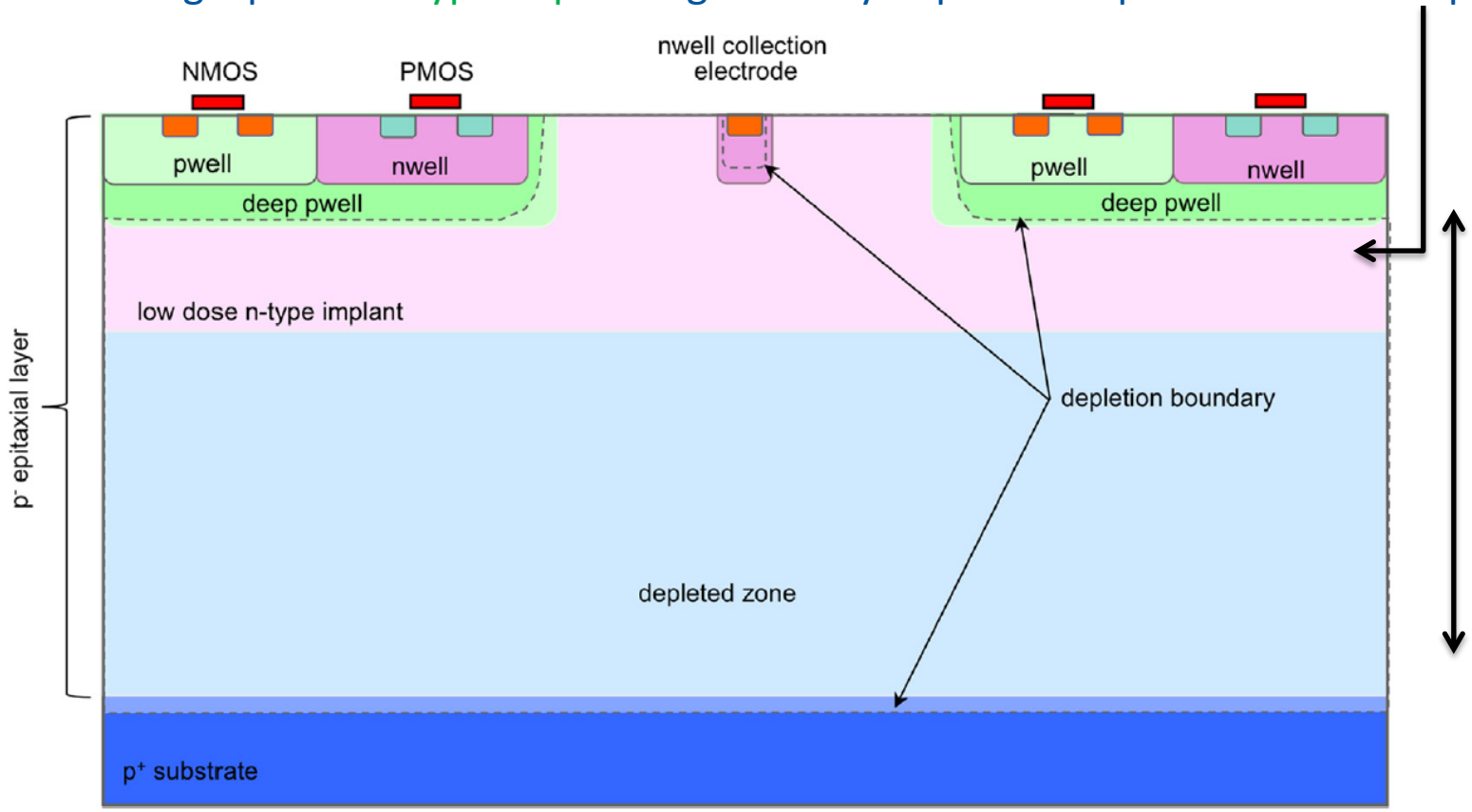
- 180nm CMOS imaging sensor process
- Electronics outside the collection electrode: small electrode (low C), large circuit area, no signal coupling



- Reverse bias to increase depletion volume (-6 V, the sensor is not fully depleted)

Modified process

- Novel modified process developed in collaboration with the foundry
- Adding a planar n-type implant significantly improves depletion under deep PWELL



25 µm
p-type epitaxial
High resistivity
(> 1kΩ cm)

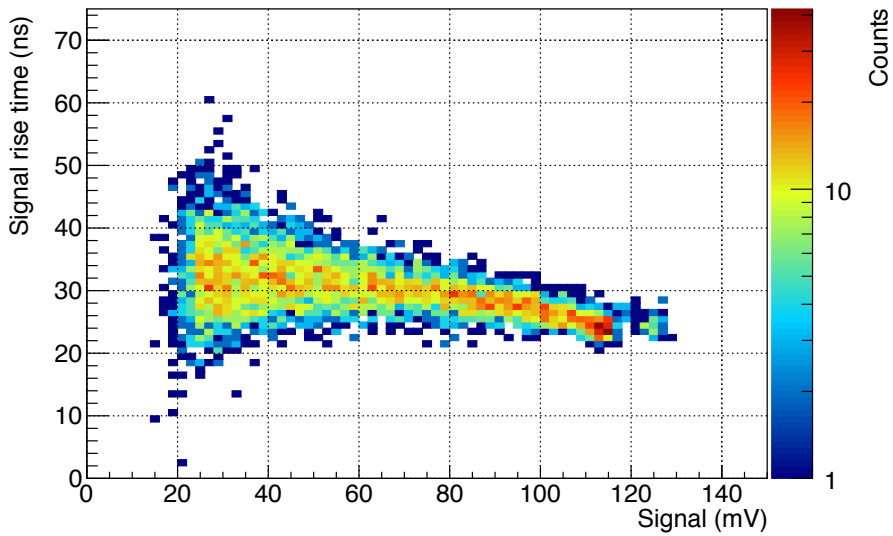
DOI 10.1016/j.nima.2017.07.046

- Possibility to fully deplete sensing volume
- No significant circuit or layout changes required

^{55}Fe measurements before irradiation

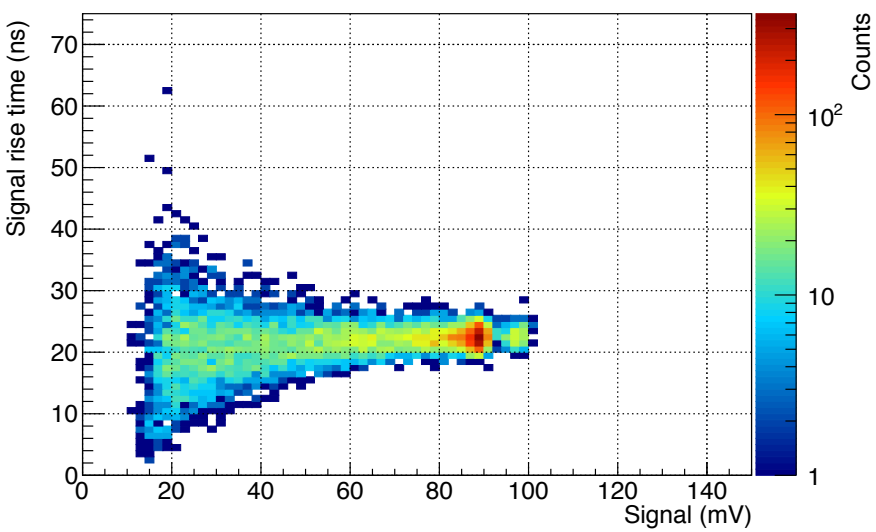
J. Van Hoorne

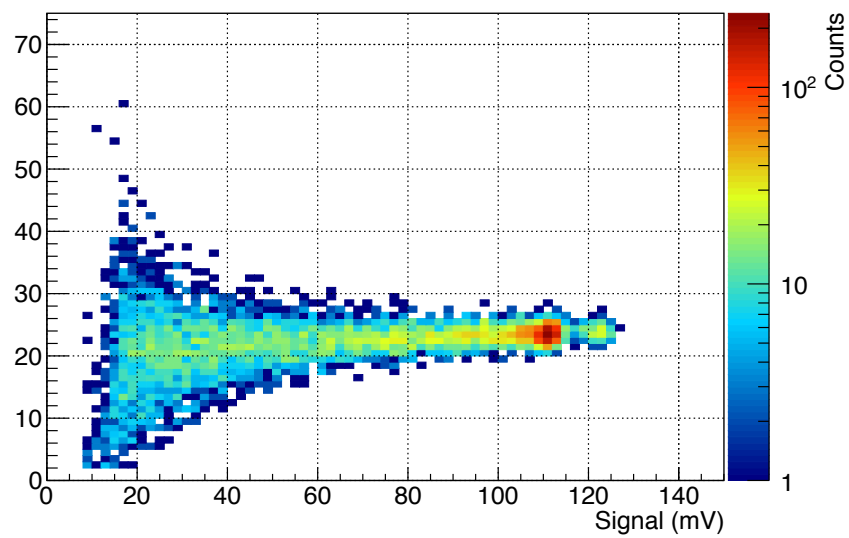
Standard process



Note: circuit contributes significantly to the signal rise time !

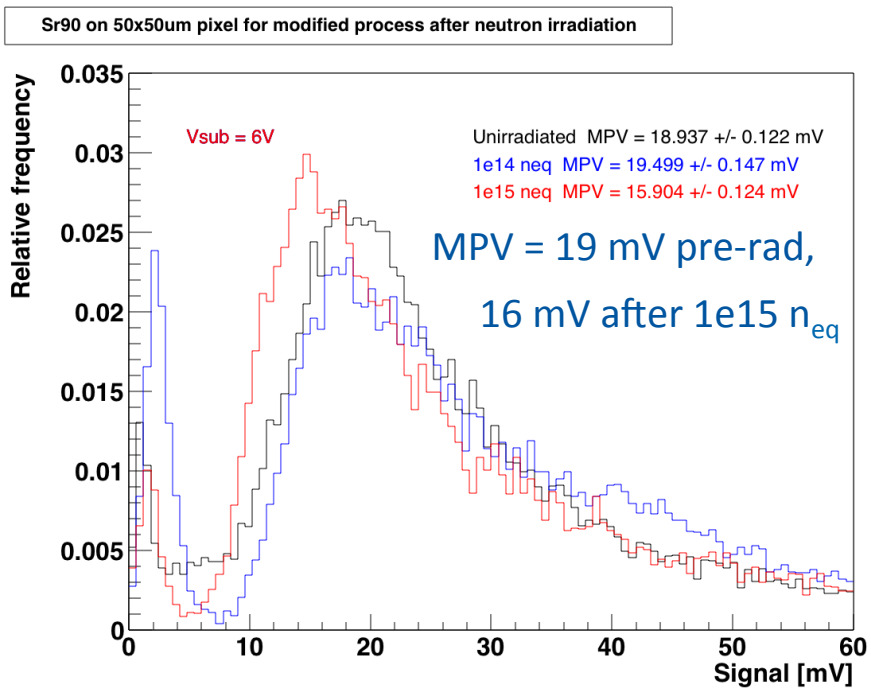
Modified process

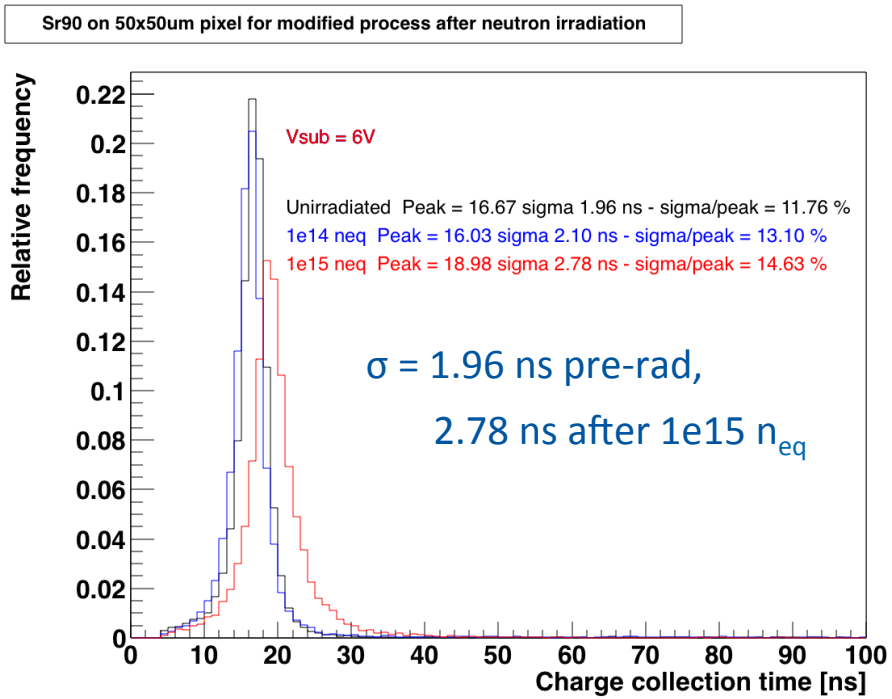




much less charge spread over different pixels and much more uniform in time response

Measurement results after irradiation





Encouraging results on detection efficiency after irradiation (1e15 n_{eq}/cm^2)

H. Pernegger et al 2017 JINST 12 P06008

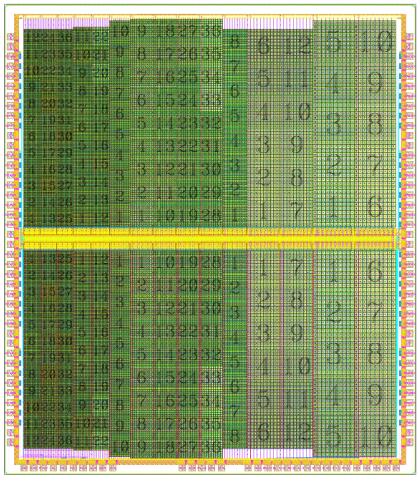
Initiated ATLAS ITK development involving several groups:

- Faster, smaller front end and faster on-chip data transmission
- Further system integration beyond chip-to-chip communication:
  serial power and on-chip sensor bias generation

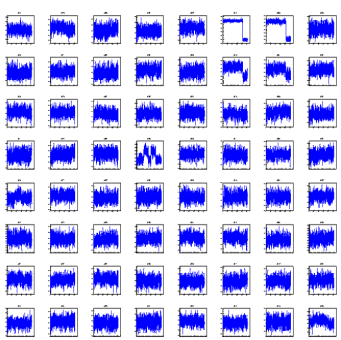
See H. Pernegger's presentation

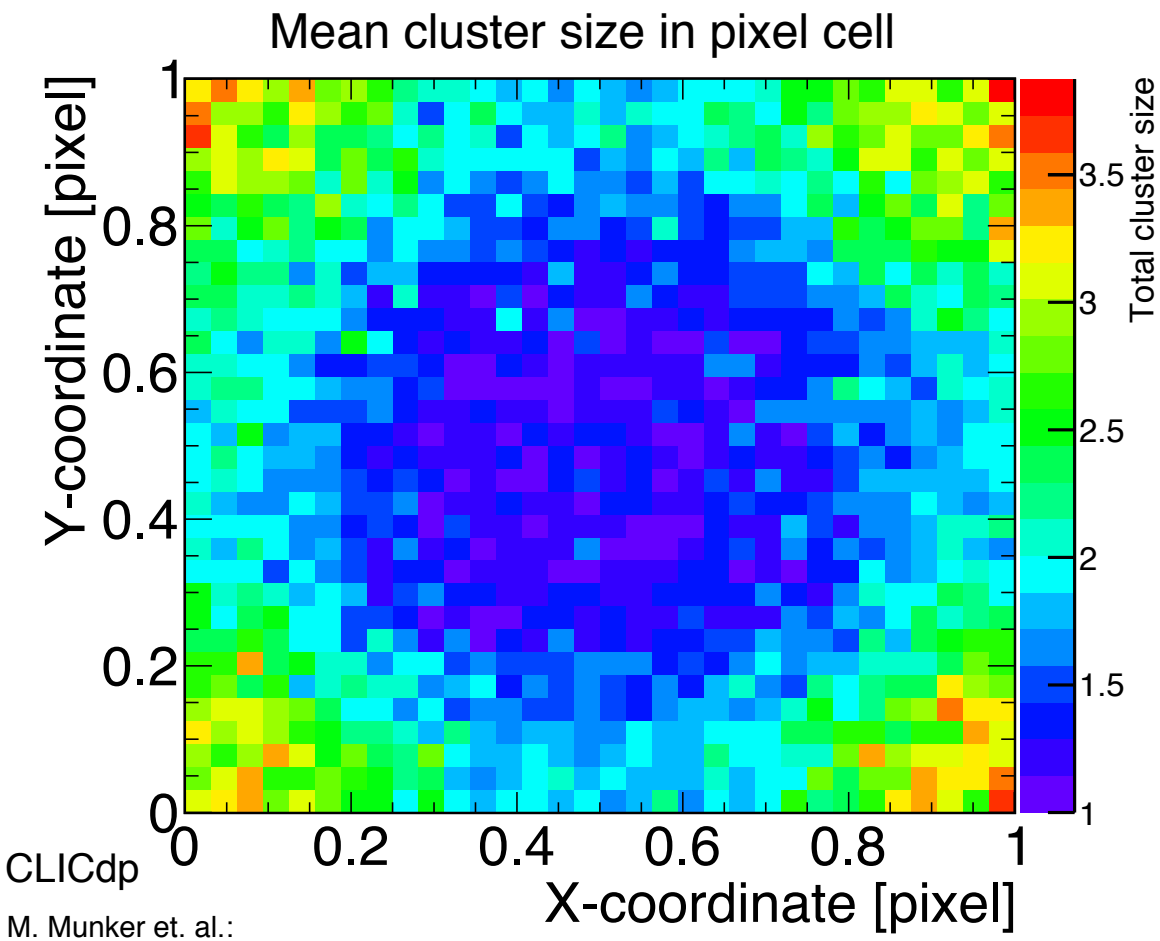
Investigator chip also measured by other groups (eg CLIC)

Investigator-1 layout



sub-matrix



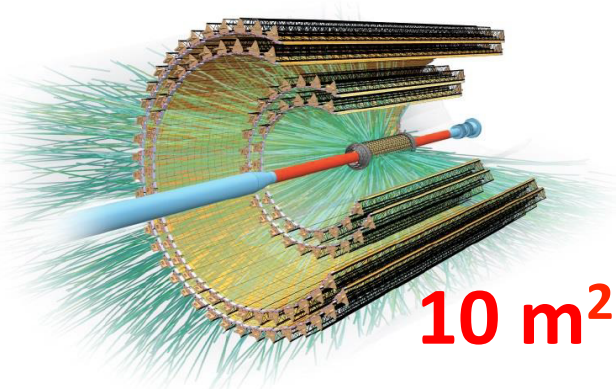


M. Munker et. al.:

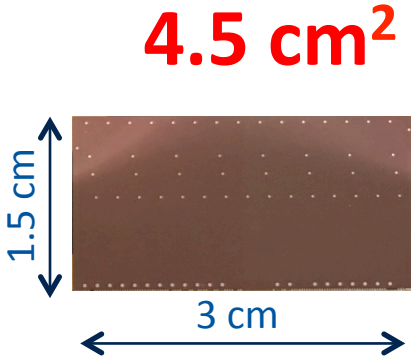
Study of the ALICE Investigator chip in view of the requirements at CLIC, CLICdp-Note-2017-004

See D. Dannheim's presentation

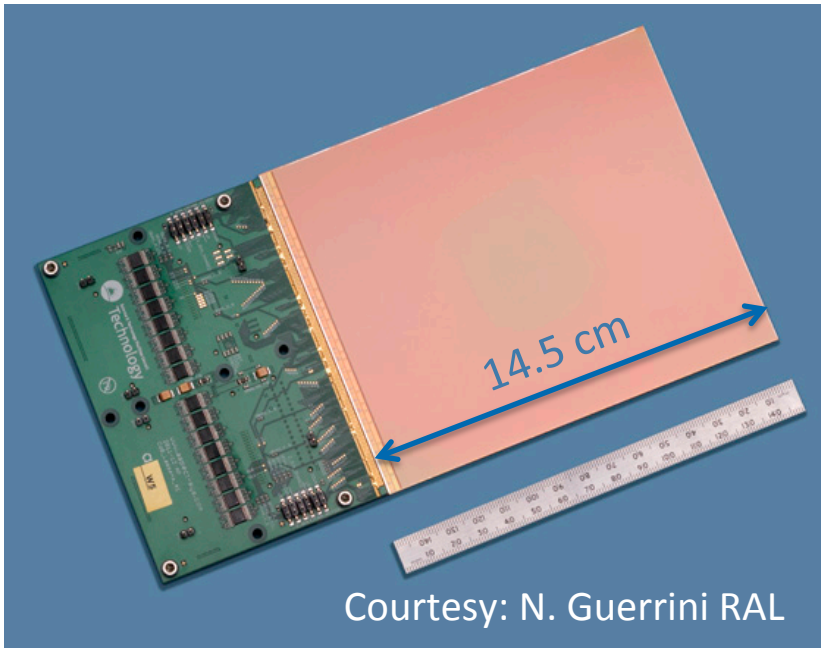
Waferscale integration



- 10 m^2 to 4.5 cm^2 ratio not ideal
- Need larger chips and new module assembly techniques



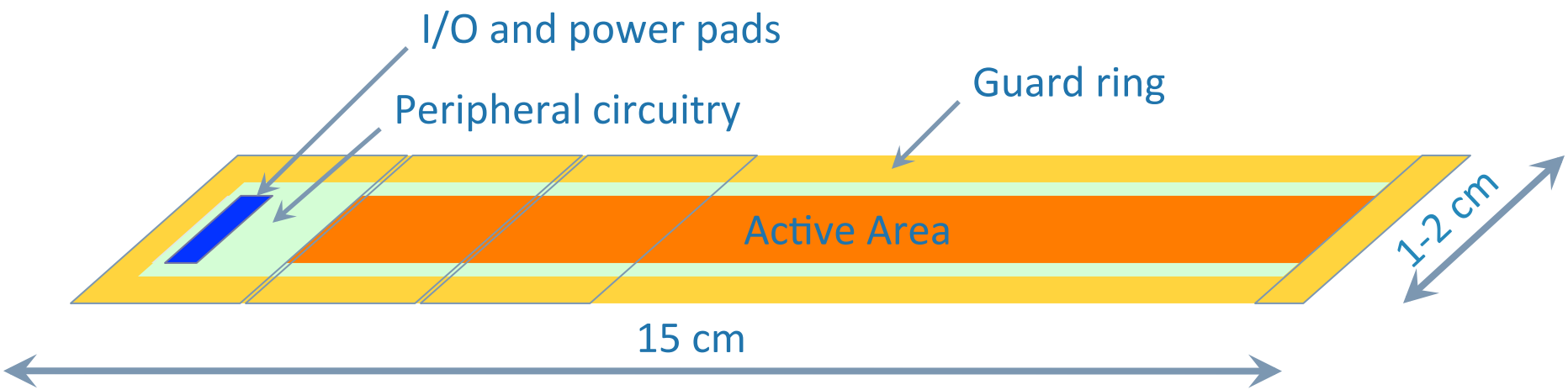
Waferscale integration for assembly of larger areas



Can we take advantage of flexible thin Si ?

Waferscale integration by stitching

In one dimension:



- Stitching is combining part of the reticle to obtain a chip with an area larger than the reticle (done for large professional CCDs for instance)
- All connections to the exterior on one side
- All routing using on-chip metal layers
- All local functions integrated

- Design issues: bias and voltage drops, long distance signal transport…

Waferscale integration: voltage drops

- Power supply drop is proportional to the square of the number of pixels in the column:

  R = resistance of one pixel, I = current consumption of one pixel

$$\Delta V = \sum_{k=1}^{N-1} R \sum_{l=k+1}^{N} I = RI \sum_{k=1}^{N-1} N - k = RI \sum_{k=1}^{N-1} k = \frac{N(N-1)}{2} RI$$

- For one full metal layer (80 mΩ/square), 10 µm x 10 µm pixel, 1 nA/pixel (!), 14 cm high column:

$$\Delta V = \frac{N(N-1)}{2} RI = \frac{14000^2}{2} 80m\Omega \times 1nA = 7.8\ mV$$

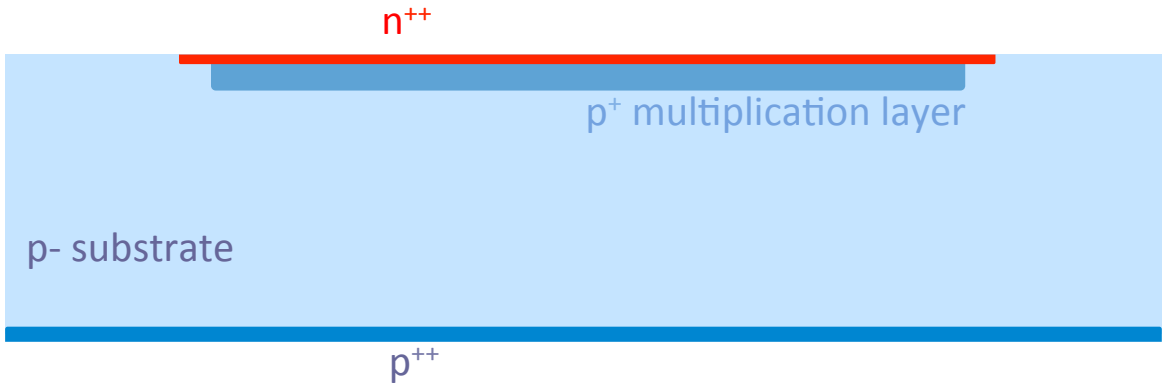
- Large chip with ALPIDE front end: (~20nA/pixel): 1.3 mV x $(14/1.37)^2$ = 136 mV

⇒ Biasing needs redesign, in weak inversion: I ~ exp(qV/nkT), nkT/q=40mV at roomT

⇒ Already now some measures needed/implemented for ATLAS development even for normally sized chips.

Timing as a 4th dimension

- Low Gain Avalanche Diodes (LGAD)



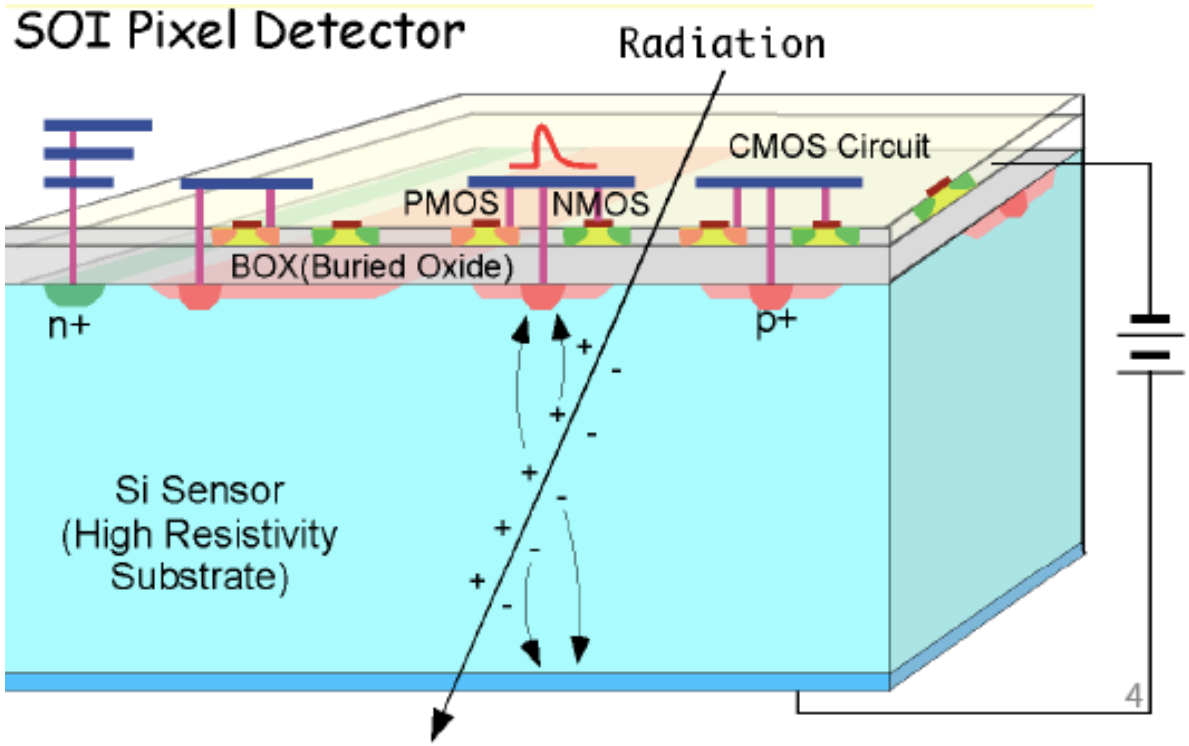
- Charge gain in Si, drastically increase slew rate
- Picosecond timing for thin detectors
- Radiation damage (acceptor removal), use Ga instead of B
- **See N. Cartiglia's presentation and LGAD session**

H. Sadrozinski et al.,NIM A730 (2013) 226-231, NIM A831 (2016) 18-23

N. Cartiglia et al. NIM A796 (2015) 141-148, NIM A845 (2017) 47-51

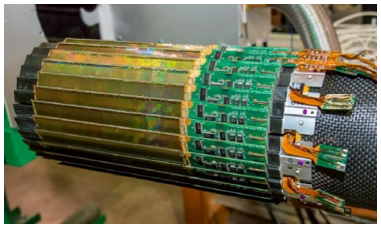
W. Riegler & G. Aglieri: 2017 JINST 12 P11017 "Time resolution of Si detectors"

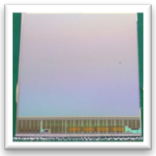
Silicon on Insulator (SOI)



- Very impressive technology developments … with excellent Q/C
- Some freedom on sensor material
- BOX causes reduced radiation tolerance, several measures for improvement
- **See Y. Arai's presentation and SOI presentations**

Monolithic CMOS sensors in HEP

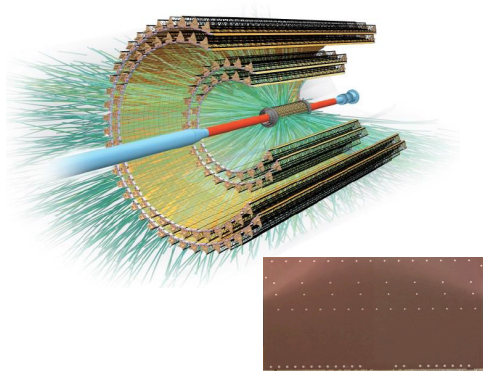




ULTIMATE in STAR

IPHC Strasbourg

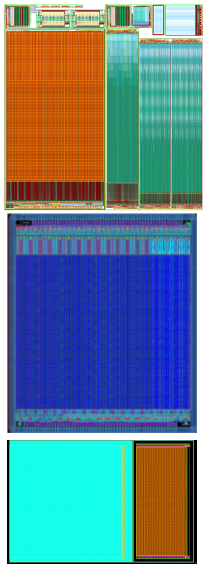
First HEP MAPS system



ALPIDE in ALICE

First MAPS with sparse readout similar to hybrid sensors

Chip-to-chip communication for data aggregation



ATLAS CMOS

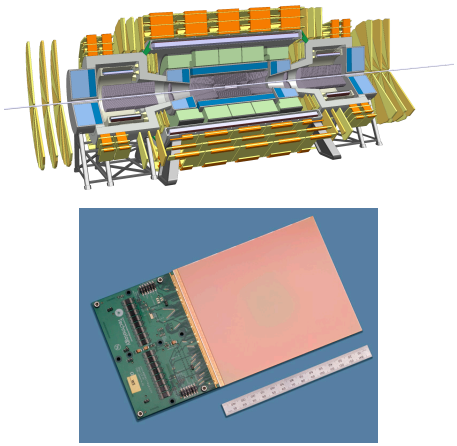
Depleted radiation hard MAPS with:

Sparse readout

Chip-to-chip communication

Serial power

…



FCC, CLIC, …

Large stitched fast radiation hard MAPS with:

Sparse readout

Chip-to-chip communication

Serial power

…

LGAD ?

Important steps in every iteration

Commercial deep submicron CMOS brought us:

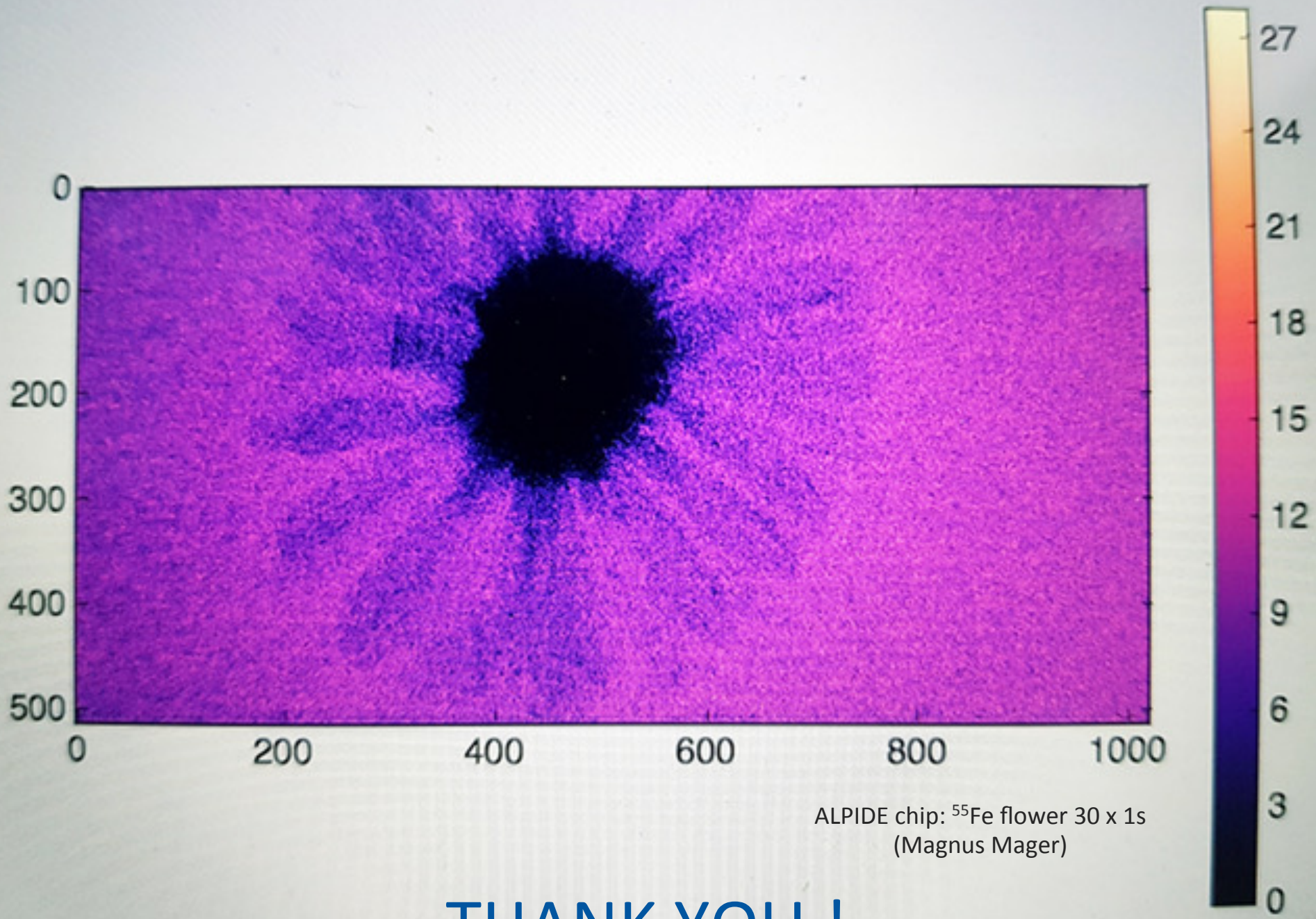
The circuit, the sensor, and radiation tolerance

Commercial deep submicron CMOS brought us:

The circuit, the sensor, and radiation tolerance

Deeper submicron should bring us:

- Waferscale sensors
- ~1 µm single point resolution
- Lower (close to zero?) analog and lower digital power
- Higher density and more metal layers
- Higher on and off-chip bandwidth
- (hopefully) even better radiation hardness



ALPIDE chip: ^{55}Fe flower 30 x 1s
(Magnus Mager)

THANK YOU !

Backup

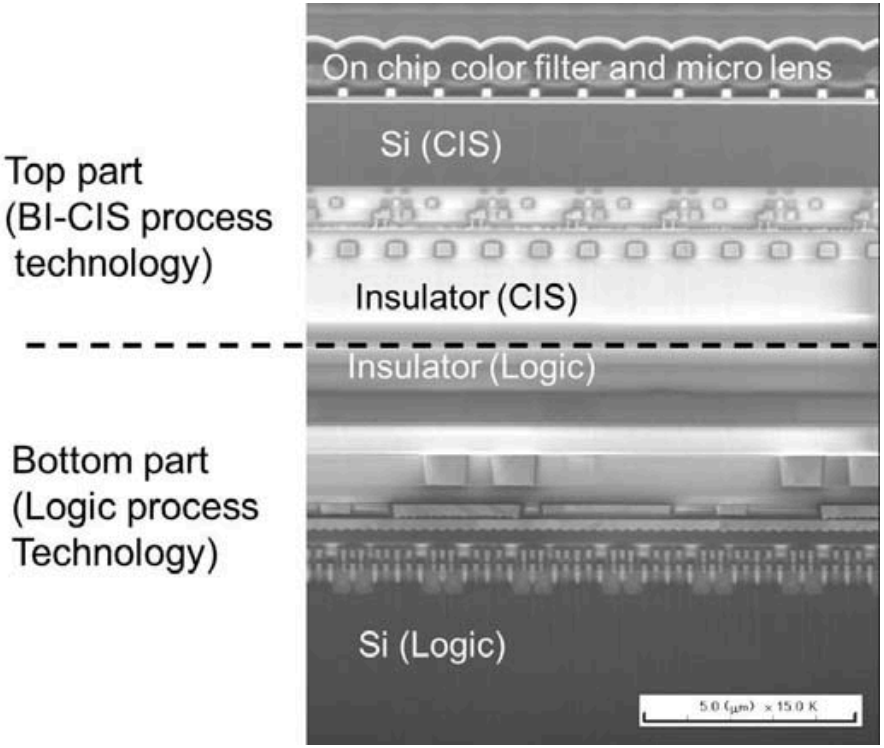
CMOS Monolithic Active Pixel Sensors

- CMOS MAPS have changed the imaging world, reaching:
  - less than 1 e^- noise

    (cfr S. Kawahito, PIXEL 2012)
  - > 40 Mpixels
  - Wafer scale integration
  - Wafer stacking
  - …

- In High Energy Physics silicon has become the standard in tracking applications both for sensor and readout

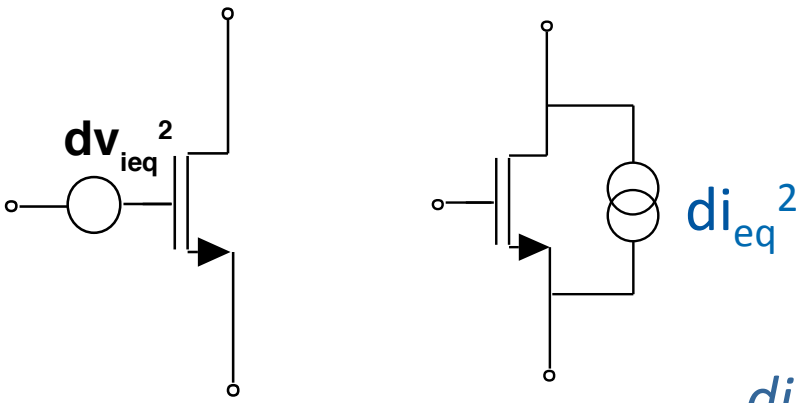
- … and now CMOS MAPS make their way in High Energy Physics !



Backside Illuminated 8M Pixel Stacked Imaging Sensor
S. Sugawa et al. Sony Corp.
ISSCC 2013

Analog Power Consumption:
Noise sources in a FET

EQUIVALENT WITH :



WHERE:

$$di_{eq}^2 = g_m^2 dv_{eq}^2$$

In weak inversion (WI): $g_m \sim I$

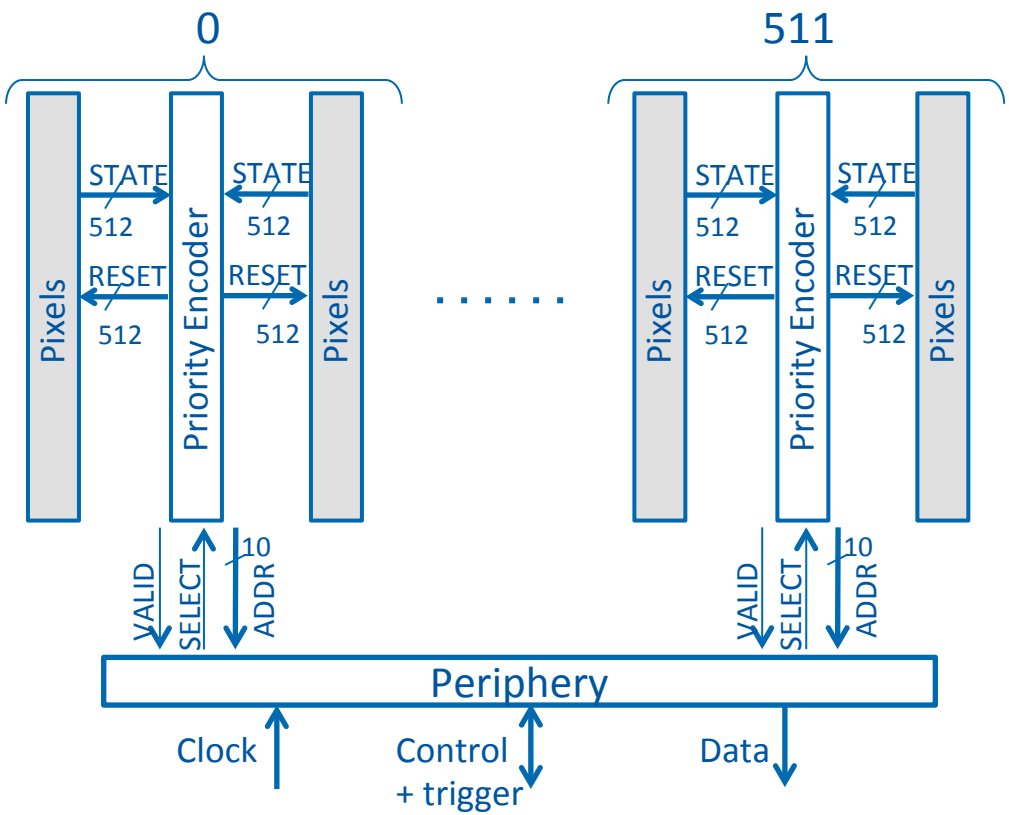
$$dv_{eq}^2 = (K_F/(WLCox^2 f^\alpha) + 2kTn/g_m)df$$

In strong inversion (SI) $g_m \sim \sqrt{I}$

$$dv_{eq}^2 = (K_F/(WLCox^2 f^\alpha) + 4kT\gamma/g_m)df$$

Transconductance gm related to power consumption

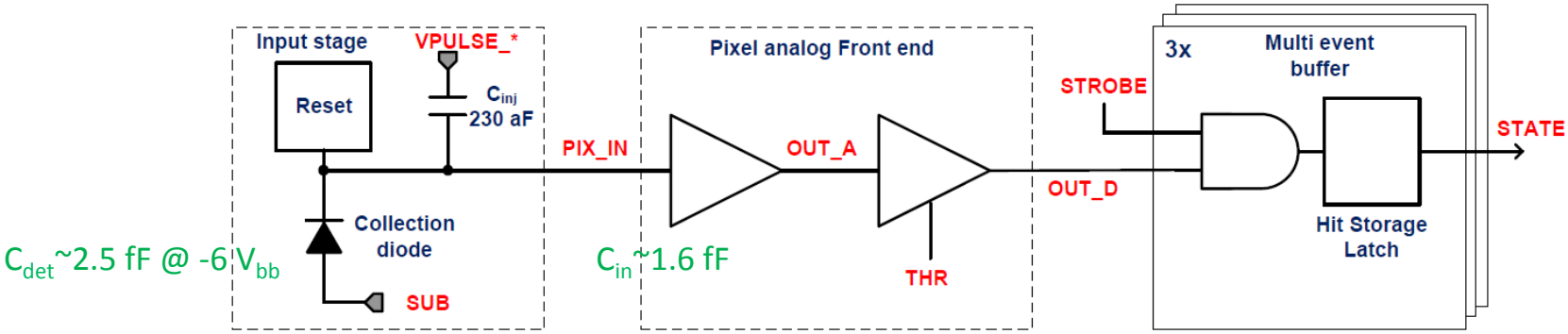
Matrix readout

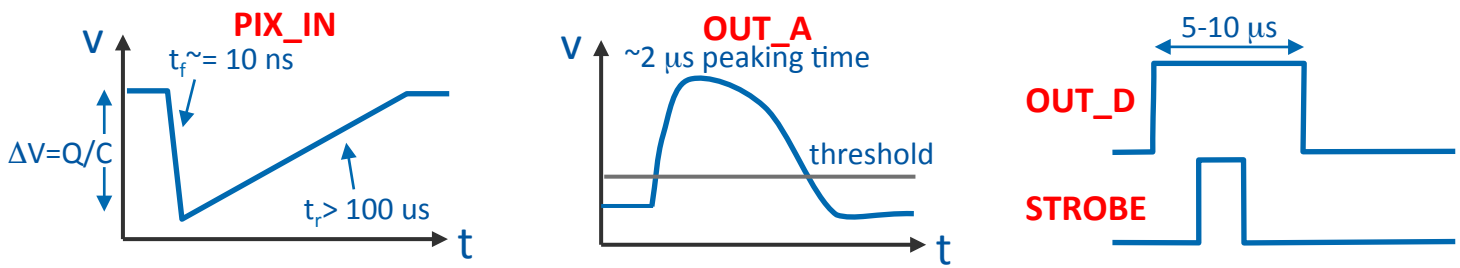


The Priority Encoder sequentially provides the addresses of all hit pixels in a double column

- Combinatorial digital circuit steered by peripheral sequential circuits during readout of a frame
- No free running clock over matrix. No activity if there are no hits
- Energy per hit: E_h ~= 100 pJ -> ~3 mW for nominal occupancy and readout rate
- Buffering and distribution of global signals (STROBE, MEMSEL, PIXEL RESET)

Pixel





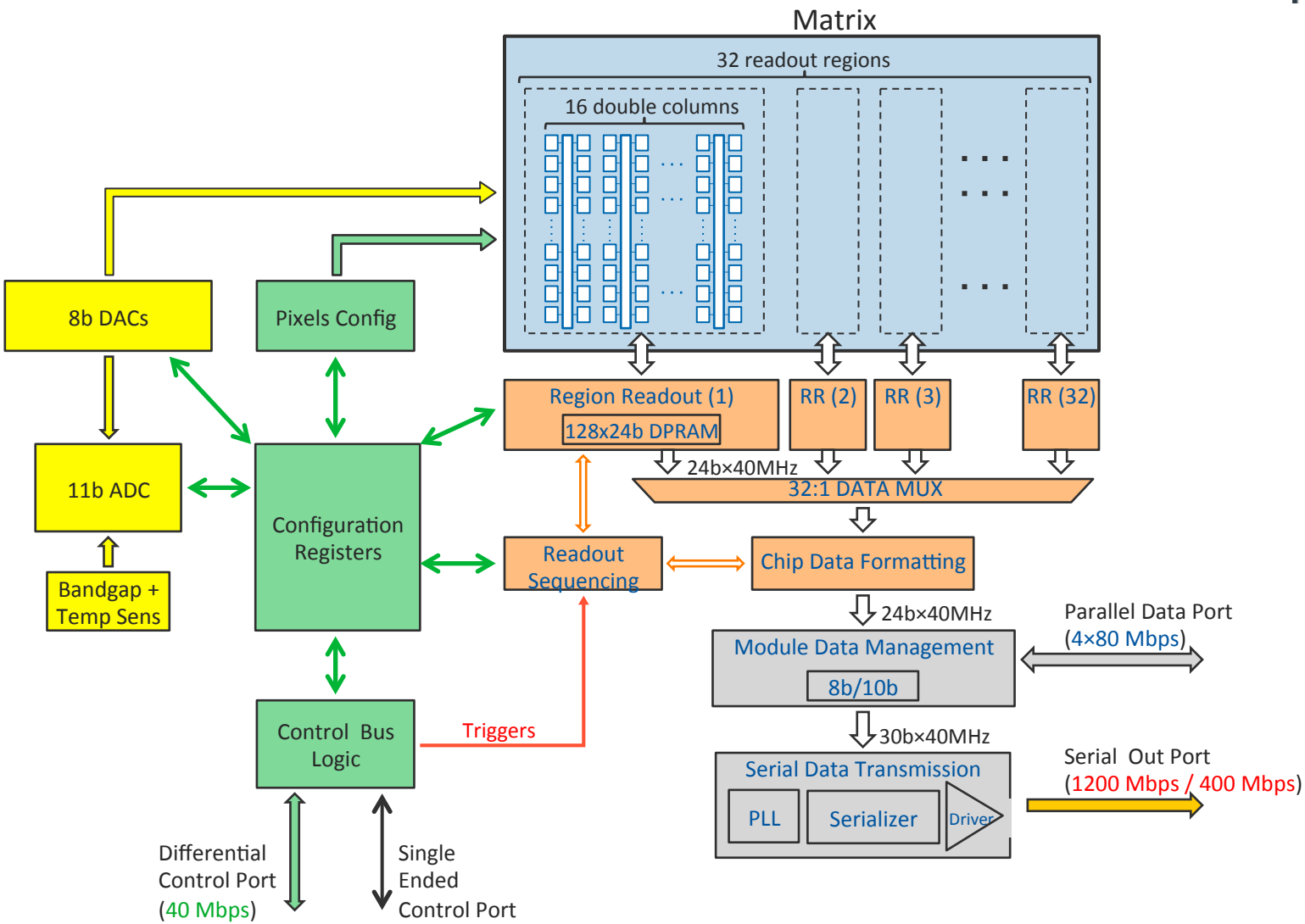
Analog front-end and discriminator continuously active

- Non-linear and operating in weak inversion. Ultra-low power: 40 nW/pixel
- The front-end acts as analogue delay line
- Test pulse charge injection circuitry
- Global threshold for discrimination -> binary pulse OUT_D

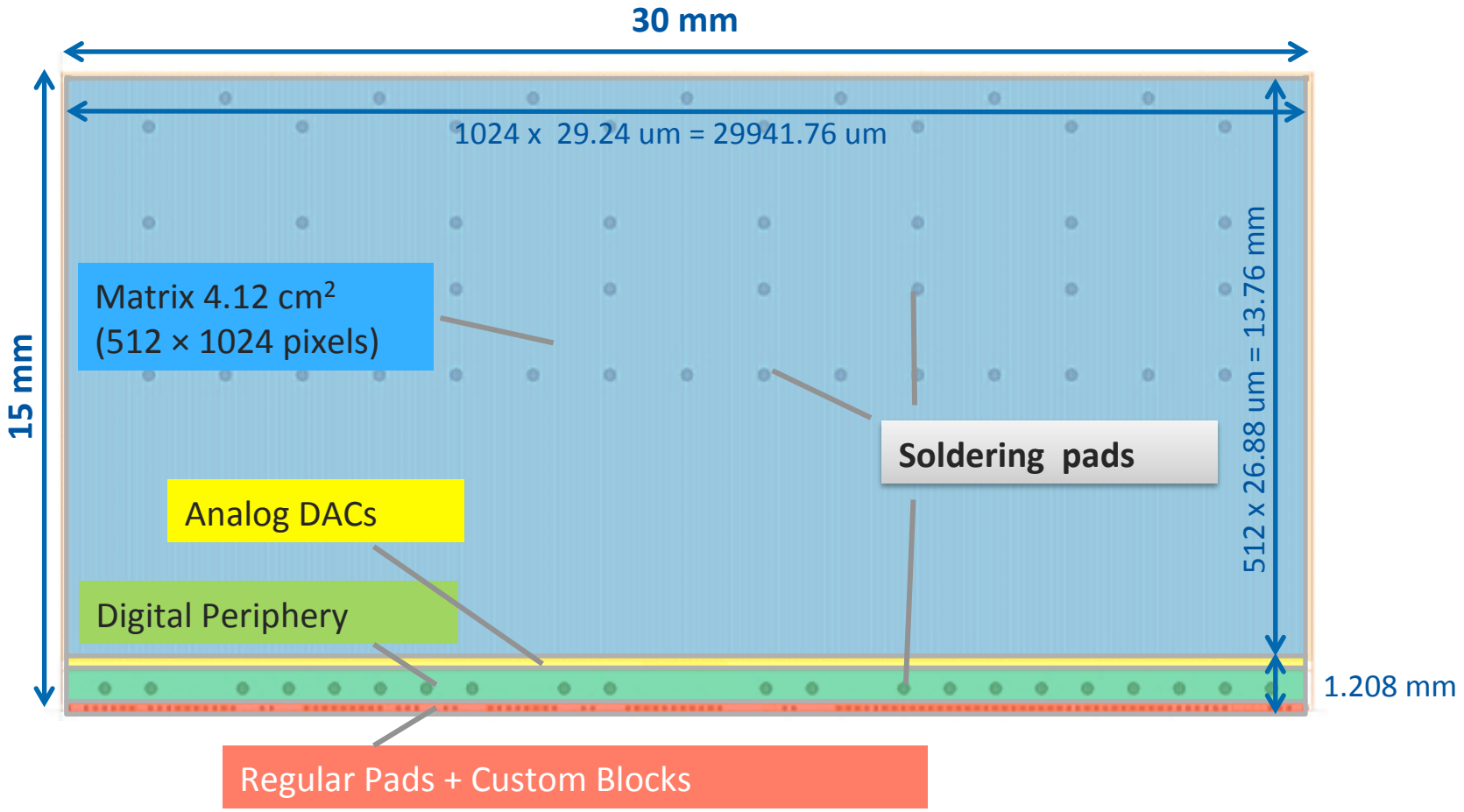
Digital pixel circuitry with three hit storage registers (multi event buffer)

- Global shutter (STROBE) latches the discriminated hits in next available register
- In-Pixel *masking* logic

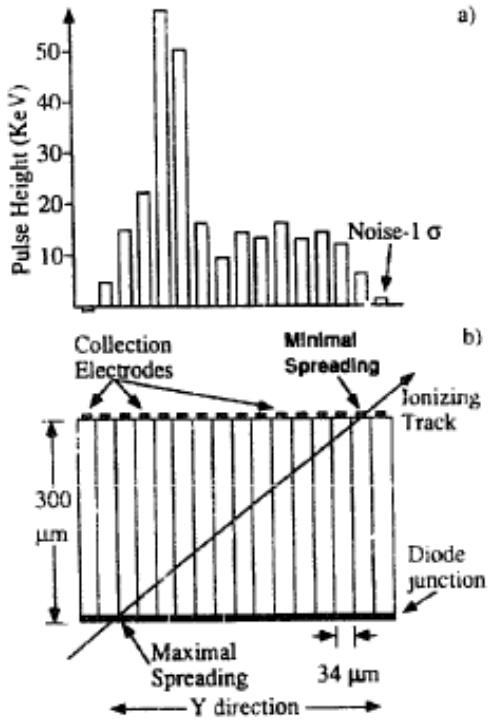
ALPIDE Readout and Control Features

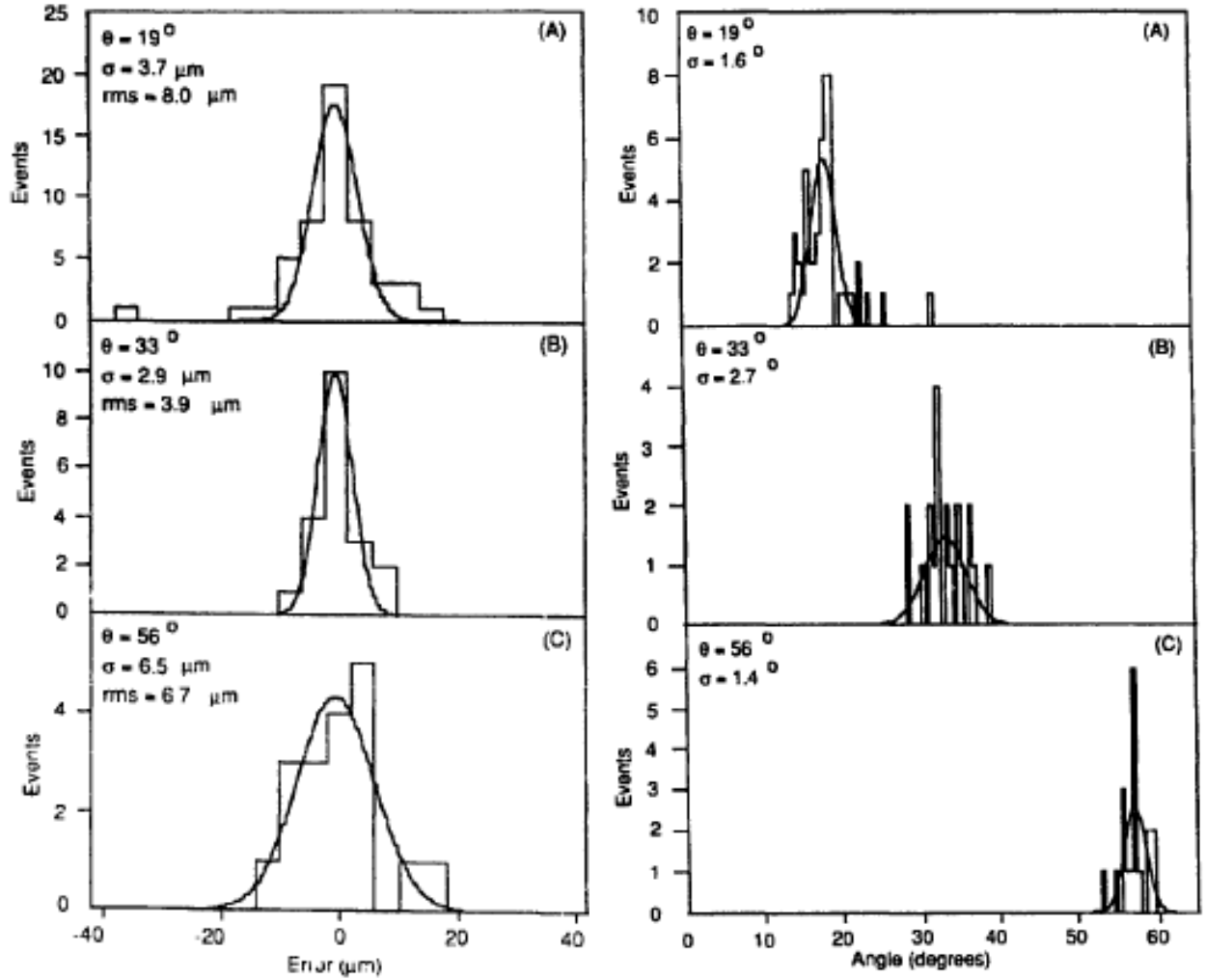


ALPIDE Floorplan



Point resolution: inclined tracks

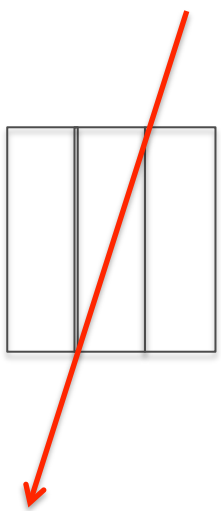


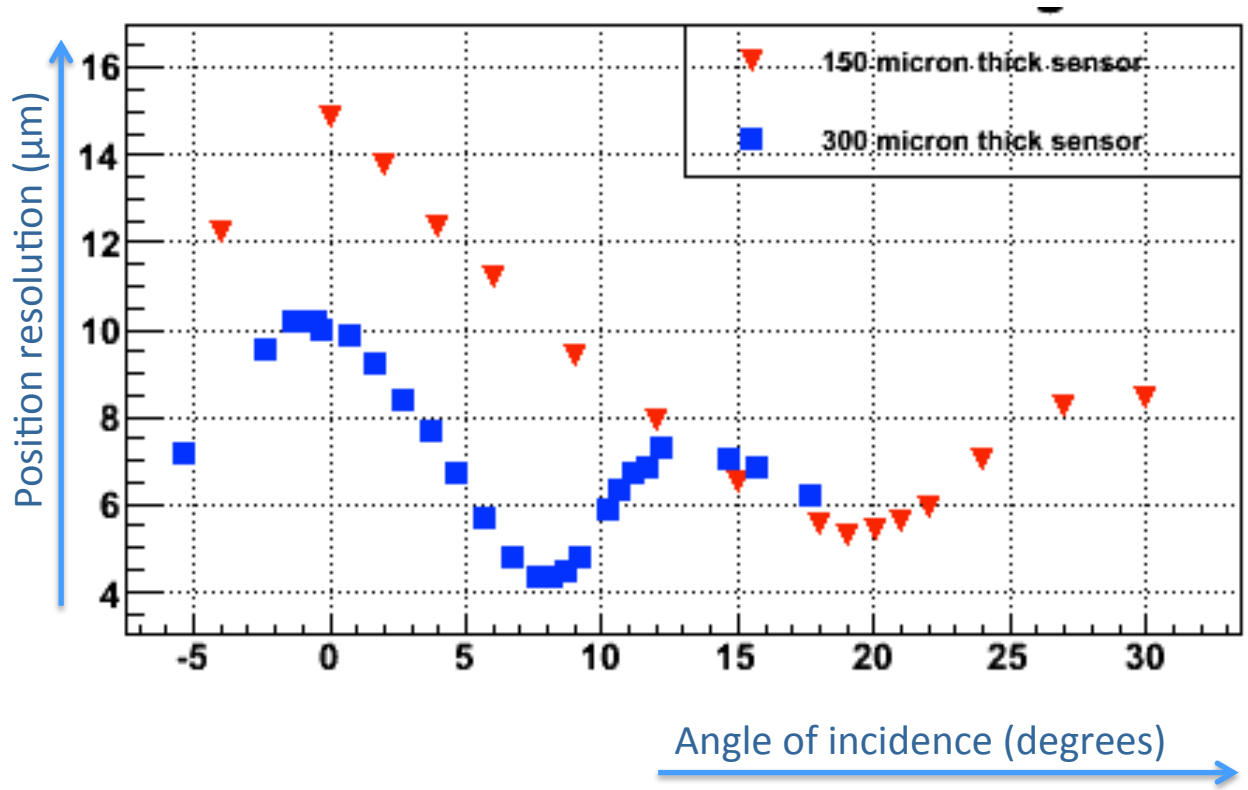


Average of extreme pixels in the cluster gives better results
In this case signal (and S/N) for a single channel reduces with track inclination

C. Kenney et al. NIM A (1994) 258-265

Point resolution: inclined tracks





Can optimize resolution using track inclination, enhance charge sharing

Timepix3: X. Llopart, J. Buytaert, M. Campbell et al.

A too simple simulation

~ 300mV at input with

2 nA total standby current

(1nA in input transistor)

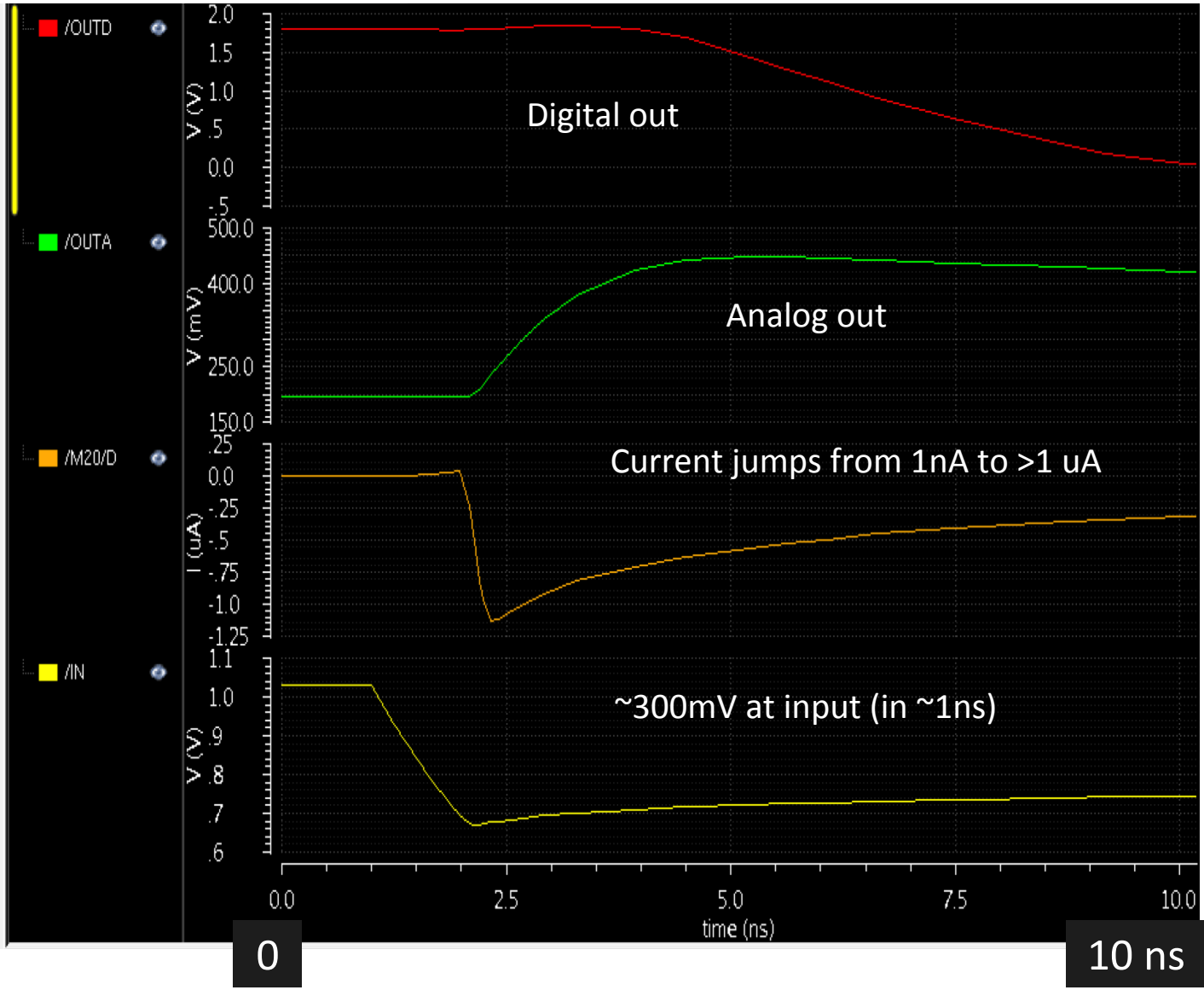
=>

Just to demonstrate that very large Q/C

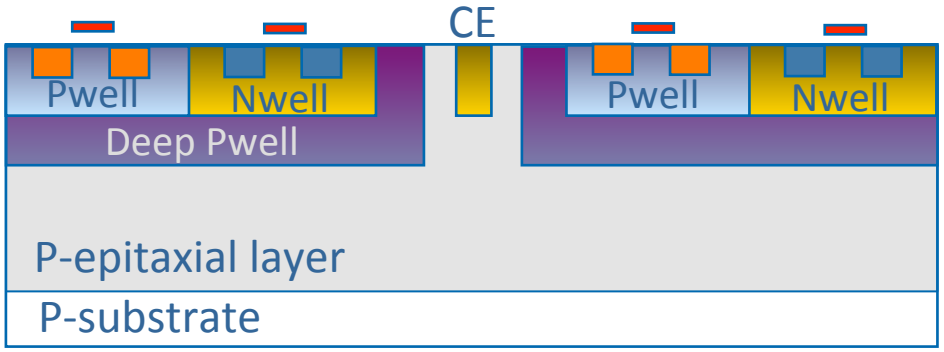
offers speed and low standby current…

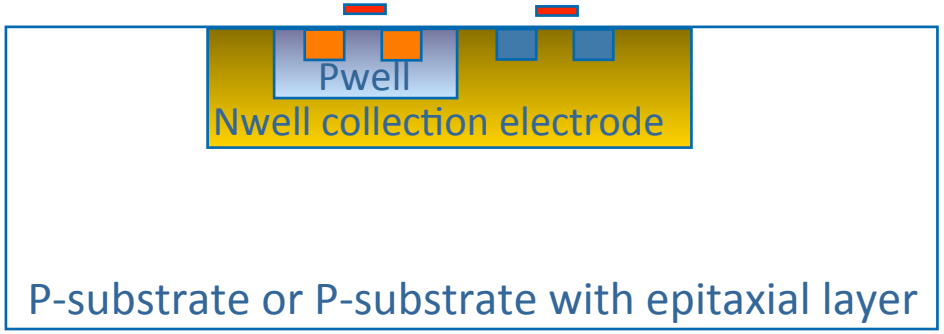
1nA/pixel = 1mA/cm²

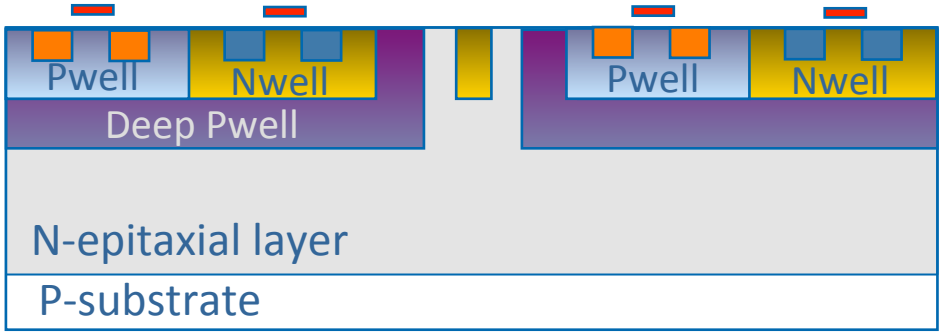
for 10µm x 10µm pixel



Full depletion and high Q/C







Junction on the front

- Deep pwell shields nwell from epi
- AC coupling between CE and circuit allows higher reverse bias (PEGASUS Bonn/IPHC)
- Either simple in-pixel circuit or large collection electrode for full depletion
- ALICE 2.5 fF but no full depletion

Circuit inside collection electrode

(ATLAS AMS 180 nm & LF 150nm, CLIC, LePIX)

- Depletion easier, risk of coupling into input
- Keep in-pixel circuit simple for low C, or use it as smart detector in hybrid solution
- Difficult to go below 10's of fF

Junction on the back or deeper into silicon

- Full depletion with very small collection electrode and potentially very low C
- Example: Change epilayer type (RAL) or TJ modified process (ALICE, ATLAS)

Synchronous vs Asynchronous: matrix power

- Assumptions: Matrix 2 cm x 2 cm
- Analog Power < 75 mW/cm^2 (36.4 µm x 36.4 µm pixel)
- Power for clock distribution (needed for synchronous design)
  - Energy per 1 cm toggled line at 1.8 V = 2 pF/cm x (1.8 V)^2 = 6.5 pJ
  - 137 lines per cm (1 per double column) for 36.4 µm pixel pitch:

    137 x 6.5 pJ x 40 MHz = 36 mW/cm^2 (in MONOPIX ~2x differential lines)

- Power for matrix readout (MALTA)

	pixel hit rate		Power/bit/cm^2 (H=2 cm)	Power (4.5 bit toggling)
Layer	hit/BC/mm^2	Mhit/mm^2/s	mW/cm^2	mW/cm^2
0	0.68	27.2	17.7	79.6
1	0.21	8.4	5.5	24.6
2	0.043	1.72	1.1	5.0
3	0.029	1.16	0.8	3.4
4	0.021	0.84	0.5	2.5

- Asynchronous much larger bandwidth

Note : need to add periphery power !!