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[Invited] Cryogenic Power Electronics for Superconducting Power Systems

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Fully superconducting power systems in electric aircraft and all-electric ships will have many power conversion and conditioning stages between the generators, transmission cables, storage devices, and loads such as motors. The system level efficiency suffers from heat leak from ambient if the power has to leave the cryogenic environment of a superconducting device for power conversion and conditioning before entering a second superconducting device. A substantial share of the total heat leak is located at the interfaces between cryogenic devices and room temperature devices. It is, therefore, an important goal to minimize the number of non-cryogenic power devices and cryogenic to normal interfaces.

To increase the system-level efficiency, simpler designs, and to increase reliability, power electronic converters operating at cryogenic temperatures are needed. Besides minimizing the heat loads at the interfaces, cryogenic power electronics can offer other benefits such as higher power density and simpler integration of various devices. However, there are several obstacles to overcome before cryogenic power electronics technology reach maturity. While semiconductors and small power electronic devices have been studied at cryogenic temperatures and certain topologies have been identified as promising candidates for cryogenic power electronics, their packaging, interconnects, dielectric aspects, and cooling protocols are still areas of active and much needed research. The topology of the converter has to take into account the limitations and the efficiencies associated with the individual components at cryogenic temperatures. One example is the matrix converter topology, which does not require a DC link capacitor and therefore limits the risk with respect to the need for large cryogenic capacitors.

This paper presents the opportunities and challenges of cryogenic power electronic systems and the results of our attempts in developing suitable topologies and address system and device level issues related to cryogenic thermal and dielectric aspects.

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