Digital Readout for Cryogenic Detectors using Superconductor Integrated Circuits

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Objectives

- Superconductor fast digitizers and low-power logic are well suited for sensor array readout, enabling precise pulse timing and digital multiplexing.

- We can do both
  - Digital time-division multiplexing
  - Time-of-arrival measurements
Digital Time-Division Multiplexing Readout Circuit for Sensor Arrays
Block Diagram

\[ f_C = f_S = \frac{f_C}{2^8} \]
\[ f_P = \frac{f_C}{2^{10}} = \frac{f_S}{2^2} \]
\[ f_R = \frac{f_C}{2^5} = 2^3 f_S \]
Signal Variations at each Channels

<table>
<thead>
<tr>
<th>CHANNEL NAME</th>
<th>SIGNAL NAME</th>
<th>TEST PATTERN 1</th>
<th>TEST PATTERN 2</th>
<th>TEST PATTERN 3</th>
</tr>
</thead>
<tbody>
<tr>
<td>CH1</td>
<td>SIG1</td>
<td>$f_c$</td>
<td>$f_c/2$</td>
<td>NO SIG</td>
</tr>
<tr>
<td>CH2</td>
<td>SIG2</td>
<td>$f_c/8$</td>
<td>$f_c/2$</td>
<td>NO SIG</td>
</tr>
<tr>
<td>CH3</td>
<td>SIG3</td>
<td>$f_c/4$</td>
<td>$f_c/2$</td>
<td>NO SIG</td>
</tr>
<tr>
<td>CH4</td>
<td>SIG4</td>
<td>$f_c/2$</td>
<td>$f_c/2$</td>
<td>NO SIG</td>
</tr>
</tbody>
</table>
Design Components: Multiplexerer
Accumulator and P2S Converter

1. $f_c/8 : 256/8 = 2^5 \Rightarrow 00000100 \ 0$
2. $f_c/4 : 256/4 = 2^6 \Rightarrow 00000010 \ 0$
3. $f_c/2 : 256/2 = 2^7 \Rightarrow 00000001 \ 0$
4. $f_c : 256 = 2^8 \Rightarrow 00000001 \ 1$
Chip Layout

Front-End #1
Front-End #2
Clock Input
Front-End #3
Front-End #4
P2S converter
Accumulator
Output drivers
Multiplexer
Clock Controller
PTLs
Synchronizer
10mm x 10mm
LOW FREQUENCY TESTING AT MONITOR LEVEL (1)

<table>
<thead>
<tr>
<th></th>
<th>f_c</th>
<th>f_c/2</th>
<th>NS</th>
</tr>
</thead>
<tbody>
<tr>
<td>CH1</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CH2</td>
<td>f_c/8</td>
<td>f_c/2</td>
<td>NS</td>
</tr>
<tr>
<td>CH3</td>
<td>f_c/4</td>
<td>f_c/2</td>
<td>NS</td>
</tr>
<tr>
<td>CH4</td>
<td>f_c/2</td>
<td>f_c/2</td>
<td>NS</td>
</tr>
</tbody>
</table>

CIRCULATING ORDER: CH1, CH2, CH3, CH4
CARRY PULSE AT THE END OF CH1 IF f_c APPLIED
FRAME PULSE AT THE BEGINNING OF CH4
LOW FREQUENCY TESTING AT MONITOR LEVEL (2)
LOW FREQUENCY TESTING AT DRIVER LEVEL

<table>
<thead>
<tr>
<th></th>
<th>CH1</th>
<th>CH2</th>
<th>CH3</th>
<th>CH4</th>
</tr>
</thead>
<tbody>
<tr>
<td>fc</td>
<td>f_c</td>
<td>f_c/2</td>
<td>f_c</td>
<td>f_c/2</td>
</tr>
<tr>
<td>f_c/8</td>
<td>f_c/2</td>
<td>f_c</td>
<td>f_c/2</td>
<td>NS</td>
</tr>
<tr>
<td>f_c/4</td>
<td>f_c/2</td>
<td>f_c</td>
<td>f_c/2</td>
<td>NS</td>
</tr>
<tr>
<td>f_c/2</td>
<td>f_c/2</td>
<td>f_c</td>
<td>f_c/2</td>
<td>NS</td>
</tr>
</tbody>
</table>

KEY FEATURES:
1. CIRCULATING ORDER CH1, CH2, CH3, CH4
2. FRAME PULSE AT THE BEGINNING OF CH3
3. STORED NUMBER: 2^5, 2^6, 2^7
4. DATA RATE: f_c/8, f_c/4, f_c/2

# OF READ PULSES: 6, 7, 8
HIGH FREQUENCY TESTING @6.4GHz

**KEY FEATURES:**
- **CIRCULATING ORDER CH1,CH2,CH3,CH4**
- **FRAME PULSE AT THE BEGINNING OF CH3**

**DATA-RS:**
- $2^6$ $f_c/4$
- $2^7$ $f_c/2$
- $2^8$ $f_c$
- $2^5$ $f_c/8$

**READ:**
- 7
- 8
- 6

**FRAME:**
- CH3
- CH4
- CH1
- CH2

**SOURCE:**
- Automatic (Auto)

**DATA RATE:**
- $f_c/8$
- $f_c/4$
- $f_c/2$

**STORED NUMBER:**
- $2^5$
- $2^6$
- $2^7$

**# OF READ PULSES:**
- 6
- 7
- 8

**Table:**

<table>
<thead>
<tr>
<th>CH</th>
<th>$f_c$</th>
<th>$f_c/2$</th>
<th>NS</th>
</tr>
</thead>
<tbody>
<tr>
<td>CH1</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CH2</td>
<td>$f_c/8$</td>
<td>$f_c/2$</td>
<td>NS</td>
</tr>
<tr>
<td>CH3</td>
<td>$f_c/4$</td>
<td>$f_c/2$</td>
<td>NS</td>
</tr>
<tr>
<td>CH4</td>
<td>$f_c/2$</td>
<td>$f_c/2$</td>
<td>NS</td>
</tr>
</tbody>
</table>
### KEY FEATURES:
- Circulating Order CH1, CH2, CH3, CH4
- Frame Pulse at the beginning of CH3
- # of Read Pulses: 6, 7, 8
- Stored Number: $2^6$, $2^6$, $2^7$
- Data Rate: $f_c/8$, $f_c/4$, $f_c/2$
Signal Reconstruction

Clock: 8GHz
Signal: 156.25kHz
Signal amplitude: 300mVpp

Clock: 8GHz
Signal: 156.25kHz
Signal amplitude: 50mVpp
Digital SNSPD Readout
Digital SNSPD Readout

- SNSPD Output: Fast rise-time (~100 ps) pulse, 10-20 µA
- Requirement: Precise measurement of time-of-arrival
  - High clock speed (time-to-digital conversion)
  - Power consumption ~ 10 µW
- Time-of-arrival of photons measured as the number (n) of clock periods ($\tau_{clk}$) in a frame of N clock periods
  - Discrete time resolution $\tau_{clk}$ ~30 ps
  - Count Rate = $1/\tau_{frame}$ ~ 65 MHz
  - Counting of clock pulses started at the beginning of a frame and stopped at the arrival of the first SNSPD output pulse
Readout Chip Test with On-chip Data Data Generator


RSFQ vs ERSFQ: power consumption

Per L-JJ pair: $P_d = 0$ W

Per L-JJ pair: $P_d = 0$ W

Per resistor: $P_s \sim 100 \text{nW}$

Per Junction: $P_d \sim 10 \text{nW}$

Per Junction: $P_d \sim 10 \text{nW}$

Power consumption balance: $(10+100) \text{nW} \rightarrow (10+0) \text{nW}$
Digital Readout Chip for 4 SNSPDs

- 4 Digitizers
- Data generator
- PTL field
- Master clock-in
- Clock routing
- Aggregation block
- Interface to frequency divider
- Frequency divider
- SNSPD chip to be placed
- 4 Digitizers (A,B,C,D) for test experiments
- SFQ/dc converters
- Synchronizer
- Accumulator and P2S converter
- Output drivers
- On-off switch and pulse distribution
- 10mmx10mm
Time Delay = 0
Time Delay = 1
Time Delay = 2
Time Delay = 3
Time Delay = 510
Time Delay = 511
Time Delay = 0
## Power Consumption and Scalability

<table>
<thead>
<tr>
<th></th>
<th>Conservative Design (I_{c-avg} = 250\mu A, V_{bias} = 2.6mV)</th>
<th>Optimized Design</th>
<th>Scaled RSFQ (I_{c-avg} = 125 \mu A, V_{bias} = 1mV)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>RSFQ</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4 digitizers + routing</td>
<td>37.20</td>
<td>22.80</td>
<td>4.38</td>
</tr>
<tr>
<td>PTL field</td>
<td>17.60</td>
<td>5.50</td>
<td>1.06</td>
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<tr>
<td>Master clock-in</td>
<td>25.80</td>
<td>25.80</td>
<td>4.96</td>
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<tr>
<td>3 Output drivers</td>
<td>109.20</td>
<td>11.47</td>
<td>2.21</td>
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<td><strong>RSFQ total:</strong></td>
<td><strong>189.8</strong></td>
<td><strong>65.6</strong></td>
<td><strong>12.6</strong></td>
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<tr>
<td><strong>eRSFQ</strong></td>
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<td></td>
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<tr>
<td>Clock routing</td>
<td>0.44</td>
<td>0.44</td>
<td>0.44</td>
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<tr>
<td>Synchronizer</td>
<td>1.14</td>
<td>1.14</td>
<td>1.14</td>
</tr>
<tr>
<td>Aggregation block</td>
<td>0.90</td>
<td>0.90</td>
<td>0.90</td>
</tr>
<tr>
<td>Interface to frequency divider</td>
<td>2.00</td>
<td>2.00</td>
<td>2.00</td>
</tr>
<tr>
<td>Frequency divider</td>
<td>1.36</td>
<td>1.36</td>
<td>1.36</td>
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<tr>
<td>Switch and pulse distribution</td>
<td>3.63</td>
<td>3.63</td>
<td>3.63</td>
</tr>
<tr>
<td>Counter and serializer</td>
<td>6.39</td>
<td>6.39</td>
<td>6.39</td>
</tr>
<tr>
<td><strong>eRSFQ total @32GHz:</strong></td>
<td><strong>15.9</strong></td>
<td><strong>15.9</strong></td>
<td><strong>15.9</strong></td>
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<tr>
<td><strong>Chip total:</strong></td>
<td><strong>205.7</strong></td>
<td><strong>81.4</strong></td>
<td><strong>28.5</strong></td>
</tr>
</tbody>
</table>

Optimized design: SFQ/DC drivers, Eliminate test pattern generator and associated circuitry
## Power Consumption and Scalability (contd.)

<table>
<thead>
<tr>
<th>Component</th>
<th>4-SNSPD Readout</th>
<th>8-SNSPD Readout</th>
<th>16-SNSPD Readout</th>
</tr>
</thead>
<tbody>
<tr>
<td>Scaled RSFQ ($I_{c\text{-avg}} = 125 \mu A, V_{bias} = 1mV$)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>All power numbers in $\mu$W</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4 digitizers + routing</td>
<td>4.38</td>
<td>8.77</td>
<td>17.54</td>
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<tr>
<td>PTL field</td>
<td>1.06</td>
<td>2.12</td>
<td>4.23</td>
</tr>
<tr>
<td>Master clock-in</td>
<td>4.96</td>
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<tr>
<td>3 Output drivers</td>
<td>2.21</td>
<td>2.21</td>
<td>2.21</td>
</tr>
<tr>
<td>RSFQ total:</td>
<td><strong>12.61</strong></td>
<td><strong>18.05</strong></td>
<td><strong>28.94</strong></td>
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<td>Clock routing</td>
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<td>Synchronizer</td>
<td>1.14</td>
<td>2.28</td>
<td>4.56</td>
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<tr>
<td>Aggregation block</td>
<td>0.90</td>
<td>1.80</td>
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<td>Interface to frequency divider</td>
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<td>eRSFQ total @32GHz:</td>
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<td><strong>17.9</strong></td>
<td><strong>22.0</strong></td>
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<tr>
<td>Chip total:</td>
<td><strong>28.5</strong></td>
<td><strong>36.0</strong></td>
<td><strong>50.9</strong></td>
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<tr>
<td><strong>Power Consumption per SNSPD</strong></td>
<td><strong>7.1</strong></td>
<td><strong>4.5</strong></td>
<td><strong>3.2</strong></td>
</tr>
</tbody>
</table>

All power numbers in $\mu$W.
Converting to SFQ5EE process at MIT/LL
We designed both RSFQ and ERSFQ 6-bit counters using MIT/LL SFQ5EE process
tvl03_ed_003: 6b counter

- Data in
- Frame clock in
- Read clock in
- Data out
- Carry out
- Frame clock out
- Read clock out
- Data in

Feeding JTLs
6b counter
ERSFQ
Pulse distribution network
P2S converter
ERSFQ counter is 22.5 times smaller in area by converting to SFQ5EE
Test Results

RSFQ margins: 41mA-68mA
ERSFQ margins: 45mA-65mA
Critical Current 51mA
2 readouts (ERSFQ and RSFQ) are placed on the same chip.
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4-channel SNSPD Aggregating Readout Chip

2 readouts (ERSFQ and RSFQ) are placed on the same chip
Conclusion

- **Digital TDM Readout**
  - By means of embedded pattern generators we proved the correct operation of each channel and of all 4 channels combined at frequencies up to 12.8 GHz.
  - We were able to perform reconstruction of signal applied to individual ADC.

- **Time-to-Digital Readout for SNSPDs**
  - Current sensitivity ($\Delta I$) < 10 µA
  - Preserves fast rise times (< 100 ps)
  - Time-of-arrival can be measured with 30 ps digital resolution
  - Low power, scalable eRFSQ circuitry
  - ERSFQ digital circuit density is 22.5X higher with 8-layer MIT/LL process than 4-layer HYPRES process
  - The goal of 10µW per SNSPD is reachable.
Digital TDM readout was supported in part by a grant from DOE office of Nuclear Physics

TDC readout was supported by MIT/LL

New RSFQ/ERSFQ Counters for MIT/LL SFQ5ee process was supported by a research grant from the Office of Naval Research

The authors would like to thank

- HYPRES and MIT/LL fab teams for fabricating the chips,
- Andrew J. Kerman, Eric Dauler for fruitful discussions,
- Igor Vernik for preliminary testing,
- Denis Amparo for taking photographs.