# Digital Readout for Cryogenic Detectors using Superconductor Integrated Circuits

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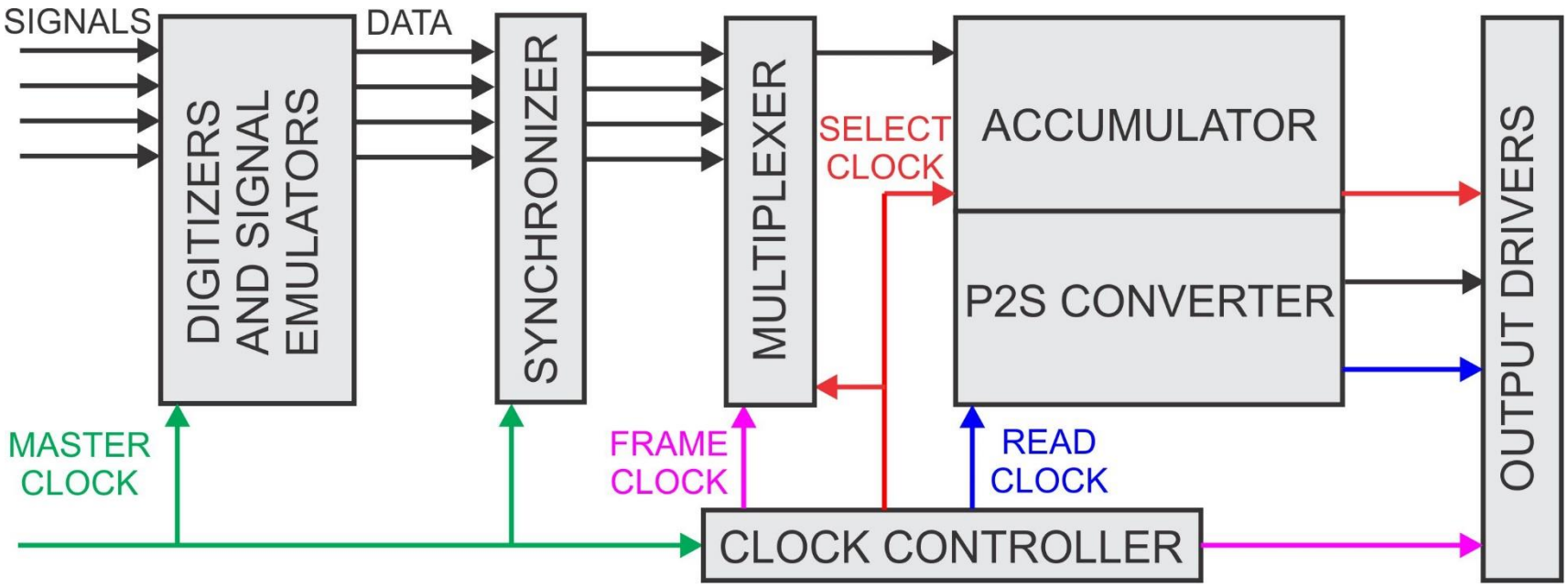
# Objectives

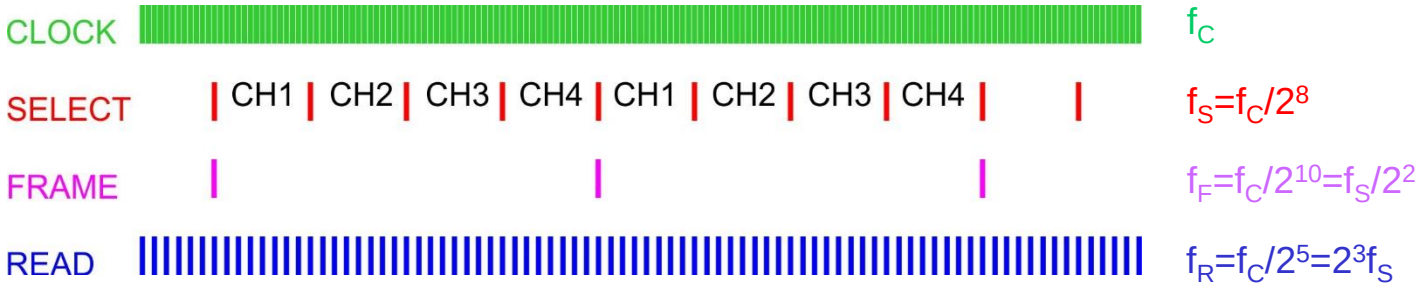
- **Superconductor fast digitizers and low-power logic are well suited for sensor array readout, enabling precise pulse timing and digital multiplexing.**

- **We can do both**
  - **Digital time-division multiplexing**
  - **Time-of-arrival measurements**

# Digital Time-Division Multiplexing Readout Circuit for Sensor Arrays

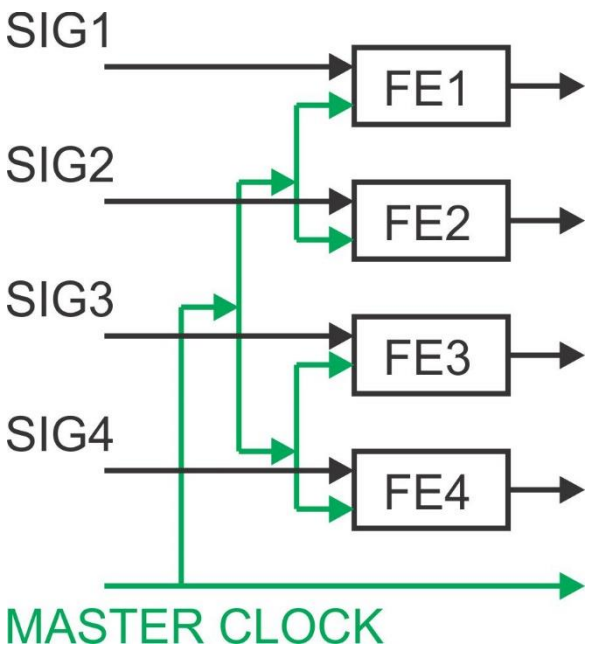
# Block Diagram



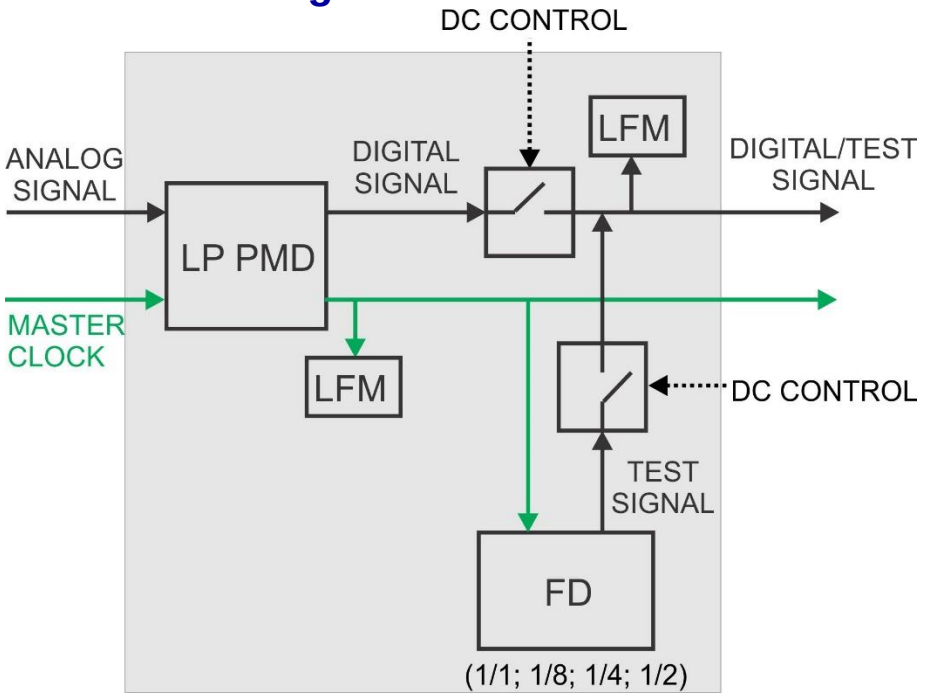



# Synchronous 4-Channel Front-End

## 4 Channels



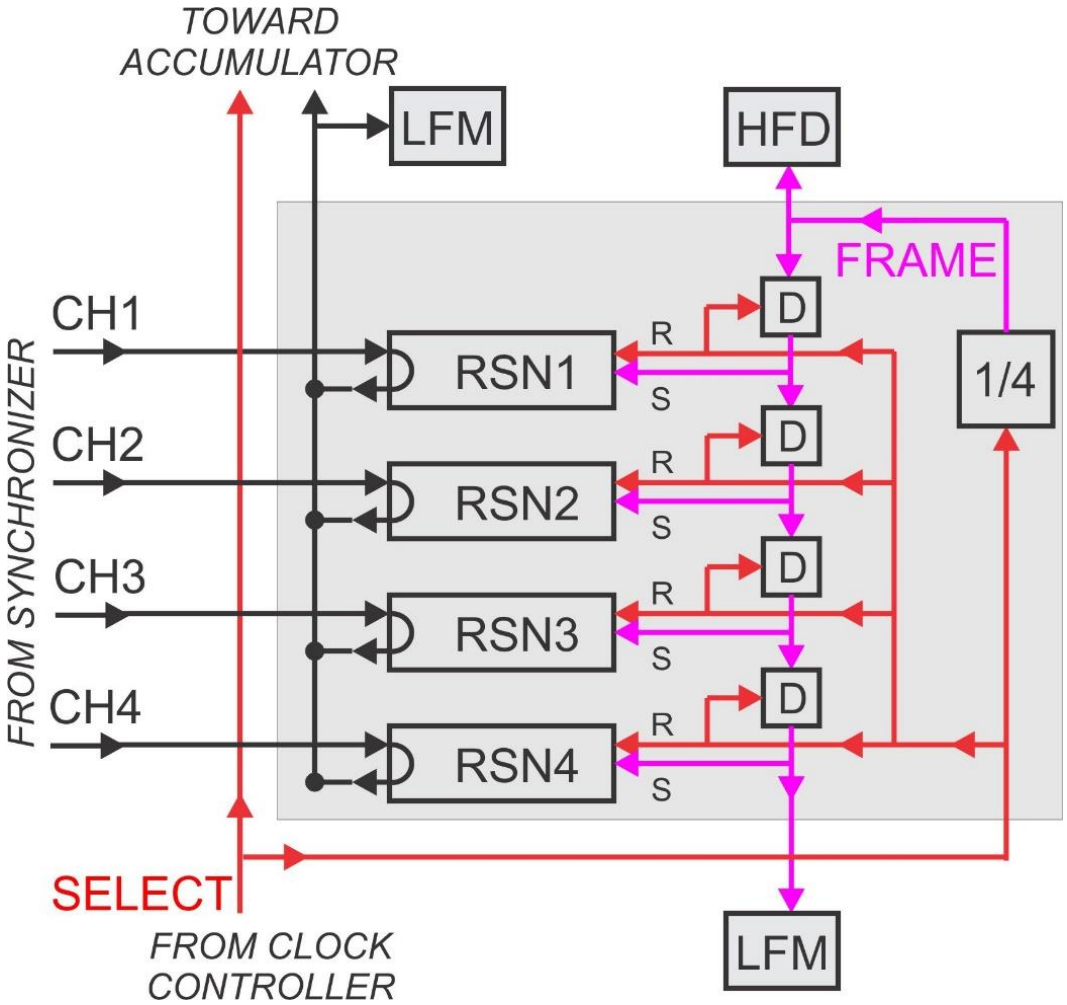

## Single Channel



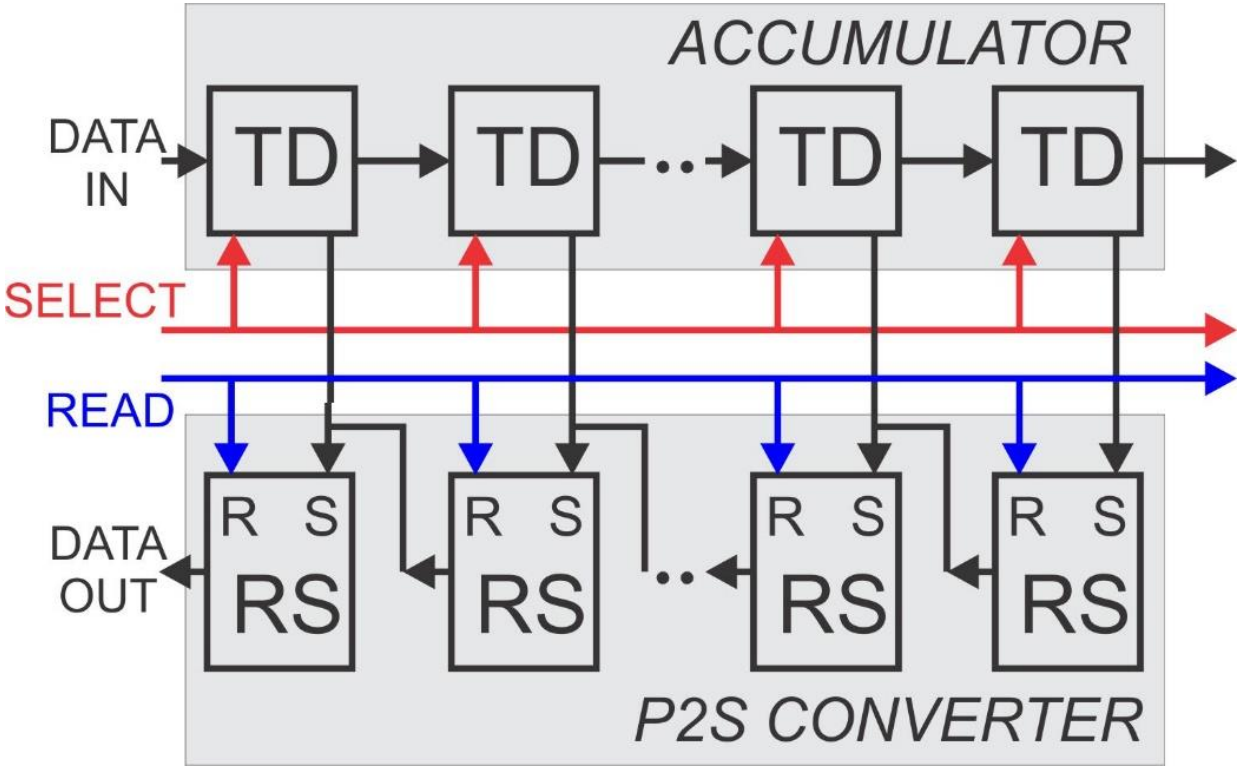

## Signal Variations at each Channels

| CHANNEL NAME | SIGNAL NAME | TEST PATTERN 1 | TEST PATTERN 2 | TEST PATTERN 3 |
|---|---|---|---|---|
| CH1 | SIG1 | $f_C$ | $f_C/2$ | NO SIG |
| CH2 | SIG2 | $f_C/8$ | $f_C/2$ | NO SIG |
| CH3 | SIG3 | $f_C/4$ | $f_C/2$ | NO SIG |
| CH4 | SIG4 | $f_C/2$ | $f_C/2$ | NO SIG |

# Design Components: Multiplexer



# Accumulator and P2S Converter




1 2 3 4 5 6 7 8 C

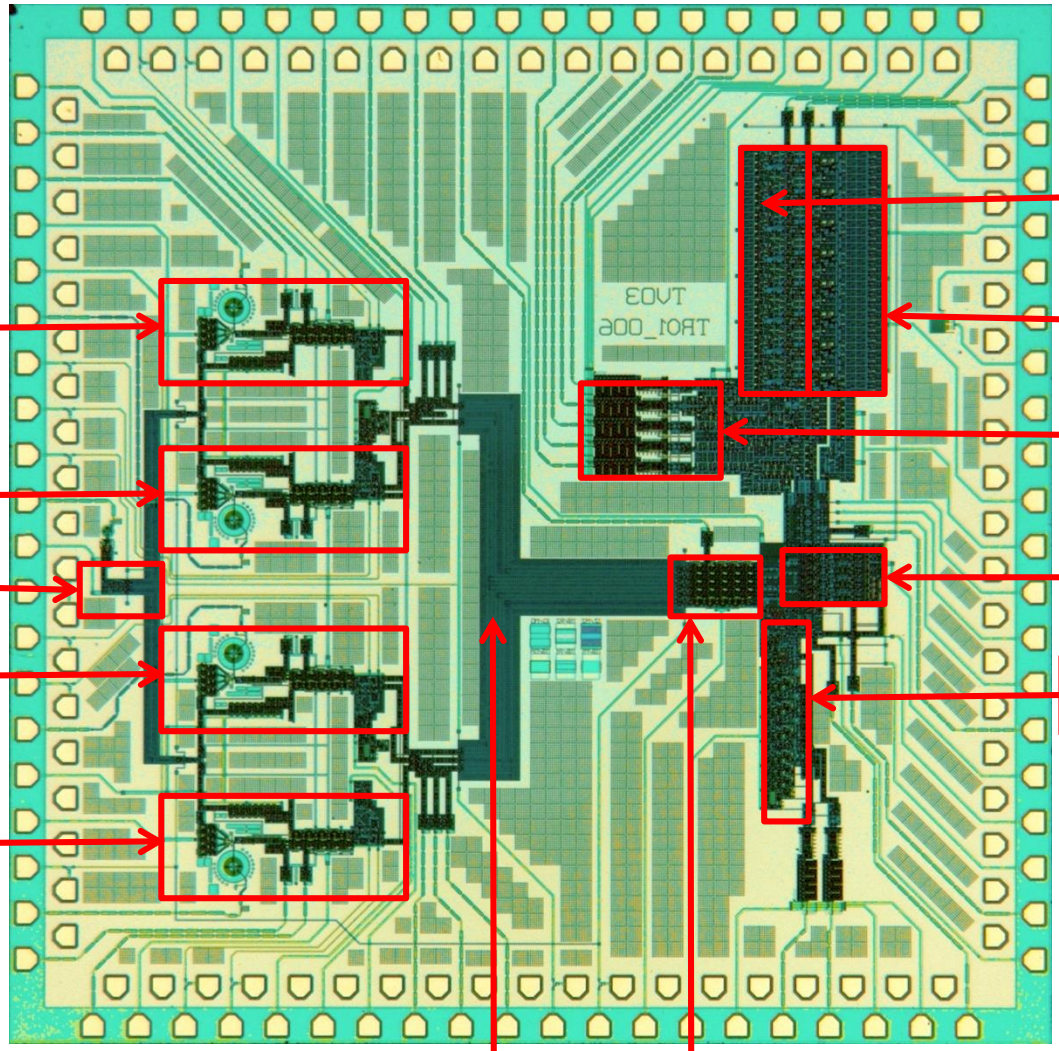
$f_C/8$ : 256/8=$2^5$ → 00000100 0

$f_C/4$ : 256/4=$2^6$ → 00000010 0

$f_C/2$ : 256/2=$2^7$ → 00000001 0

$f_C$ : 256 = $2^8$ → 00000000 1

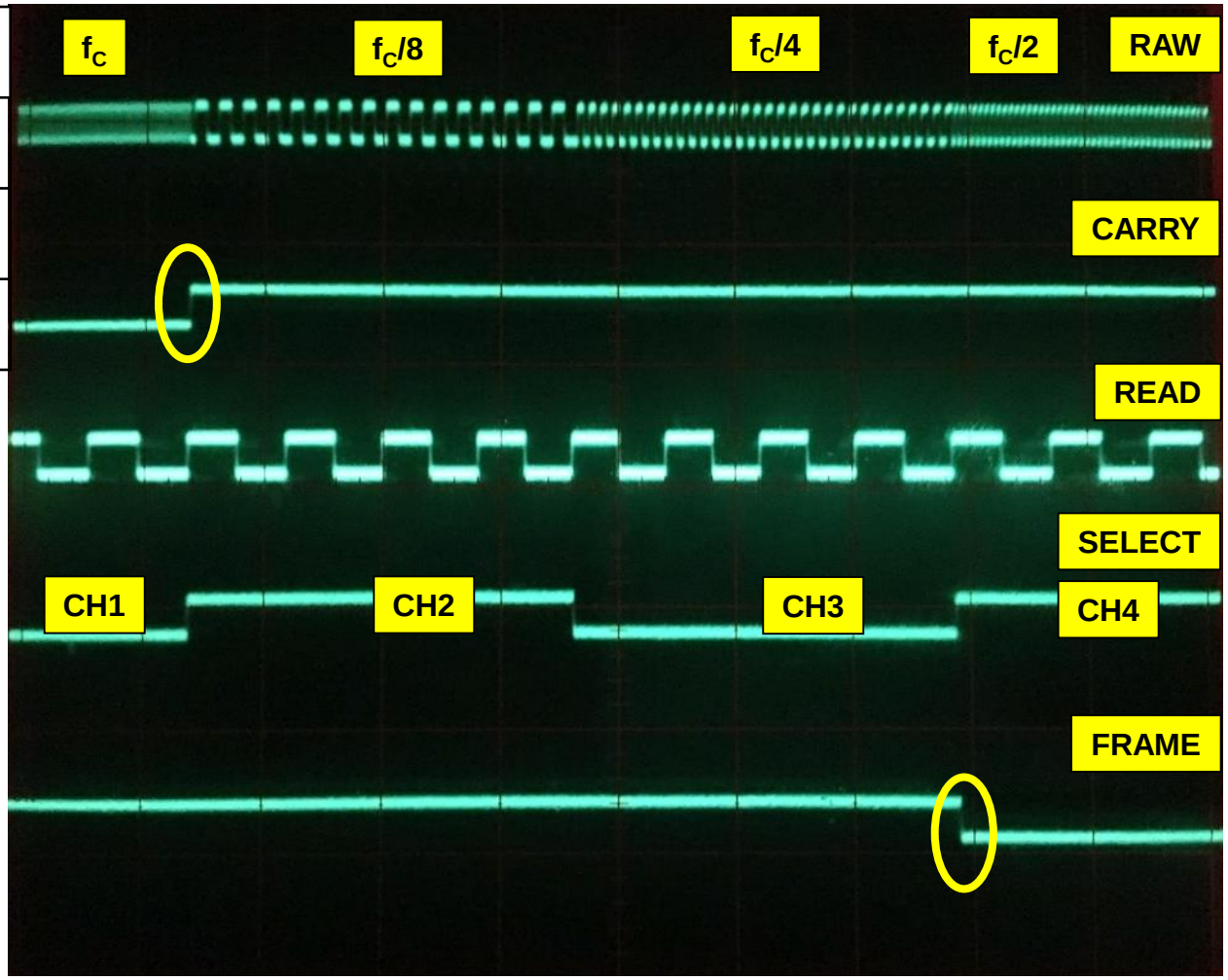
# Chip Layout




10mmx10mm

# LOW FREQUENCY TESTING AT MONITOR LEVEL (1)

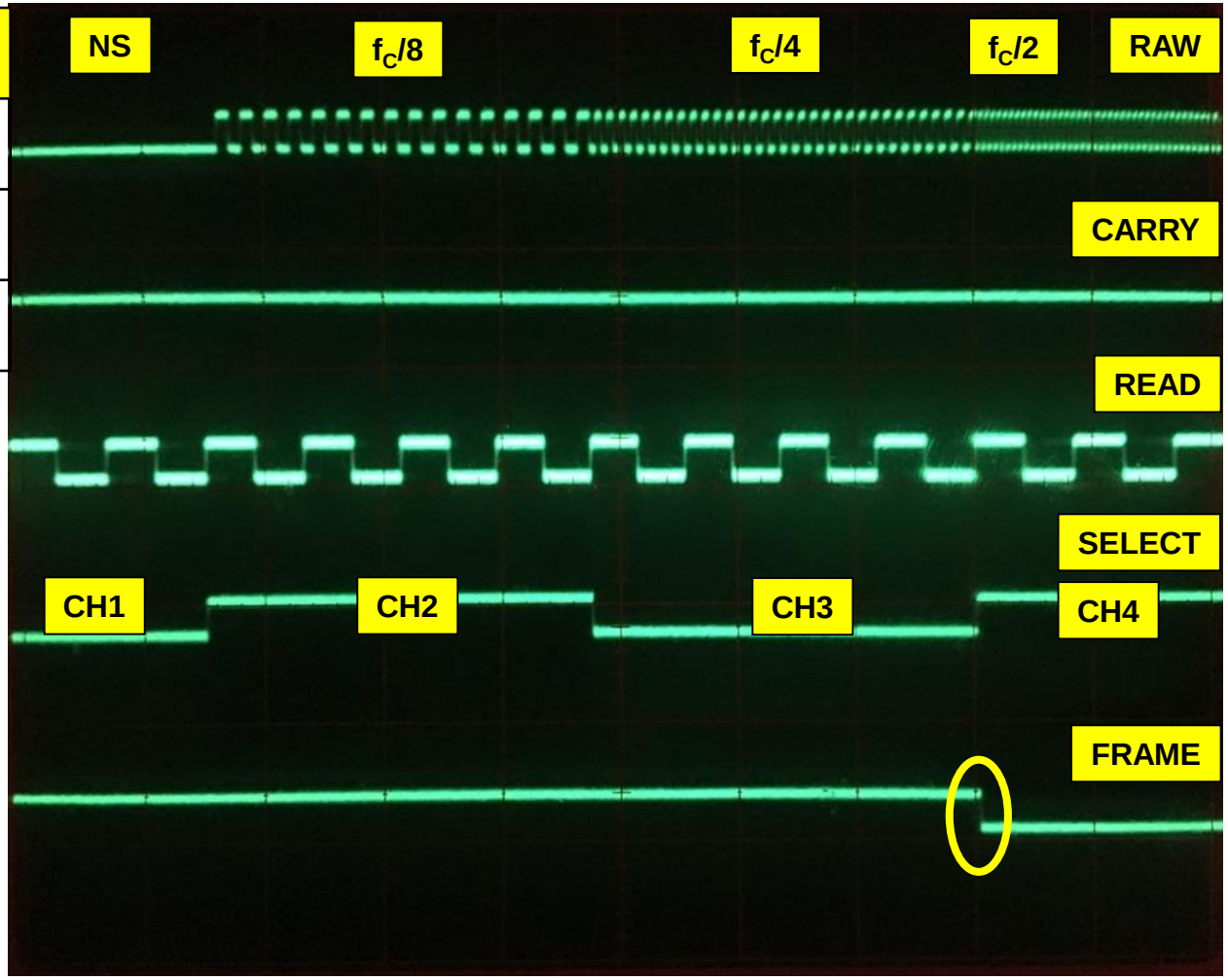
| | | | |
|---|---|---|---|
| CH1 | $f_C$ | $f_C/2$ | NS |
| CH2 | $f_C/8$ | $f_C/2$ | NS |
| CH3 | $f_C/4$ | $f_C/2$ | NS |
| CH4 | $f_C/2$ | $f_C/2$ | NS |




*CIRCULATING ORDER: CH1,CH2,CH3,CH4*
*CARRY PULSE AT THE END OF CH1 IF $f_C$ APPLIED*
*FRAME PULSE AT THE BEGINNING OF CH4*

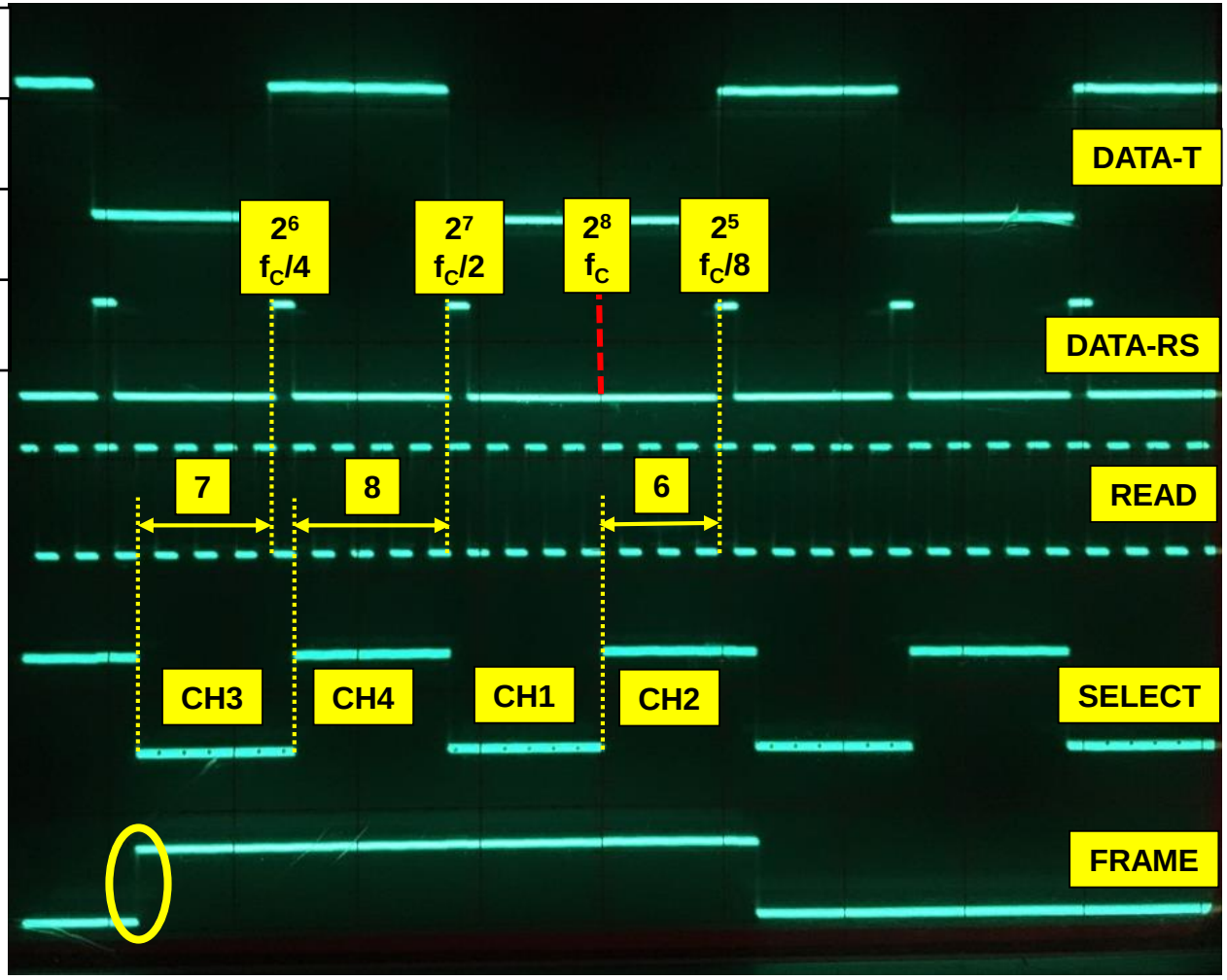
# LOW FREQUENCY TESTING AT MONITOR LEVEL (2)

| | | | |
|---|---|---|---|
| CH1 | $f_C$ | $f_C/2$ | NS |
| CH2 | $f_C/8$ | $f_C/2$ | NS |
| CH3 | $f_C/4$ | $f_C/2$ | NS |
| CH4 | $f_C/2$ | $f_C/2$ | NS |



# LOW FREQUENCY TESTING AT DRIVER LEVEL

| | | | |
|---|---|---|---|
| CH1 | $f_C$ | $f_C/2$ | NS |
| CH2 | $f_C/8$ | $f_C/2$ | NS |
| CH3 | $f_C/4$ | $f_C/2$ | NS |
| CH4 | $f_C/2$ | $f_C/2$ | NS |

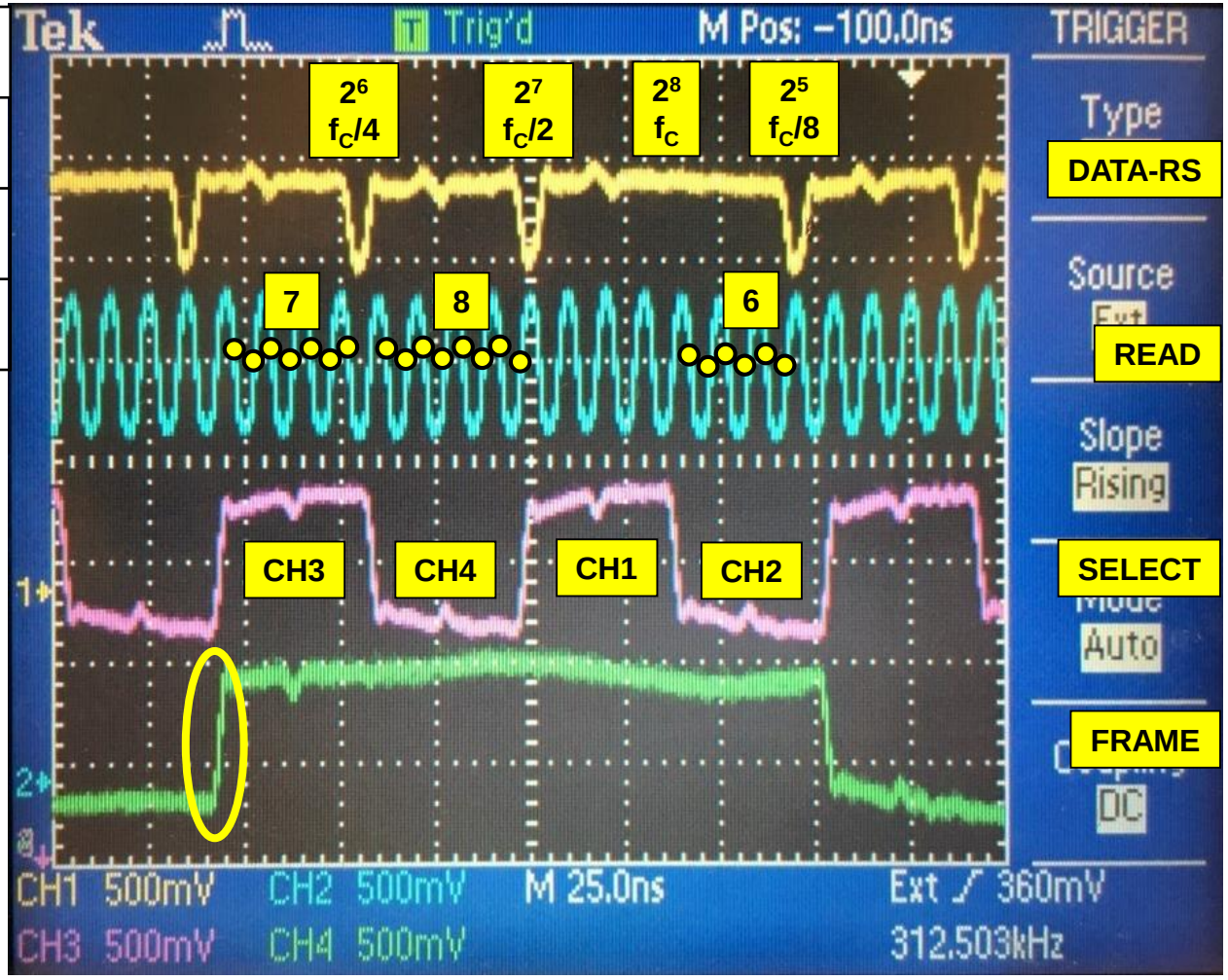



*KEY FEATURES:*
*CIRCULATING ORDER CH1,CH2,CH3,CH4*
*FRAME PULSE AT THE BEGINNING OF CH3*

| | | | |
|---|---|---|---|
| *# OF READ PULSES:* | *6* | *7* | *8* |
| *STORED NUMBER:* | $2^5$ | $2^6$ | $2^7$ |
| *DATA RATE:* | $f_C/8$ | $f_C/4$ | $f_C/2$ |

# HIGH FREQUENCY TESTING @6.4GHz

| | | | |
|---|---|---|---|
| CH1 | $f_C$ | $f_C/2$ | NS |
| CH2 | $f_C/8$ | $f_C/2$ | NS |
| CH3 | $f_C/4$ | $f_C/2$ | NS |
| CH4 | $f_C/2$ | $f_C/2$ | NS |

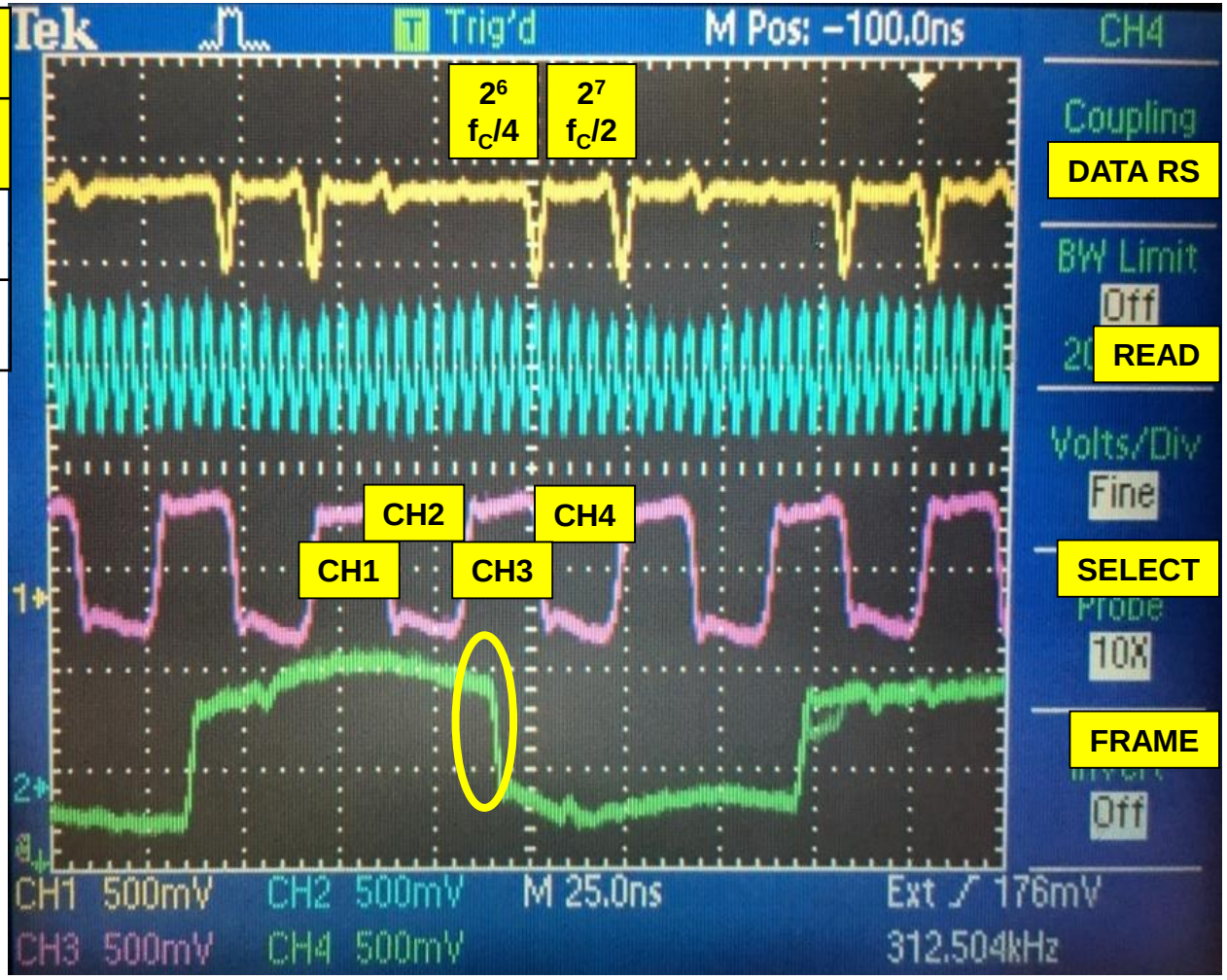



*KEY FEATURES:*
*CIRCULATING ORDER CH1,CH2,CH3,CH4*
*FRAME PULSE AT THE BEGINNING OF CH3*

| | | | |
|---|---|---|---|
| *# OF READ PULSES:* | *6* | *7* | *8* |
| *STORED NUMBER:* | *$2^5$* | *$2^6$* | *$2^7$* |
| *DATA RATE:* | *$f_C/8$* | *$f_C/4$* | *$f_C/2$* |

# HIGH FREQUENCY TESTING @12.8GHz

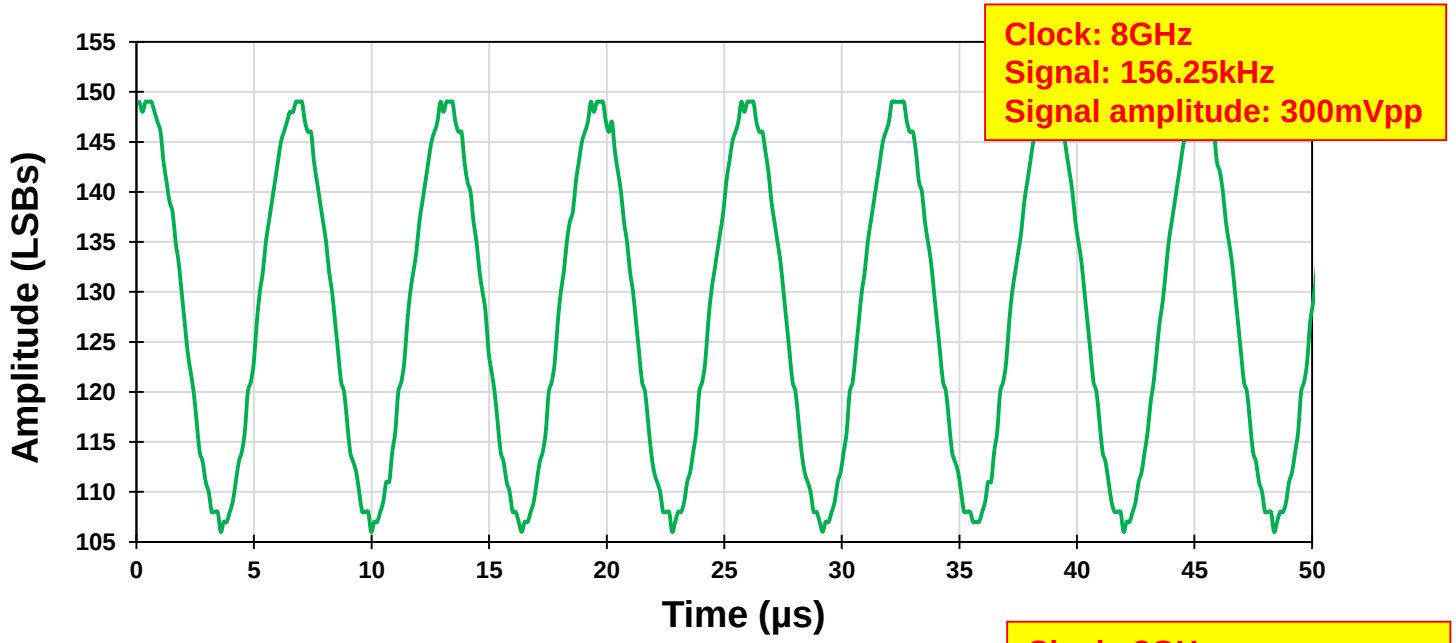
| | | | |
|---|---|---|---|
| CH1 | $f_C$ | $f_C/2$ | NS |
| CH2 | $f_C/8$ | $f_C/2$ | NS |
| CH3 | $f_C/4$ | $f_C/2$ | NS |
| CH4 | $f_C/2$ | $f_C/2$ | NS |

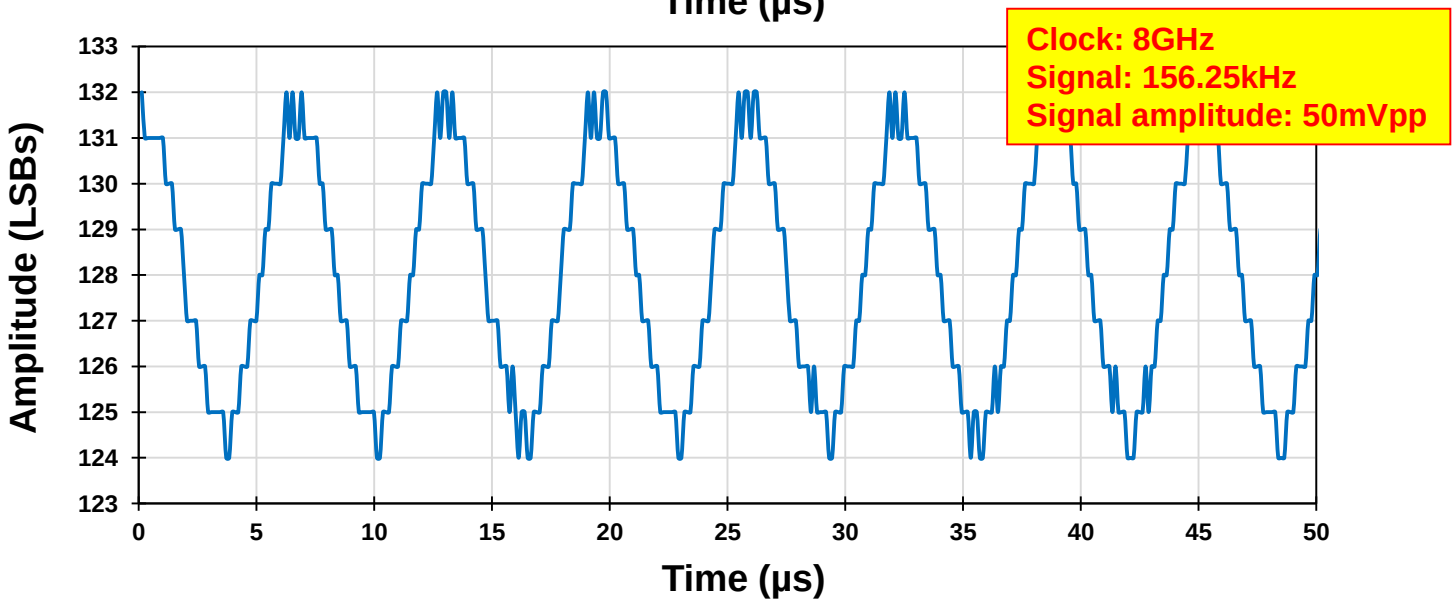



*KEY FEATURES:*
*CIRCULATING ORDER CH1,CH2,CH3,CH4*
*FRAME PULSE AT THE BEGINNING OF CH3*

| | | | |
|---|---|---|---|
| *# OF READ PULSES:* | *6* | *7* | *8* |
| *STORED NUMBER:* | $2^5$ | $2^6$ | $2^7$ |
| *DATA RATE:* | $f_C/8$ | $f_C/4$ | $f_C/2$ |

# Signal Reconstruction



# Digital SNSPD Readout

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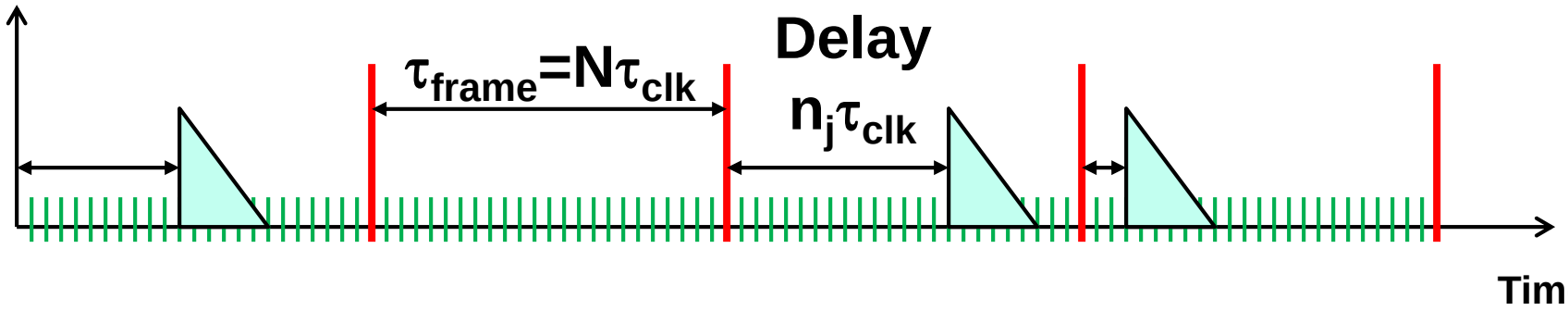
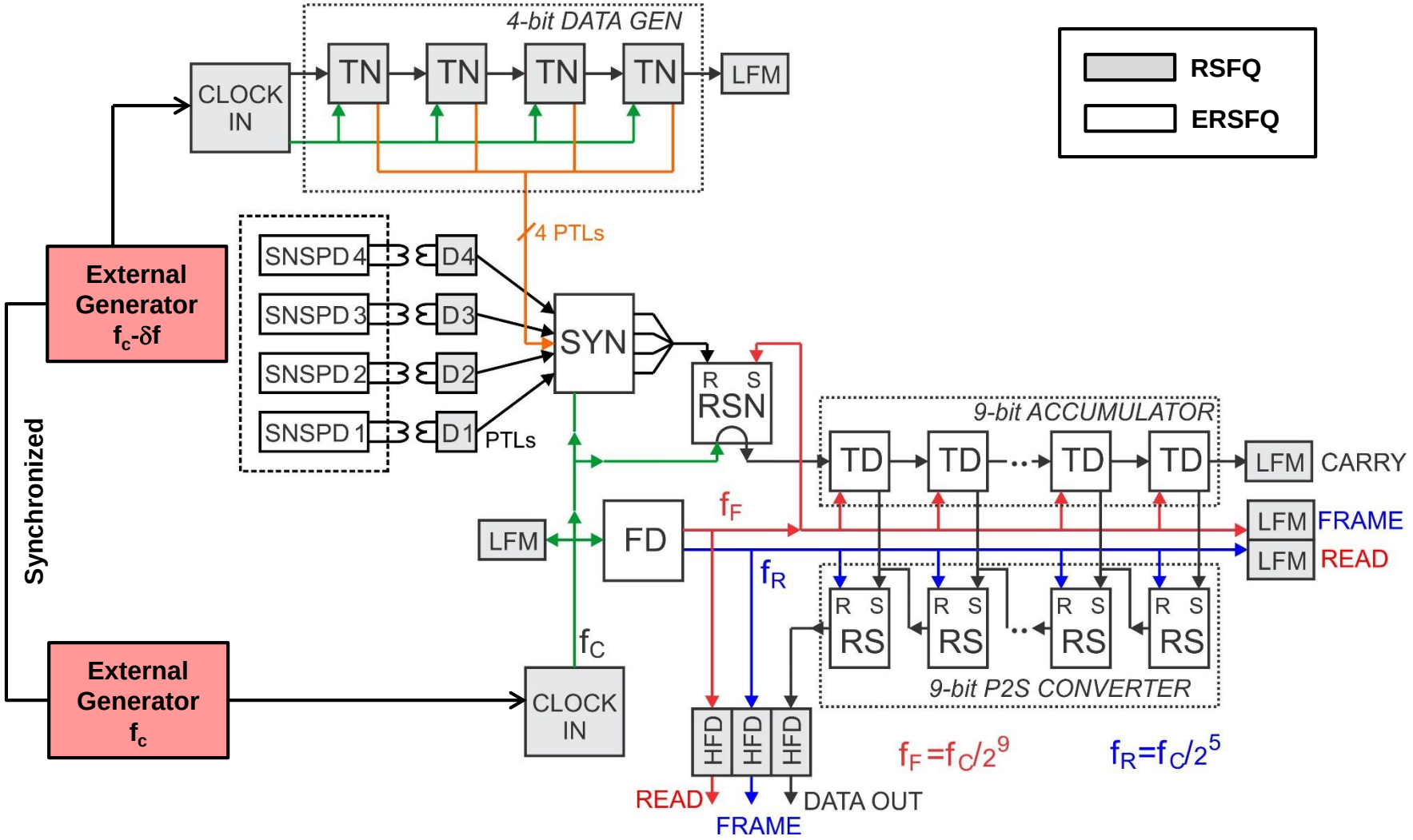



- SNSPD Output: Fast rise-time (~100 ps) pulse, 10-20 μA
- Requirement: Precise measurement of time-of-arrival
  - High clock speed (time-to-digital conversion)
  - Power consumption ~ 10 μW
- Time-of-arrival of photons measured as the number (n) of clock periods ($\tau_{clk}$) in a frame of N clock periods
  - Discrete time resolution $\tau_{clk}$ ~30 ps
  - Count Rate = $1/\tau_{frame}$ ~ 65 MHz
  - Counting of clock pulses started at the beginning of a frame and stopped at the arrival of the first SNSPD output pulse

# Readout Chip Test with On-chip Data Generator

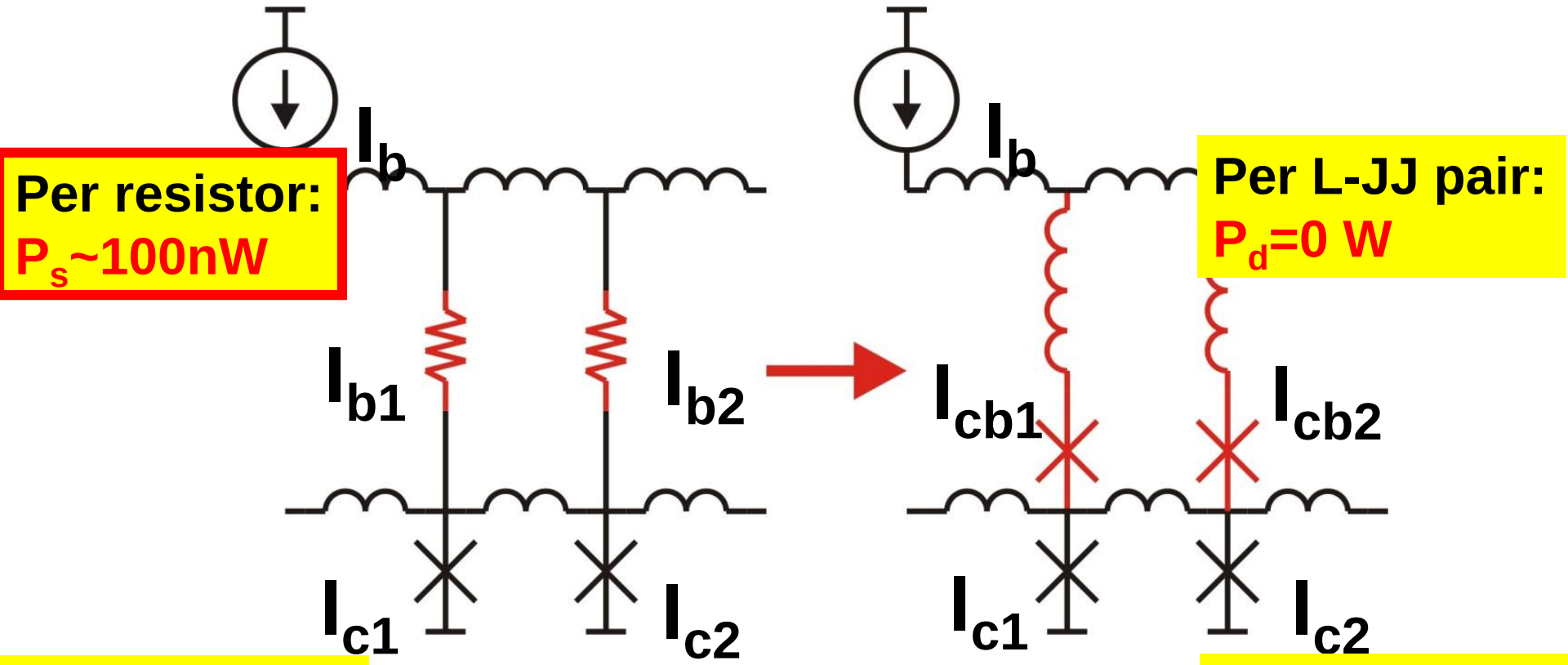




*O. A. Mukhanov and S. R. Rylov, "Time-to-digital converters based on RSFQ digital counters," IEEE Trans. Appl. Supercond., vol. 7, pp. 2669-2672, June 1997.*

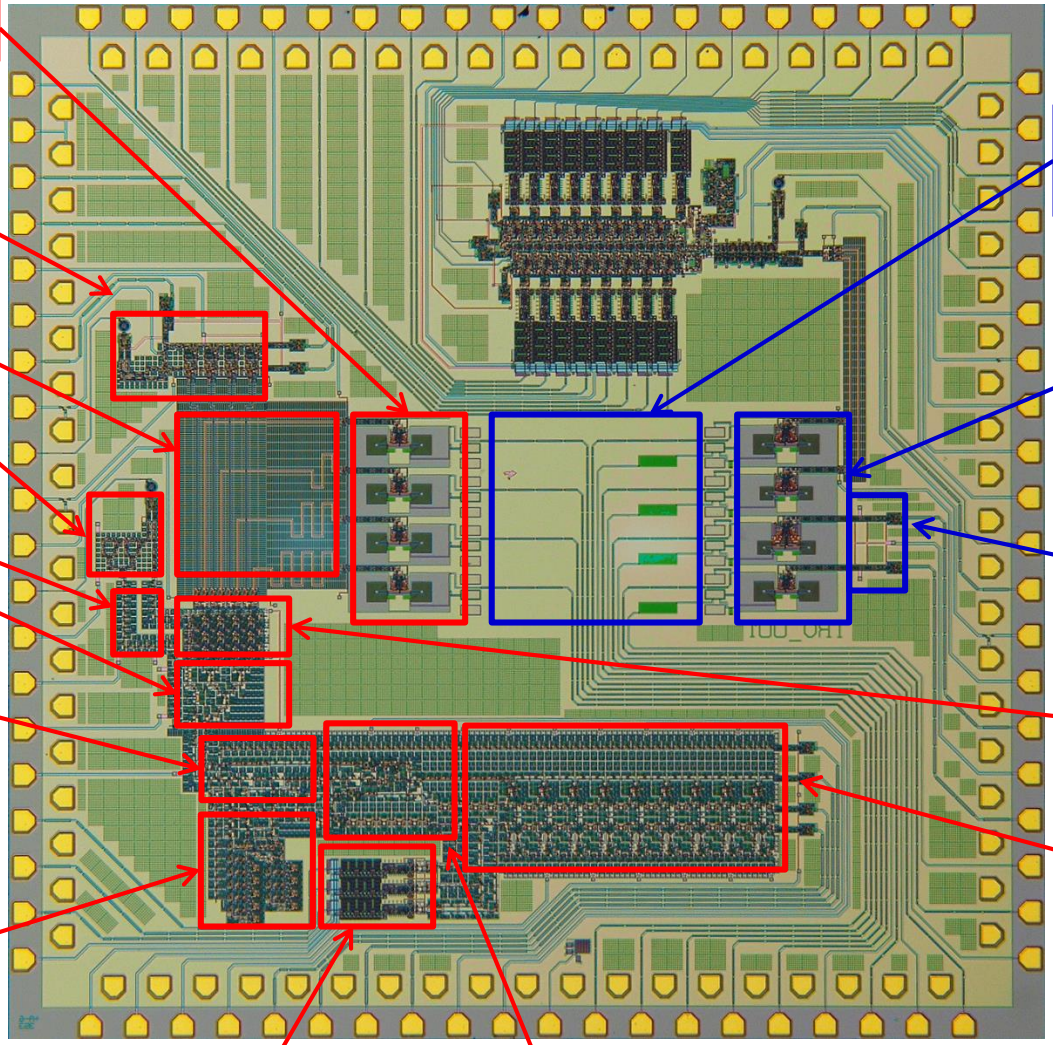
*A. Kirichenko, S. Sarwana, D. Gupta, I. Rochwarger, and O. Mukhanov, "Multi Channel Time Digitizing Systems," IEEE Trans. Appl. Supercond., vol. 13, pp. 454-458, June 2003*

# RSFQ vs ERSFQ: power consumption




Power consumption balance: (10+100)nW→(10+0)nW

# Digital Readout Chip for 4 SNSPDs



4 Digitizers

Data generator

PTL field

Master clock-in

Clock routing

Aggregation block

Interface to frequency divider

Frequency divider

Output drivers

On-off switch and pulse distribution

SNSPD chip to be placed

4 Digitizers (A,B,C,D) for test experiments

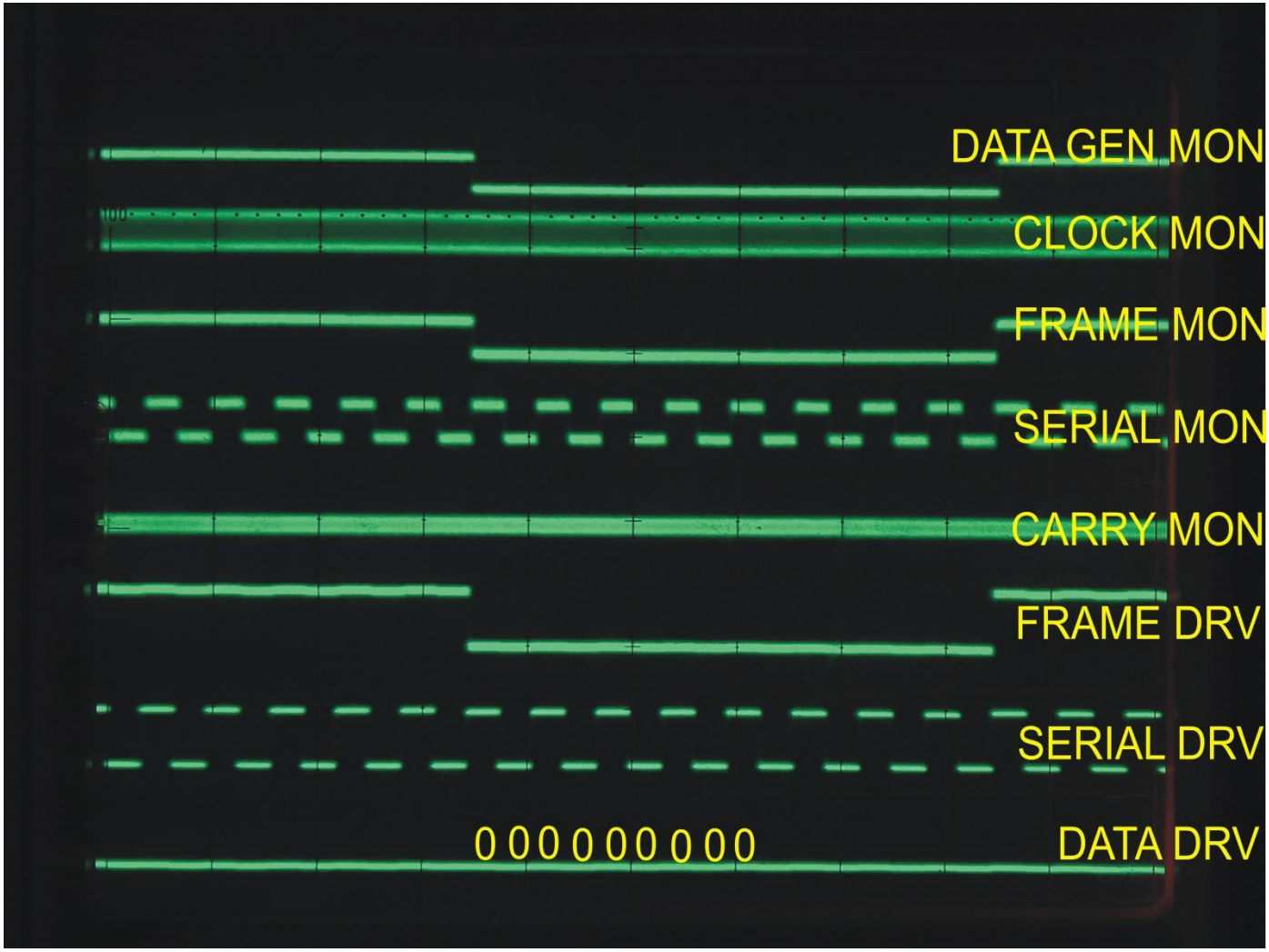
SFQ/dc converters

Synchronizer

Accumulator and P2S converter

10mmx10mm

# Time Delay = 0


DATA GEN MON
CLOCK MON
FRAME MON
SERIAL MON
CARRY MON
FRAME DRV
SERIAL DRV
0 0 0 0 0 0 0 0 0 0
DATA DRV

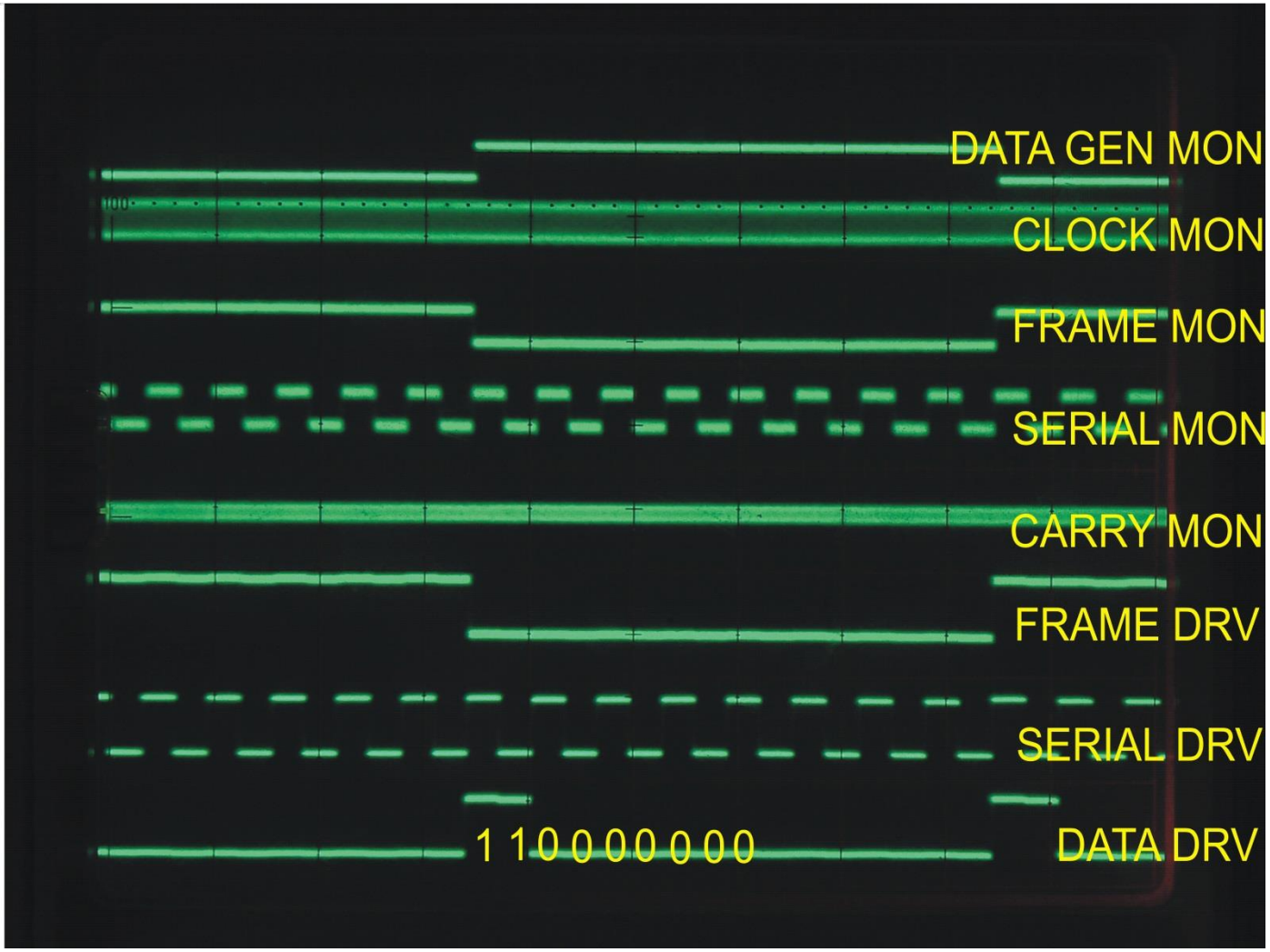
# Time Delay = 1


DATA GEN MON
CLOCK MON
FRAME MON
SERIAL MON
CARRY MON
FRAME DRV
SERIAL DRV
DATA DRV
1 0 0 0 0 0 0 0 0

# Time Delay = 2


DATA GEN MON
CLOCK MON
FRAME MON
SERIAL MON
CARRY MON
FRAME DRV
SERIAL DRV
0 1 0 0 0 0 0 0 0
DATA DRV

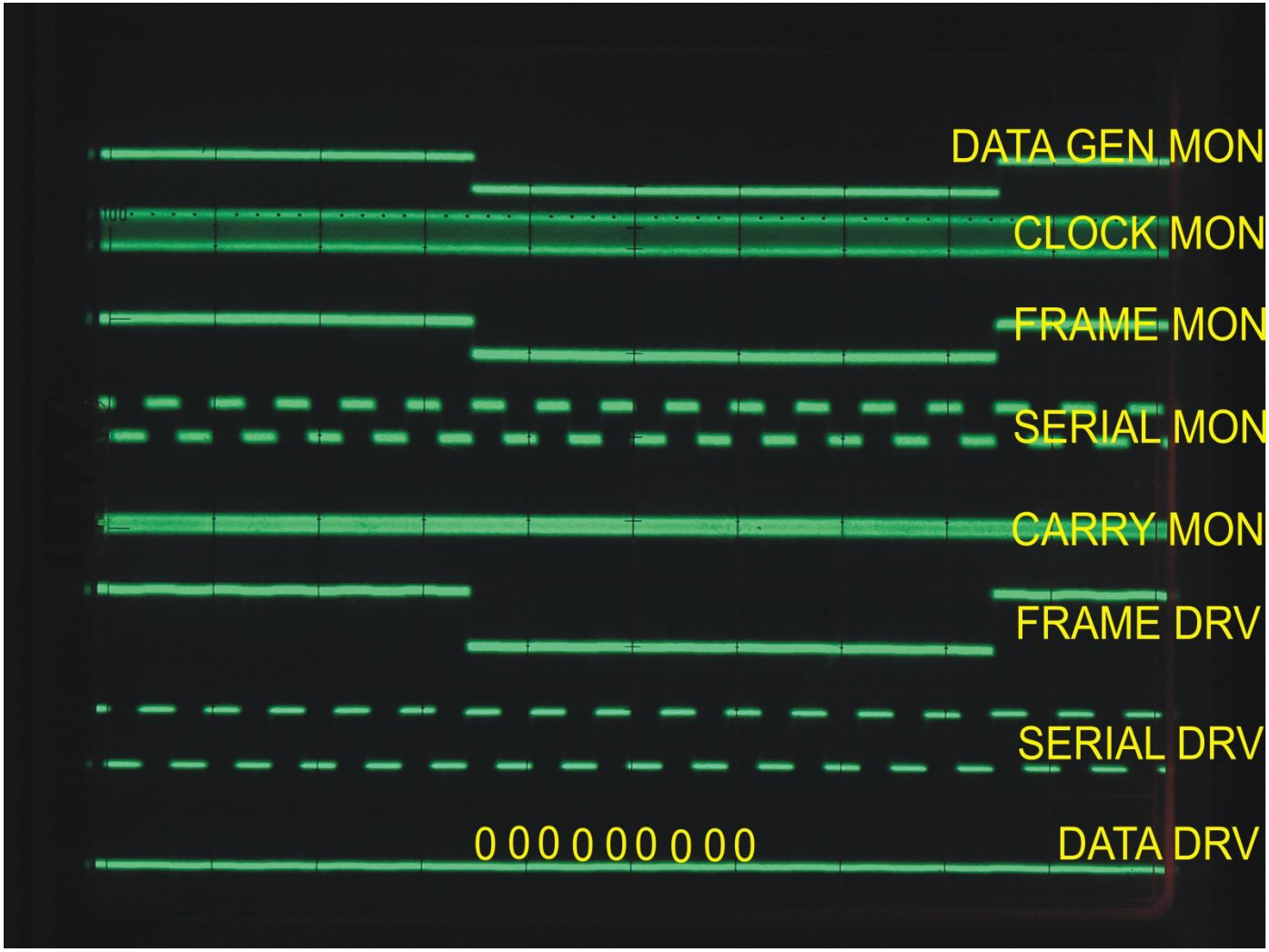
# Time Delay = 3


DATA GEN MON
CLOCK MON
FRAME MON
SERIAL MON
CARRY MON
FRAME DRV
SERIAL DRV
DATA DRV
1 1 0 0 0 0 0 0 0

# Time Delay = 510

# Time Delay = 511

# Time Delay = 0


DATA GEN MON
CLOCK MON
FRAME MON
SERIAL MON
CARRY MON
FRAME DRV
SERIAL DRV
0 0 0 0 0 0 0 0 0 0
DATA DRV

# Power Consumption and Scalability

| All power numbers in μW | | Conservative Design ($I_{c\text{-}avg}$ = 250μA, $V_{bias}$ = 2.6mV) | Optimized Design | Scaled RSFQ ($I_{c\text{-}avg}$ = 125 μA, $V_{bias}$ = 1mV) |
|---|---|---|---|---|
| RSFQ | 4 digitizers + routing | 37.20 | 22.80 | 4.38 |
| | PTL field | 17.60 | 5.50 | 1.06 |
| | Master clock-in | 25.80 | 25.80 | 4.96 |
| | 3 Output drivers | 109.20 | 11.47 | 2.21 |
| | **RSFQ total:** | **189.8** | **65.6** | **12.6** |
| eRSFQ | Clock routing | 0.44 | 0.44 | 0.44 |
| | Synchronizer | 1.14 | 1.14 | 1.14 |
| | Aggregation block | 0.90 | 0.90 | 0.90 |
| | Interface to frequency divider | 2.00 | 2.00 | 2.00 |
| | Frequency divider | 1.36 | 1.36 | 1.36 |
| | Switch and pulse distribution | 3.63 | 3.63 | 3.63 |
| | Counter and serializer | 6.39 | 6.39 | 6.39 |
| | **eRSFQ total @32GHz:** | **15.9** | **15.9** | **15.9** |
| | **Chip total:** | **205.7** | **81.4** | **28.5** |

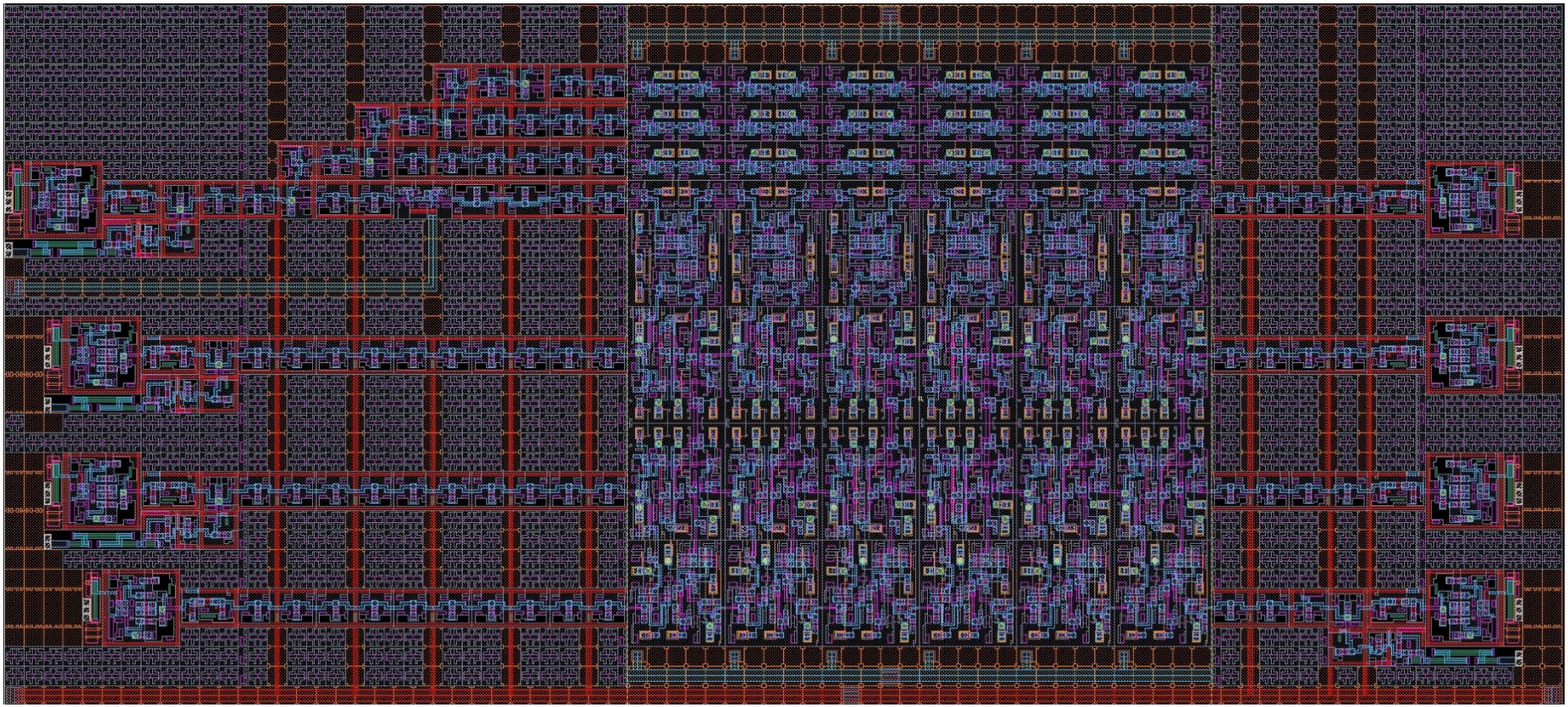
**Optimized design: SFQ/DC drivers, Eliminate test pattern generator and associated circuitry**

# Power Consumption and Scalability (contd.)

| All power numbers in μW | | 4-SNSPD Readout | 8-SNSPD Readout | 16-SNSPD Readout |
|---|---|---|---|---|
| | | Scaled RSFQ ($I_{c\text{-}avg}$ = 125 μA, $V_{bias}$ = 1mV) | Scaled RSFQ ($I_{c\text{-}avg}$ = 125 μA, $V_{bias}$ = 1mV) | Scaled RSFQ ($I_{c\text{-}avg}$ = 125 μA, $V_{bias}$ = 1mV) |
| RSFQ | 4 digitizers + routing | 4.38 | 8.77 | 17.54 |
| | PTL field | 1.06 | 2.12 | 4.23 |
| | Master clock-in | 4.96 | 4.96 | 4.96 |
| | 3 Output drivers | 2.21 | 2.21 | 2.21 |
| | **RSFQ total:** | **12.61** | **18.05** | **28.94** |
| eRSFQ | Clock routing | 0.44 | 0.44 | 0.44 |
| | Synchronizer | 1.14 | 2.28 | 4.56 |
| | Aggregation block | 0.90 | 1.80 | 3.60 |
| | Interface to frequency divider | 2.00 | 2.00 | 2.00 |
| | Frequency divider | 1.36 | 1.36 | 1.36 |
| | Switch and pulse distribution | 3.63 | 3.63 | 3.63 |
| | Counter and serializer | 6.39 | 6.39 | 6.39 |
| | **eRSFQ total @32GHz:** | **15.9** | **17.9** | **22.0** |
| | **Chip total:** | **28.5** | **36.0** | **50.9** |
| **Power Consumption per SNSPD** | | **7.1** | **4.5** | **3.2** |

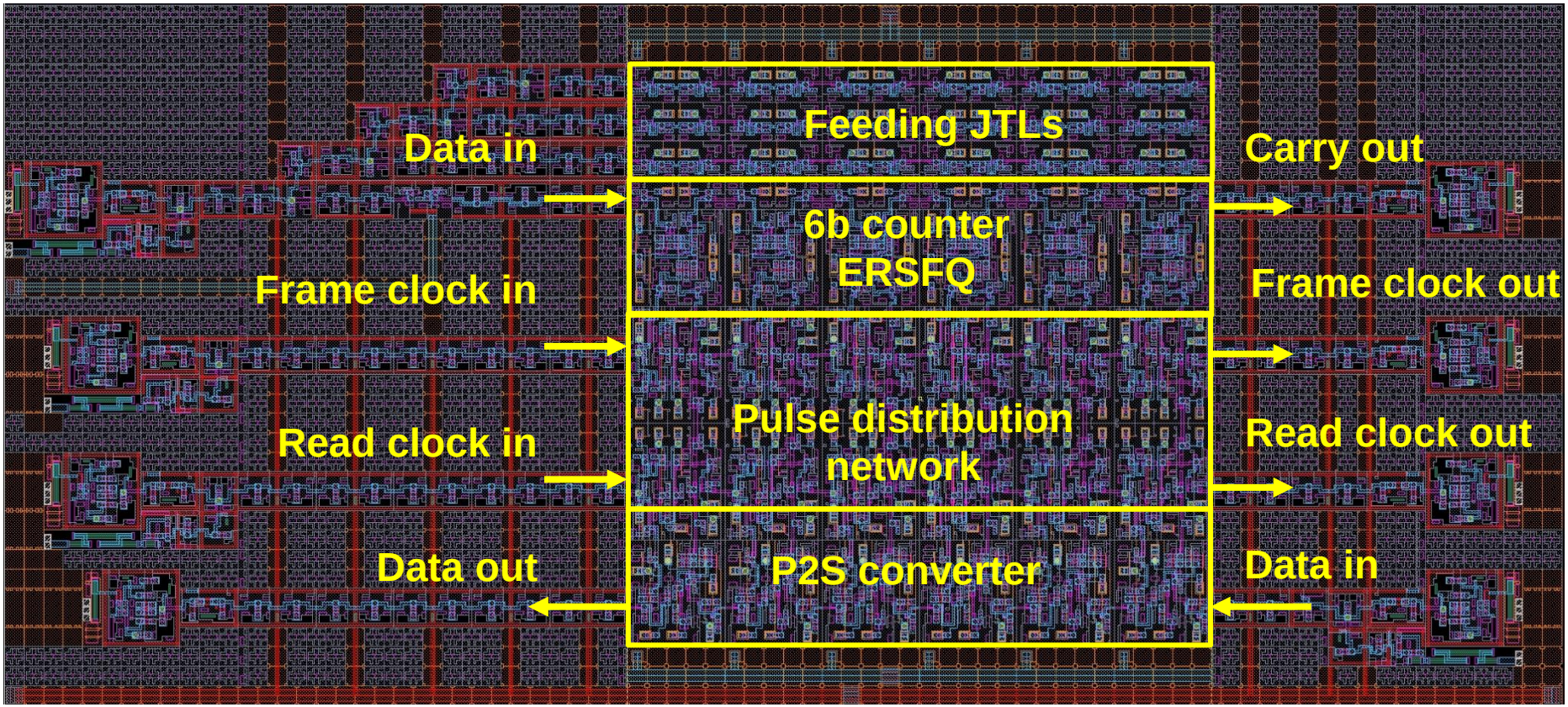
# Converting to SFQ5EE process at MIT/LL

# Chip tvl03_ed_003: 6b counter

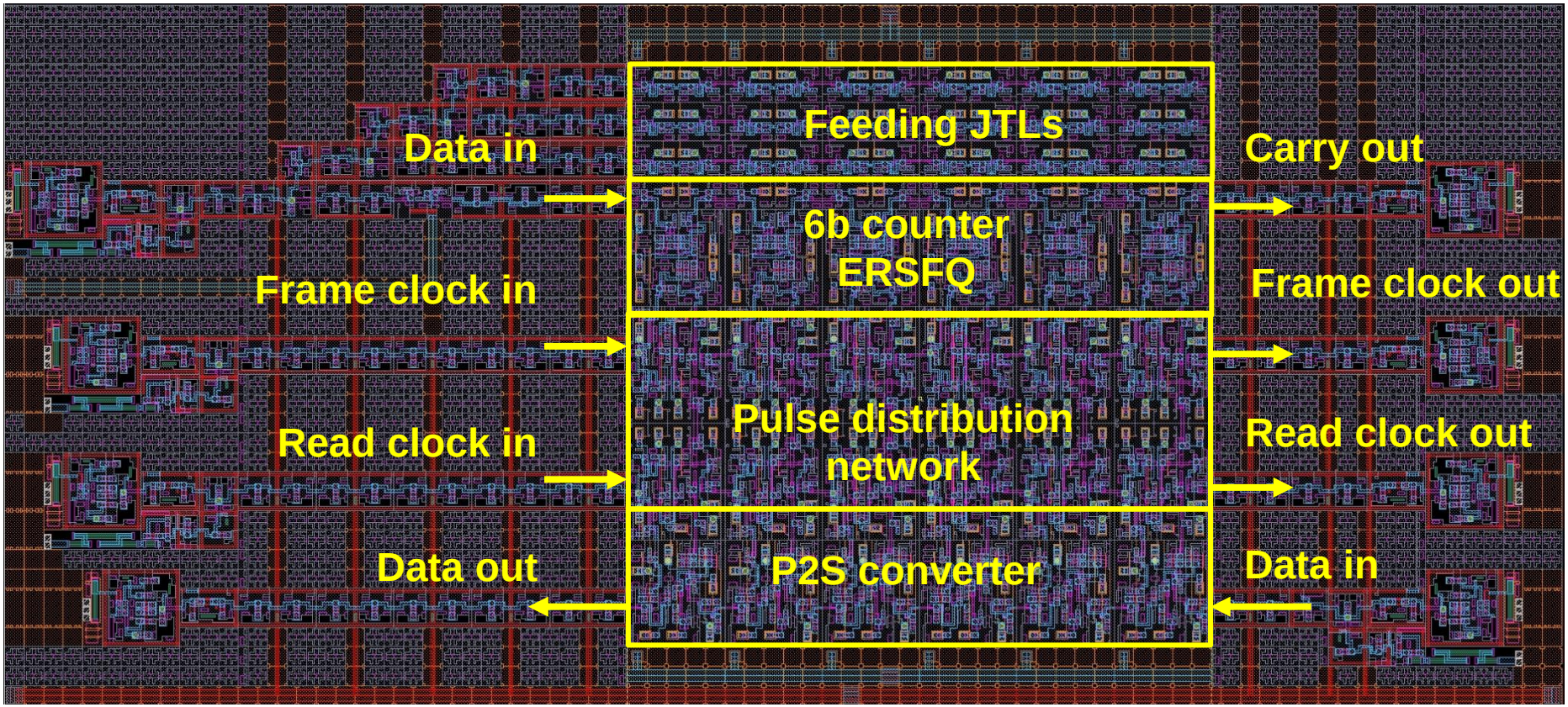


**We designed both RSFQ and ERSFQ 6-bit counters using MIT/LL SFQ5EE process**

# tvl03_ed_003: 6b counter

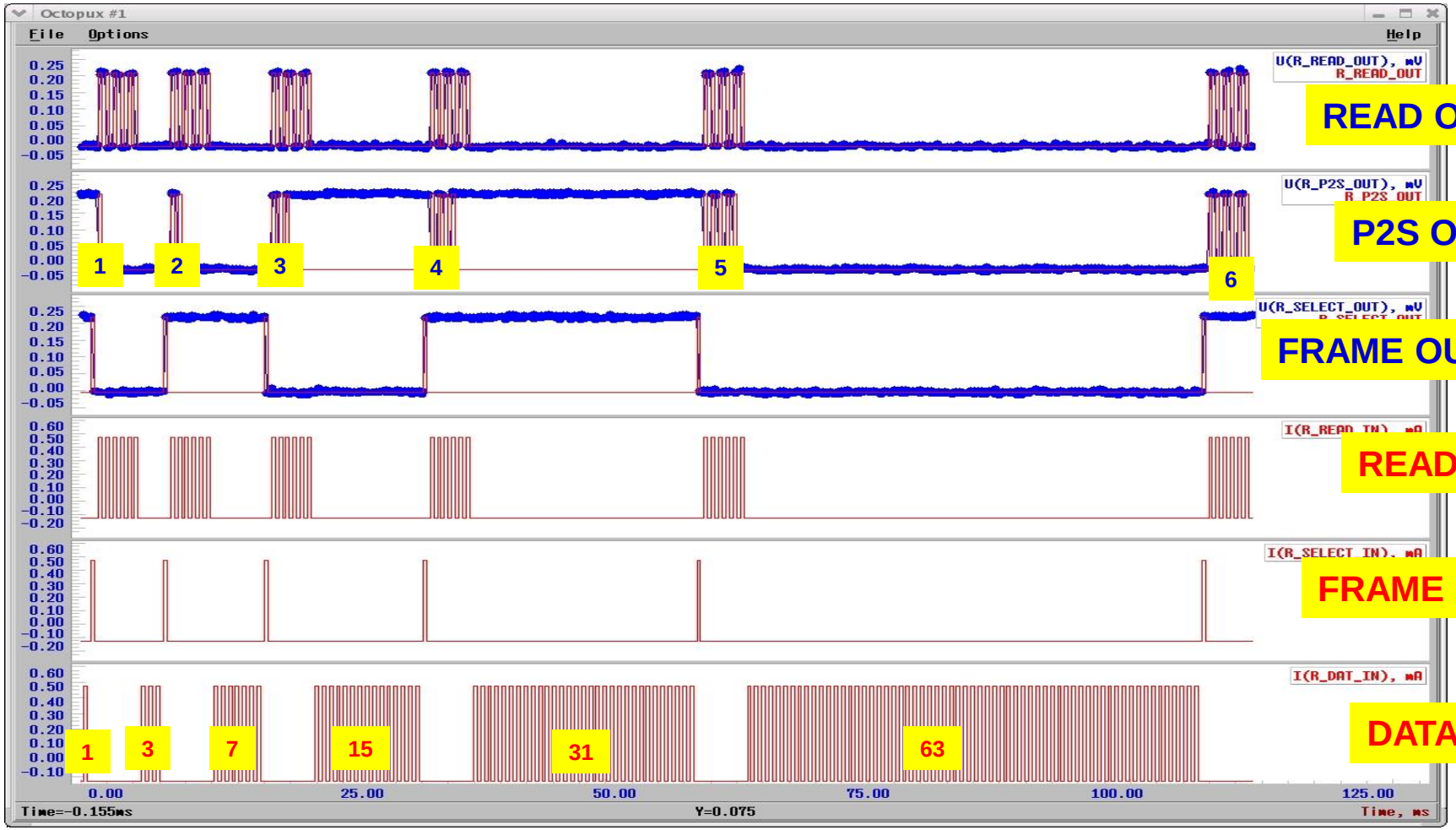


# tvl03_ed_003: 6b counter




ERSFQ counter is 22.5 times smaller in area by converting to SFQ5EE

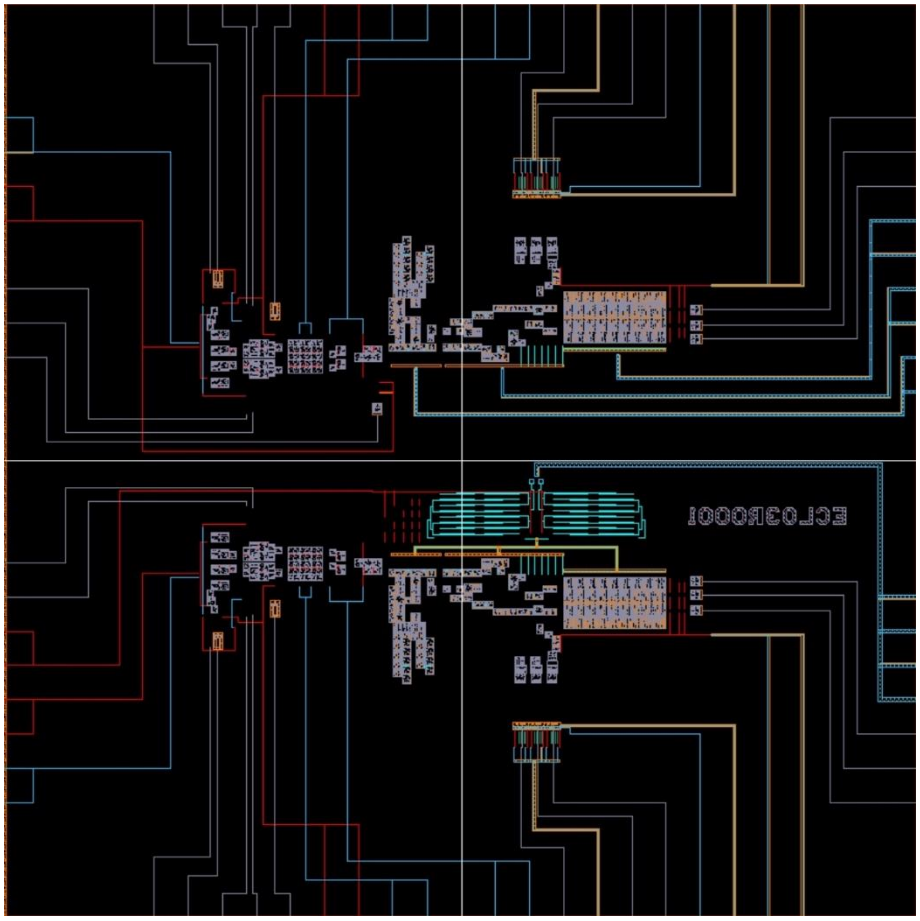
# Test Results




RSFQ margins: 41mA-68mA

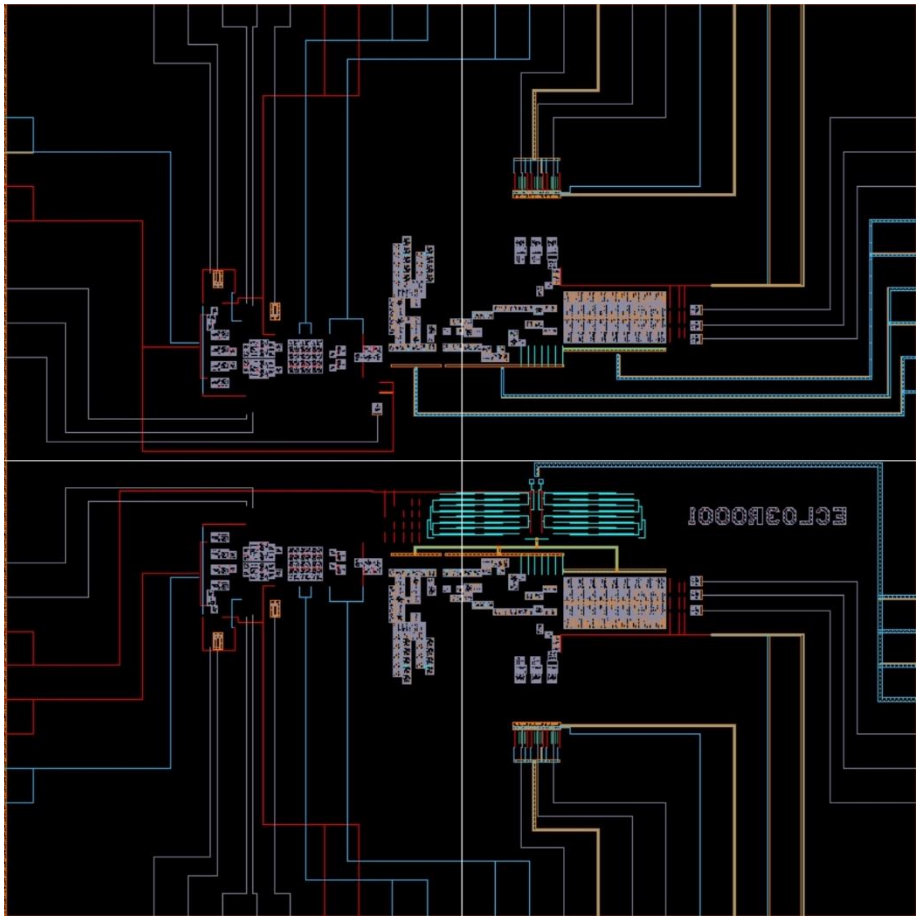
ERSFQ margins: 45mA-65mA
Critical Current 51mA

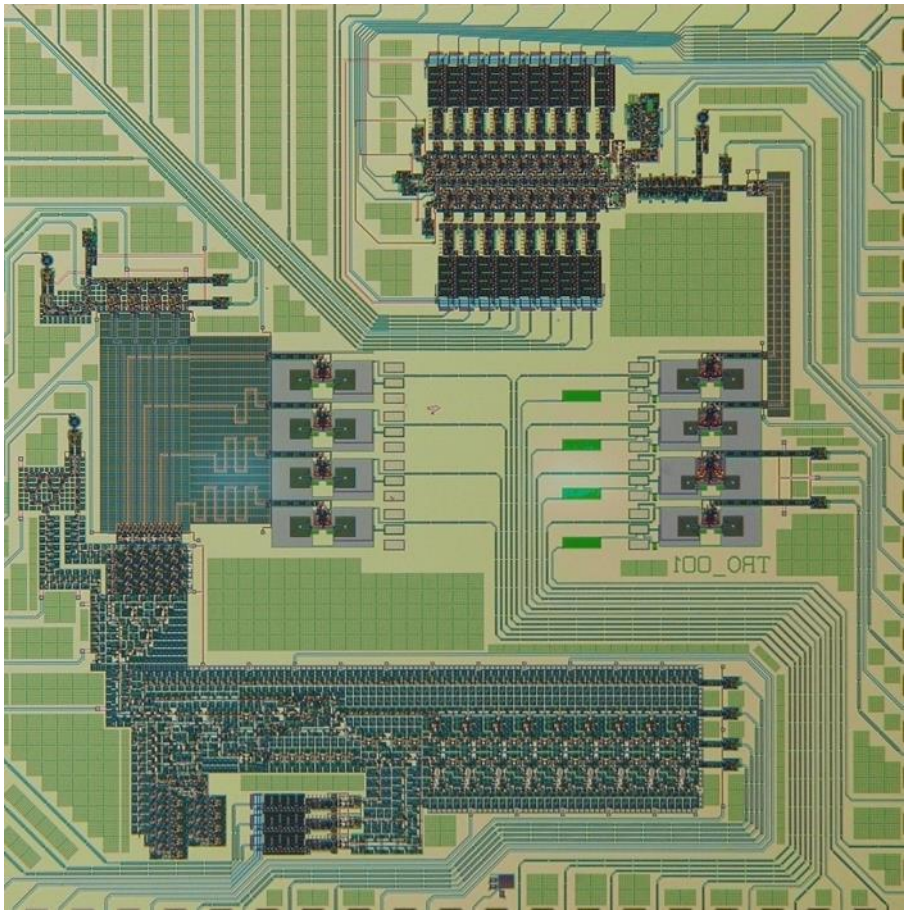
# 4-channel SNSPD Aggregating Readout Chip



**2 readouts (ERSFQ and RSFQ) are placed on the same chip**

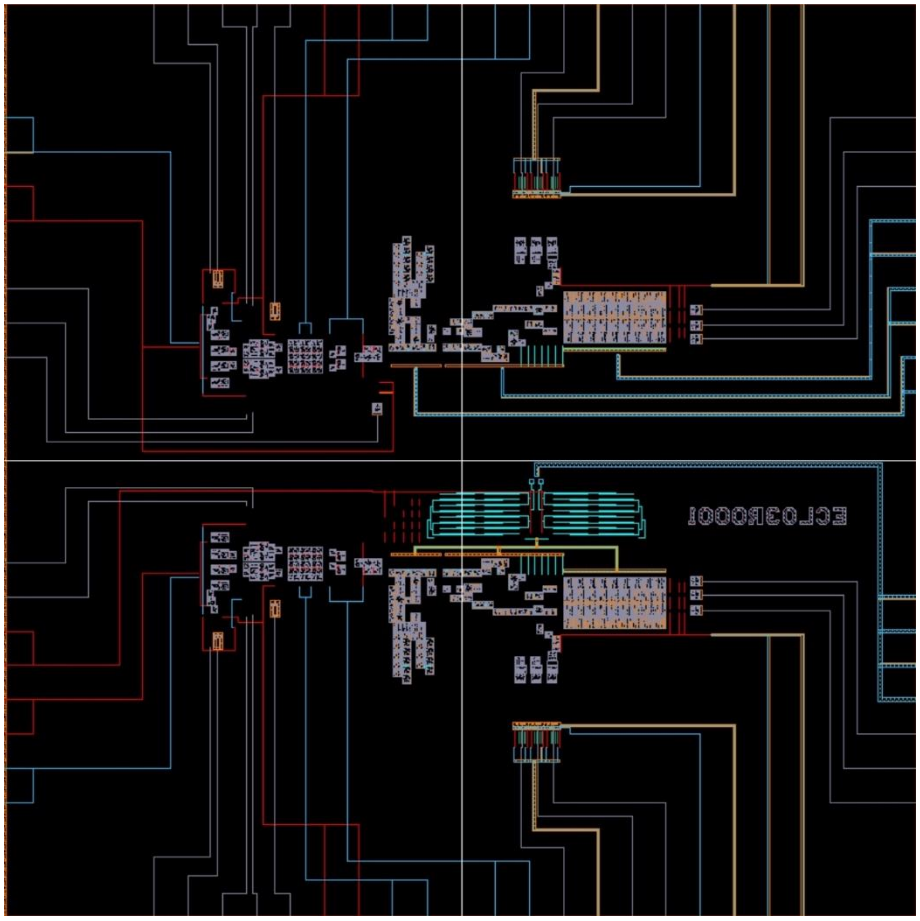
# 4-channel SNSPD Aggregating Readout Chip

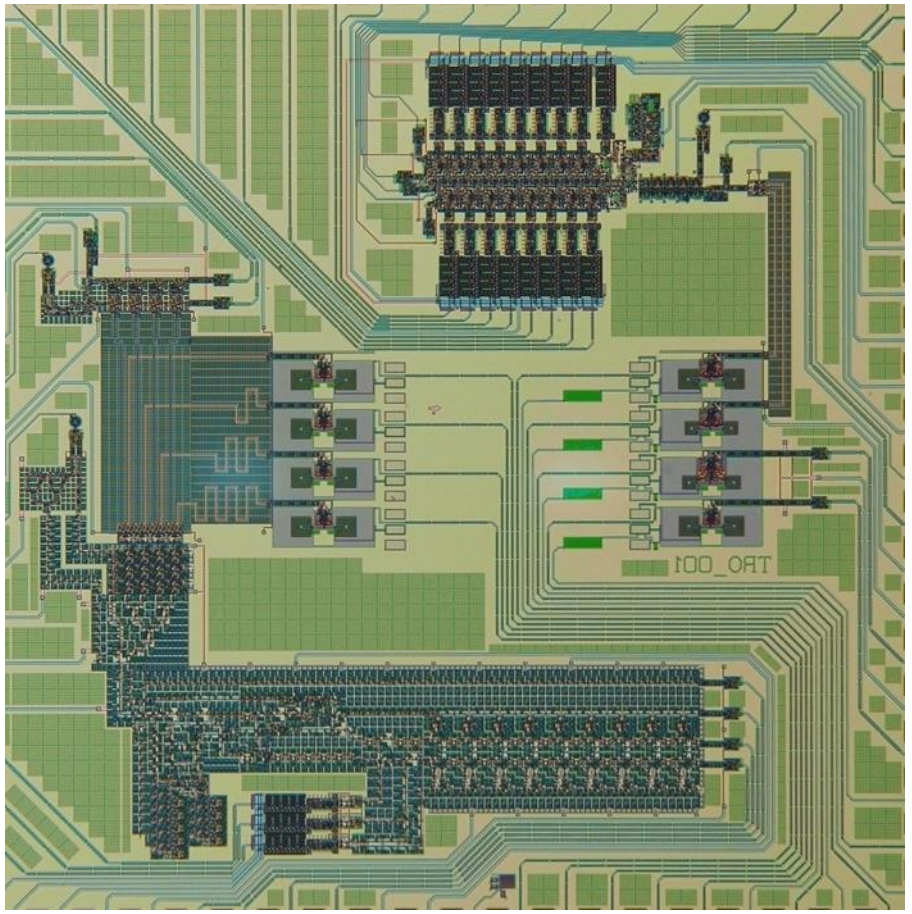




**2 readouts (ERSFQ and RSFQ) are placed on the same chip**

# 4-channel SNSPD Aggregating Readout Chip





4 mm

8.8 mm

**2 readouts (ERSFQ and RSFQ) are placed on the same chip**

# Conclusion

## Digital TDM Readout

- By means of embedded pattern generators we proved the correct operation of each channel and of all 4 channels combined at frequencies up to 12.8 GHz.
- We were able to perform reconstruction of signal applied to individual ADC.

## Time-to-Digital Readout for SNSPDs

- Current sensitivity ($\Delta I$) < 10 μA
- Preserves fast rise times (< 100 ps)
- Time-of-arrival can be measured with 30 ps digital resolution
- Low power, scalable eRFSQ circuitry
- ERSFQ digital circuit density is 22.5X higher with 8-layer MIT/LL process than 4-layer HYPRES process
- The goal of 10μW per SNSPD is reachable.

# Acknowledgment


- Digital TDM readout was supported in part by a grant from DOE office of Nuclear Physics
- TDC readout was supported by MIT/LL
- New RSFQ/ERSFQ Counters for MIT/LL SFQ5ee process was supported by a research grant from the Office of Naval Research
- The authors would like to thank
  - HYPRES and MIT/LL fab teams for fabricating the chips,
  - Andrew J. Kerman, Eric Dauler for fruitful discussions,
  - Igor Vernik for preliminary testing,
  - Denis Amparo for taking photographs.