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[Invited] Prototyping Extensible Quantum Computing Architectures

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Quantum computing architectures with ten or more quantum bits (qubits) have been implemented using trapped ions and superconducting devices. The next milestone in the quest for a quantum computer is the realization of quantum error correction codes. Such codes will require a very large number of qubits that must be controlled and measured by means of classical electronics. One architectural aspect requiring immediate attention is the realization of a suitable interconnect between the quantum and classical hardware. In this talk, I will introduce the quantum socket, a three-dimensional wiring method for qubits with superior performance as compared to two-dimensional methods based on wire bonding. The quantum socket is based on spring-mounted micro wires –the three-dimensional wires –that connect electrically to a micro-fabricated chip by pushing directly on it. The wires have a coaxial geometry and operate well over a frequency range from DC to 10 GHz. I will present a detailed characterization of the quantum socket and a proof of concept for quantum computing applications, where a quantum socket was used to measure superconducting resonators at a temperature of ˜10 mK. I will then discuss another technology for extensibility based on chip-to-chip thermo-compressive bonding. I will present a series of experiments where two chips containing superconducting devices were bonded together. In particular, I will present results for the bonding resistance at 10 mK and experiments where superconducting resonators made from indium were fabricated beneath a protective superconducting tunnel. In conclusion, I will give an outlook demonstrating how the quantum socket ands chip-to-chip bonding can be used to wire a quantum processor with a 10 × 10 qubit lattice and I will outline our present work toward the implementation of such a lattice.

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