# (O)DMB and FED upgrade for HL-LHC

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*Forward muon upgrade workshop*
*Texas A&M, College Station*

ODMB

# ODMB FGPA option

| | Current ODMBv1 2013 | Virtex-6 XC6VLX130T-1FFG1156C | | Estimated ODMBv2 2020 | Kintex-7 XC7K325T-3FFG900E | Artix-7 XC7A200T-3FFG1156E |
|---|---|---|---|---|---|---|
| **Logic (slices)** | **8.1k** | 20k | | **15k** | 51k | 33k |
| **Total RAM** | **3 Mb** | 9.5 Mb | | **6 Mb** | 16 Mb | 13 Mb |
| **Clock managers** | **2** | 10 | | **4** | 10 | 10 |
| **I/O** | **300** | 600 | | **379** | 500 | 500 |
| **Opt. transceivers** | **8 @ 3.2 Gbps** | 20 @ 5 Gbps | | **12** | 16 @ 12.5 Gbps | 16 @ 6.6 Gbps |
| **Price** | | $700-1,000 | | | $1,940 | $325 |

- The Artix-7 is much cheaper *today* than the Kintex 7
  - Only drawback seems to be links at half-speed
  - Covers needs with more fiber links
- Might save money even with prices coming down and additional CTP7 boards

# Options

- **Option A**: run all ODMB links at 10Gbs+
  - ME1/1 = 3 links
  - ME2/1 = 2 links
  - ME3/1, ME4/1 = 1 link
  - CTP7s needed = 12
  - Using VTTx in ME2/1 due to FP space constraints
  - Could fit to 11, but doesn't make sense - not a multiple of 2 (endcaps)
  - ODMB has to use Kintex7 on all boards = expensive

- **Option B**: ME1/1 at 10Gbs+, others at 6.4Gbs
  - ME1/1 = 3 links
  - ME2/1 = 2 links **(safety factor = 1.88)**
  - ME3/1 and ME4/1 = 2 links
  - **Depending on final rate numbers, might require 3 links in ME2/1 → will need more expensive 4-link TX**
  - CTP7s needed = 12
  - Only 1 spare RX left -- that's probably ok even if using multifiber "SLink" (?)
  - CTP7 cost unchanged
  - ODMB uses Kintex7 on ME1/1, Artix7 on ME2/1, ME3/1, ME4/1
  - Saves 180 k$

# Options

- **Option 3:** all ODMBs run at 6.4Gbs
  - ME1/1 = 4 links
  - ME2/1 = 2 links **(safety factor = 1.88)**
  - ME3/1, ME4/1 = 2 links
  - **Depending on final rate numbers, might require 3 links in ME2/1 → will need more expensive 4-link TX**
  - CTP7s needed = 14
  - Awkward mapping but enough links, would work
  - ODMB uses Artix7 in all cases
  - 115k savings on ME1/1 alone - compared to option 2 (excluding spares)
  - CTP7 cost goes up by 30k

- **Note:** with a small design change on CTP7 RX count could be increased to 72 (CTP7 has 13 backplane links -- not used in CSC)
  - Seems not worth it
  - Option 3 could fit to 12 boards but no RX is left for DAQ backpressure
  - Option 1 could fit to 10 boards but no RX is left for DAQ backpressure
  - May be possible to increase CTP7 RX count to ~79 in the expense of removing 12 TXs -- might be worth it (total TX count = 36)
  - Redesign costs unclear -- have to check with University of Wisconsin
  - Replace one TX MiniPOD with RX MiniPOD, possibly small routing change

# FPGA and CPT7 costs

- Current costs of ODMB FPGAs and CTP7
  - 2 k$ for Kintex7, 0.325 k$ for Artix7
  - 15 k$ for each CTP7

| Option | # Kintex7 | # Artix7 | # CTP7 | # links | k$ FPGA | k$ CTP7 | k$ sum |
|---|---|---|---|---|---|---|---|
| A | 180 | 0 | 12 | 356 | 360 | 180 | **540 k$** |
| B | 72 | 108 | 12 | 432 | 179 | 180 | **359 k$** |
| C | 0 | 180 | 14 | 504 | 59 | 210 | **269 k$** |

- Not included cost of additional fibers and µTCA crate
- Not included savings from spares (~10%)

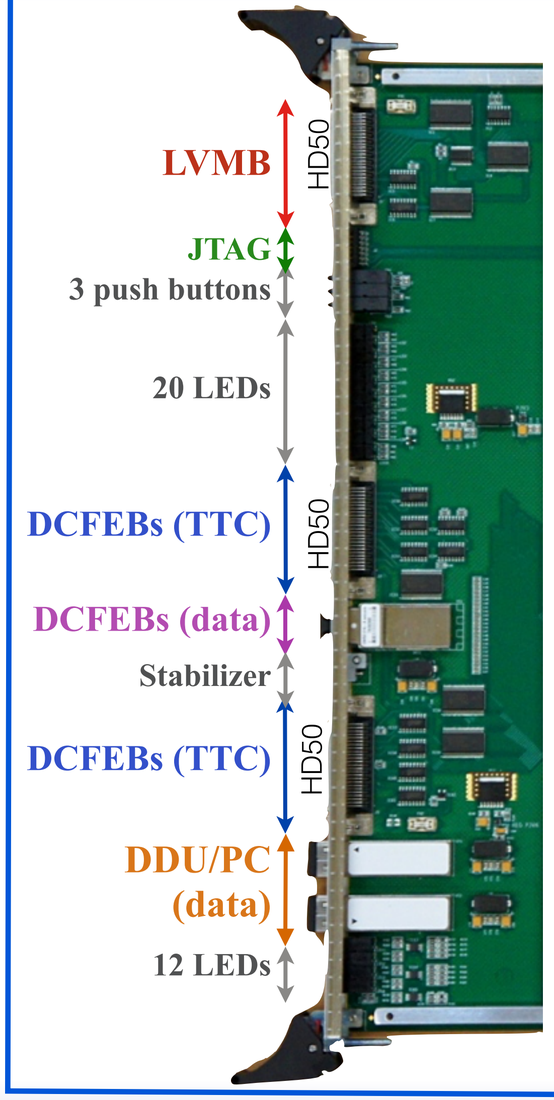
Concerns about rate or other limitations?

# Backup

# Front panel designs, opt. transceivers

Main features of PCB design quite similar in both cases

ODMBv2.1



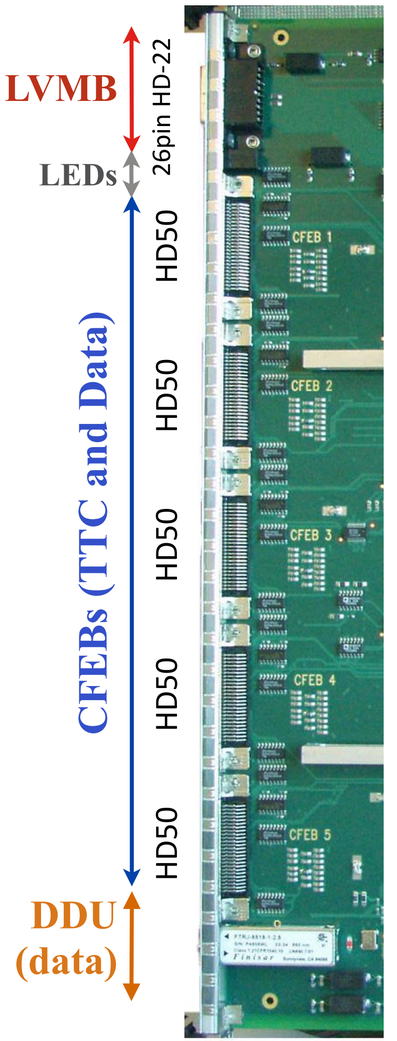

**ME1/1**

- One front panel change with respect to **ODMB 2013**
  - ✳ ***Replace 4.25 Gbps transceivers with 10+ Gbps parts***

**ME234/1**

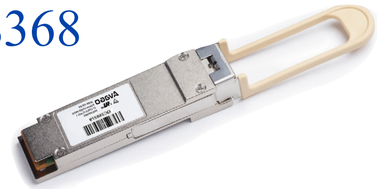
- Two front panel changes with respect to **DMB 2003**
  - ✳ ***Replace 4.25 Gbps transceivers with 10+ Gbps parts***
  - ✳ ***Remove LEDs, install snap-12***
  - ✳ ***Place JTAG connector on board***

ODMBv2.2




- Current FTLF8524E2GNL: **4.25 Gbps**, $40
- Similar Finisar transceiver FTLX8571D3BCV
  - **10.3 Gbps**, $73, **two needed for ME1/1**

- Multilane transceiver would give more flexibility
  - AFBR-79EEPZ: **four 10.3 Gbps links**, $368
  - AFBR-79FIPZ: **four 16 Gbps links**



**Design in 4-5 years → prices will come down/new tech**

# Kintex-7 product table

Kintex-7

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | Part Number | | XC7K70T | XC7K160T | XC7K325T | XC7K355T | XC7K410T | XC7K420T | XC7K480T |
| | | EasyPath™ Cost Reduction Solutions[1] | | — | — | XCE7K325T | XCE7K355T | XCE7K410T | XCE7K420T | XCE7K480T |
| Logic Resources | | Slices | | 10,250 | 25,350 | 50,950 | 55,650 | 63,550 | 65,150 | 74,650 |
| | | Logic Cells | | 65,600 | 162,240 | 326,080 | 356,160 | 406,720 | 416,960 | 477,760 |
| | | CLB Flip-Flops | | 82,000 | 202,800 | 407,600 | 445,200 | 508,400 | 521,200 | 597,200 |
| Memory Resources | | Maximum Distributed RAM (Kb) | | 838 | 2,188 | 4,000 | 5,088 | 5,663 | 5,938 | 6,788 |
| | | Block RAM/FIFO w/ ECC (36 Kb each) | | 135 | 325 | 445 | 715 | 795 | 835 | 955 |
| | | Total Block RAM (Kb) | | 4,860 | 11,700 | 16,020 | 25,740 | 28,620 | 30,060 | 34,380 |
| Clock Resources | | CMTs (1 MMCM + 1 PLL) | | 6 | 8 | 10 | 6 | 10 | 8 | 8 |
| I/O Resources | | Maximum Single-Ended I/O | | 300 | 400 | 500 | 300 | 500 | 400 | 400 |
| | | Maximum Differential I/O Pairs | | 144 | 192 | 240 | 144 | 240 | 192 | 192 |
| Integrated IP Resources | | DSP48 Slices | | 240 | 600 | 840 | 1,440 | 1,540 | 1,680 | 1,920 |
| | | PCIe® Gen2[2] | | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | | Analog Mixed Signal (AMS) / XADC | | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | | Configuration AES / HMAC Blocks | | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | | GTX Transceivers (12.5 Gb/s Max Rate) | | 8 | 8 | 16 | 24 | 16 | 32 | 32 |
| Speed Grades | | Commercial | | -1, -2 | -1, -2 | -1, -2 | -1, -2 | -1, -2 | -1, -2 | -1, -2 |
| | | Extended | | -2L, -3 | -2L, -3 | -2L, -3 | -2L, -3 | -2L, -3 | -2L, -3 | -2L, -3 |
| | | Industrial | | -1, -2 | -1, -2, -2L | -1, -2, -2L | -1, -2, -2L | -1, -2, -2L | -1, -2, -2L | -1, -2, -2L |
| | Package[3] | Dimensions (mm) | | | | **Available User I/O**: 3.3V HR I/O, 1.8V HP I/Os (GTX) | | | | |
| | FBG484 / FBV484 | 23 x 23 | | 185, 100 (4) | 185, 100 (4) | | | | | |
| Footprint Compatible | FBG676 / FBV676 | 27 x 27 | | 200, 100 (8) | 250, 150 (8) | 250, 150 (8) | | 250, 150 (8) | | |
| | FFG676 / FFV676 | 27 x 27 | | | 250, 150 (8) | 250, 150 (8) | | 250, 150 (8) | | |
| Footprint Compatible | FBG900 / FBV900 | 31 x 31 | | | | 350, 150 (16) | | 350, 150 (16) | | |
| | FFG900 / FFV900 | 31 x 31 | | | | 350, 150 (16) | | 350, 150 (16) | | |
| | FFG901 / FFV901 | 31 x 31 | | | | | 300, 0 (24) | | 380, 0 (28) | 380, 0 (28) |
| | FFG1156 / FFV1156 | 35 x 35 | | | | | | | 400, 0 (32) | 400, 0 (32) |

XMP085 (v3.8)

**FBG / FBV:** 1.0 mm Lidless flip-chip; **FFG / FFV**: 1.0 mm Flip-chip fine-pitch

# Artix-7 product table

| | | | **Artix®-7 FPGAs**<br>Optimized for Lowest Cost and Lowest Power Applications<br>(1.0V, 0.95V, 0.9V) | | | | | |
|---|---|---|---|---|---|---|---|---|
| | Part Number | | XC7A15T | XC7A35T | XC7A50T | XC7A75T | XC7A100T | XC7A200T |
| Logic Resources | Logic Cells | | 16,640 | 33,280 | 52,160 | 75,520 | 101,440 | 215,360 |
| | Slices | | 2,600 | 5,200 | 8,150 | 11,800 | 15,850 | 33,650 |
| | CLB Flip-Flops | | 20,800 | 41,600 | 65,200 | 94,400 | 126,800 | 269,200 |
| Memory Resources | Maximum Distributed RAM (Kb) | | 200 | 400 | 600 | 892 | 1,188 | 2,888 |
| | Block RAM/FIFO w/ ECC (36 Kb each) | | 25 | 50 | 75 | 105 | 135 | 365 |
| | Total Block RAM (Kb) | | 900 | 1,800 | 2,700 | 3,780 | 4,860 | 13,140 |
| Clock Resources | CMTs (1 MMCM + 1 PLL) | | 5 | 5 | 5 | 6 | 6 | 10 |
| I/O Resources | Maximum Single-Ended I/O | | 250 | 250 | 250 | 300 | 300 | 500 |
| | Maximum Differential I/O Pairs | | 120 | 120 | 120 | 144 | 144 | 240 |
| Embedded Hard IP Resources | DSP Slices | | 45 | 90 | 120 | 180 | 240 | 740 |
| | PCIe® Gen2[1] | | 1 | 1 | 1 | 1 | 1 | 1 |
| | Analog Mixed Signal (AMS) / XADC | | 1 | 1 | 1 | 1 | 1 | 1 |
| | Configuration AES / HMAC Blocks | | 1 | 1 | 1 | 1 | 1 | 1 |
| | GTP Transceivers (6.6 Gb/s Max Rate)[2] | | 4 | 4 | 4 | 8 | 8 | 16 |
| Speed Grades | Commercial | | -1, -2 | -1, -2 | -1, -2 | -1, -2 | -1, -2 | -1, -2 |
| | Extended | | -2L, -3 | -2L, -3 | -2L, -3 | -2L, -3 | -2L, -3 | -2L, -3 |
| | Industrial | | -1, -2, -1L | -1, -2, -1L | -1, -2, -1L | -1, -2, -1L | -1, -2, -1L | -1, -2, -1L |
| | Package[3], [4] | Dimensions (mm) | **Available User I/O**: 3.3V SelectIO™ HR I/O (GTP Transceivers) | | | | | |
| | CPG236 | 10 x 10 | 106 (2) | 106 (2) | 106 (2) | | | |
| | CSG324 | 15 x 15 | 210 (0) | 210 (0) | 210 (0) | 210 (0) | 210 (0) | |
| | CSG325 | 15 x 15 | 150 (4) | 150 (4) | 150 (4) | | | |
| | FTG256 | 17 x 17 | 170 (0) | 170 (0) | 170 (0) | 170 (0) | 170 (0) | |
| | SBG484 / SBV484 | 19 x 19 | | | | | | 285 (4) |
| Footprint Compatible | FGG484 | 23 x 23 | 250 (4) | 250 (4) | 250 (4) | 285 (4) | 285 (4) | |
| | FBG484 / FBV484 | 23 x 23 | | | | | | 285 (4) |
| Footprint Compatible | FGG676 | 27 x 27 | | | | 300 (8) | 300 (8) | |
| | FBG676 / FBV676 | 27 x 27 | | | | | | 400 (8) |
| | FFG1156 / FFV1156 | 35 x 35 | | | | | | 500 (16) |

XMP086 (v4.7)

**CPG**: 0.5 mm Wire-bond chip-scale; **CSG**: 0.8 mm Wire-bond chip-scale; **FTG**: 1.0 mm Wire-bond fine-pitch; **SBG / SBV**: 0.8 mm Lidless flip-chip; **FGG**: 1.0 mm Wire-bond fine-pitch; **FBG / FBV** 1.0 mm Lidless flip-chip; **FFG / FFV**: 1.0 mm Flip-chip fine-pitch

Artix7 to be used, 16 MGT

# Virtex-6 product table

Current ODMB

| | Part Number | XC6VLX75T | XC6VLX130T | XC6VLX195T | XC6VLX240T | XC6VLX365T | XC6VLX550T | XC6VLX760 | XC6VSX315T | XC6VSX475T | XC6VHX250T | XC6VHX255T | XC6VHX380T | XC6VHX565T |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | EasyPath™ FPGA Cost Reduction Solutions[1] | XCE6VLX75T | XCE6VLX130T | XCE6VLX195T | XCE6VLX240T | XCE6VLX365T | XCE6VLX550T | XCE6VLX760 | XCE6VSX315T | XCE6VSX475T | XCE6VHX250T | XCE6VHX255T | XCE6VHX380T | XCE6VHX565T |
| Logic Resources | Slices[2] | 11,640 | 20,000 | 31,200 | 37,680 | 56,880 | 85,920 | 118,560 | 49,200 | 74,400 | 39,360 | 39,600 | 59,760 | 88,560 |
| | Logic Cells[3] | 74,496 | 128,000 | 199,680 | 241,152 | 364,032 | 549,888 | 758,784 | 314,880 | 476,160 | 251,904 | 253,440 | 382,464 | 566,784 |
| | CLB Flip-Flops | 93,120 | 160,000 | 249,600 | 301,440 | 455,040 | 687,360 | 948,480 | 393,600 | 595,200 | 314,880 | 316,800 | 478,080 | 708,480 |
| Memory Resources | Maximum Distributed RAM (Kb) | 1,045 | 1,740 | 3,040 | 3,650 | 4,130 | 6,200 | 8,280 | 5,090 | 7,640 | 3,040 | 3,050 | 4,570 | 6,370 |
| | Block RAM/FIFO w/ECC (36 Kb each) | 156 | 264 | 344 | 416 | 416 | 632 | 720 | 704 | 1,064 | 504 | 516 | 768 | 912 |
| | Total Block RAM (Kb) | 5,616 | 9,504 | 12,384 | 14,976 | 14,976 | 22,752 | 25,920 | 25,344 | 38,304 | 18,144 | 18,567 | 27,648 | 32,832 |
| Clock Resources | Mixed-Mode Clock Managers (MMCM) | 6 | 10 | 10 | 12 | 12 | 18 | 18 | 12 | 18 | 12 | 12 | 18 | 18 |
| I/O Resources[4,5] | Maximum Single-Ended I/O | 360 | 600 | 600 | 720 | 720 | 1,200 | 1,200 | 720 | 840 | 320 | 480 | 720 | 720 |
| | Maximum Differential I/O Pairs | 180 | 300 | 300 | 360 | 360 | 600 | 600 | 360 | 420 | 160 | 240 | 360 | 360 |
| Embedded Hard IP Resources[6] | DSP48E1 Slices | 288 | 480 | 640 | 768 | 576 | 864 | 864 | 1,344 | 2,016 | 576 | 576 | 864 | 864 |
| | PCI Express® Interface Blocks | 1 | 2 | 2 | 2 | 2 | 2 | — | 2 | 2 | 4 | 2 | 4 | 4 |
| | 10/100/1000 Ethernet MAC Blocks | 4 | 4 | 4 | 4 | 4 | 4 | — | 4 | 4 | 4 | 2 | 4 | 4 |
| | GTX Low-Power Transceivers | 12 | 20 | 20 | 24 | 24 | 36 | — | 24 | 36 | 48 | 24 | 48 | 48 |
| | GTH High-Speed Transceivers | — | — | — | — | — | — | — | — | — | — | 24 | 24 | 24 |
| Speed Grades | Commercial | -L1, -1, -2, -3 | -L1, -1, -2, -3 | -L1, -1, -2, -3 | -L1, -1, -2, -3 | -L1, -1, -2, -3 | -L1, -1, -2 | -L1, -1, -2 | -L1, -1, -2, -3 | -L1, -1, -2 | -1, -2, -3 | -1, -2, -3 | -1, -2, -3 | -1, -2 |
| | Extended | — | — | — | — | — | -2 | -2 | — | -2 | — | — | -2 | -2 |
| | Industrial | -L1, -1, -2 | -L1, -1, -2 | -L1, -1, -2 | -L1, -1, -2 | -L1, -1, -2 | -L1, -1 | -L1, -1 | -L1, -1, -2 | -L1, -1 | -1, -2 | -1, -2 | -1, -2 | -1 |
| Configuration | Configuration Memory (Mb) | 26.3 | 43.8 | 61.6 | 73.9 | 96.1 | 144.1 | 184.9 | 104.5 | 156.7 | 79.9 | 79.9 | 119.8 | 160.7 |
| Package[7] | Area | Available User I/O: SelectIO™ Interface Pins[4, 5] (GTX Low-Power Transceivers, GTH High-Speed Transceivers) | | | | | | | | | | | | |
| FFA Packages (FF): Flip-chip, fine-pitch BGA (1.0 mm ball spacing) | | | | | | | | | | | | | | |
| FF484 | 23 x 23 mm | 240 (8, 0) | 240 (8, 0) | | | | | | | | | | | |
| FF784 | 29 x 29 mm | 360 (12, 0) | 400 (12, 0) | 400 (12, 0) | 400 (12, 0) | | | | | | | | | |
| FF1156 | 35 x 35 mm | | 600 (20, 0) | 600 (20, 0) | 600 (20, 0) | 600 (20, 0) | | | 600 (20, 0) | 600 (20, 0) | | | | |
| FF1759 | 42.5 x 42.5 mm | | | | 720 (24, 0) | 720 (24, 0) | 840 (36, 0) | | 720 (24, 0) | 840 (36, 0) | | | | |
| FF1760 | 42.5 x 42.5 mm | | | | | | 1,200 (0, 0) | 1,200 (0, 0) | | | | | | |
| FF1154 | 35 x 35 mm | | | | | | | | | | 320 (48, 0) | | 320 (48, 0) | |
| FF1155 | 35 x 35 mm | | | | | | | | | | | 440 (24, 12) | 440 (24, 12) | |
| FF1923 | 45 x 45 mm | | | | | | | | | | | 480 (24, 24) | 720 (40, 24) | 720 (40, 24) |
| FF1924 | 45 x 45 mm | | | | | | | | | | | | 640 (48, 24) | 640 (48, 24) |

XMP068 (v1.3)

Notes:
1. EasyPath FPGAs provide a conversion-free, low-risk path for volume production.
2. A single Virtex-6 FPGA CLB comprises two slices, each containing four 6-input LUTs and eight flip-flops (twice the number found in a Virtex-4 FPGA slice), for a total of eight 6-input LUTs and 16 flip-flops per CLB.
3. Virtex-6 FPGA logic cell ratings reflect the increased logic capacity offered by the 6-input LUT architecture.
4. Digitally Controlled Impedance (DCI) is available on I/Os of all devices.
5. Supported I/O standards include: HT, LVCMOS (1.2V, 1.5V, 1.8V, 2.5V), HSTL I (1.2V,1.5V,1.8V), HSTL II (1.5V,1.8V), HSTL III (1.5V,1.8V), LVDS, Extended LVDS, RSDS, Bus LVDS, LVPECL, SSTL I (1.8V, 2.5V), SSTL II (1.8V, 2.5V), and SSTL (1.5V).
6. One System Monitor block is included in all devices.