

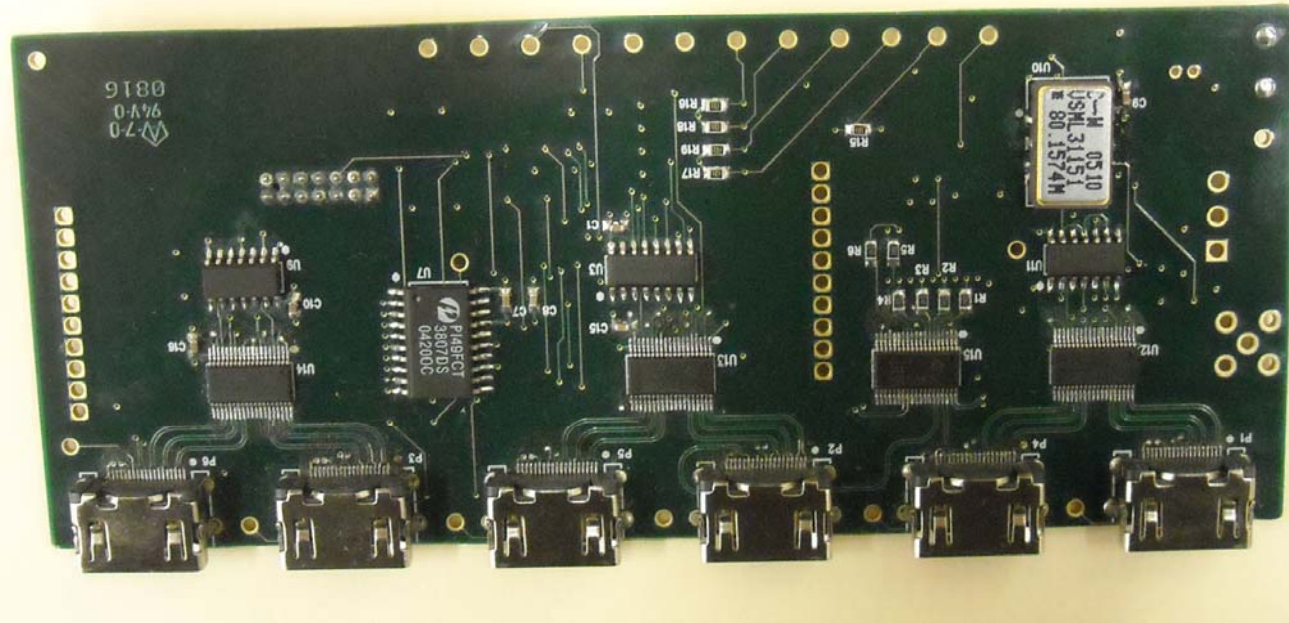
CCB to OH Link Status

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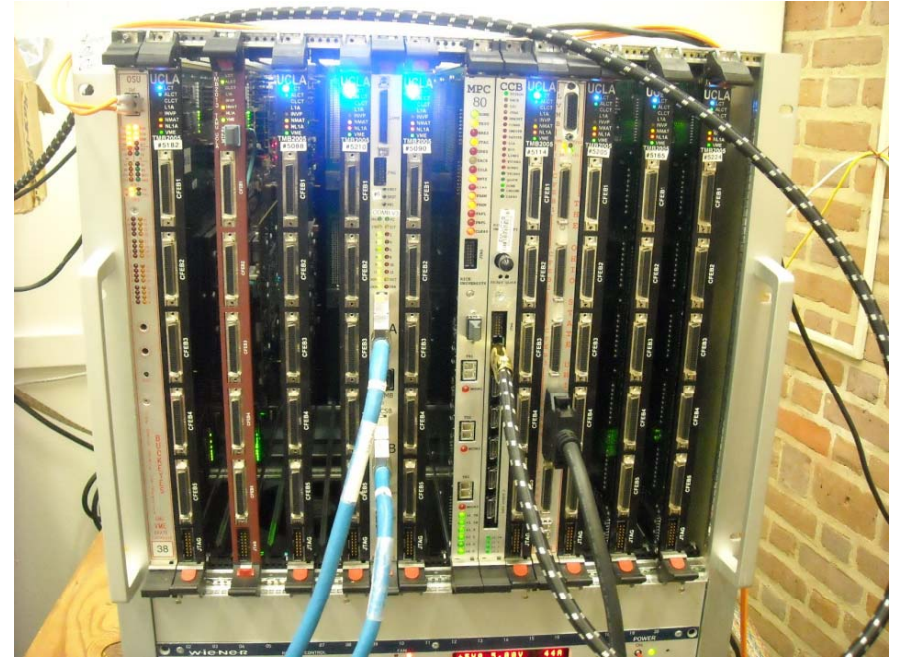
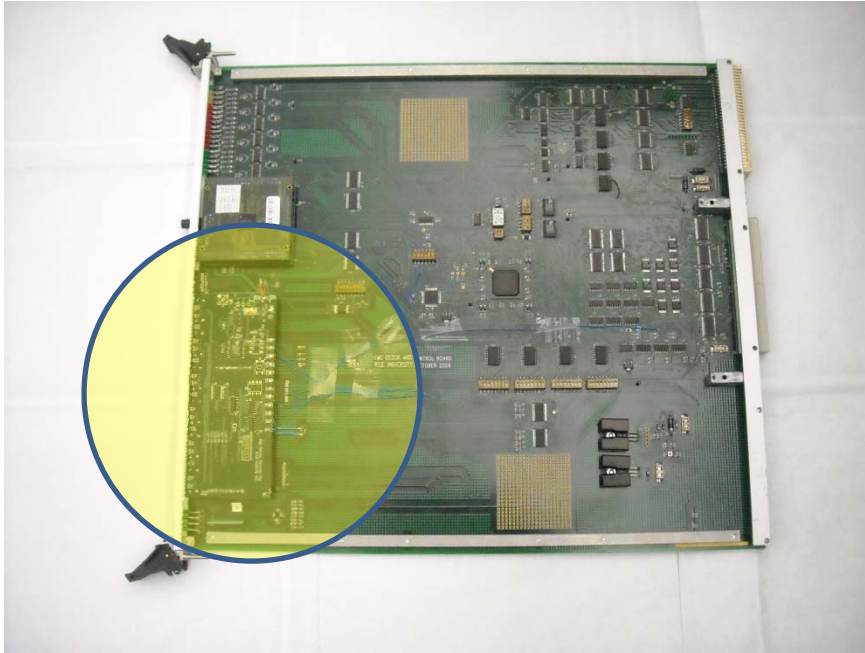
December 7, 2016

Mezzanine Board



- **Can be used as a mezzanine on top of the CCB baseboard or as a standalone board with external PS**
- **Six HDMI channels to Optohybrid v2b board**
 - 5 twisted pairs in each cable to carry 40.08MHz clock, TMS, TCK, TDI and TDO signals in LVDS levels
 - 2 single ended lines (Hard Reset and MUX_CONTROL to select the JTAG path on the OH)
- **40.08MHz clock comes from either CCB baseboard (TTC) or crystal oscillator (standalone version)**
- **JTAG path is either from CCB baseboard or Xilinx compatible 14-pin connector (standalone version)**
- **Hard Reset originates from either CCB baseboard or push button (standalone version)**
- **Mezzanine specification and firmware for the modified CCB are available at <https://padley.rice.edu/cms/projects.html#ccbgem>**

Modified CCB Board



- **10 CCB mezzanine boards were assembled and tested in spring 2016**
 - 6 mezzanines installed on CCB baseboards (TAMU, Rice, 4 boards at CERN)
 - 4 standalone boards (Rice, TAMU, Brussels)
- **10 more CCB mezzanines were fabricated and assembled in November 2016**
 - for UCLA and other test stands, more spares (both mezzanine and standalone versions)

Software Tools

The screenshot shows a web browser window with the following content:

- Address bar: `http://bo...%27s+FPGA`
- Search bar: `bonner-utca.rice.edu:20011/um:xdaq-application:lid=30/GEMreadFPGAAsysmon?GEM=`
- GEM Tests** section:
 - Choose GEM: `GEM 1` | `Read FPGA IDCode & Status from OptoHybrid board`
 - Choose GEM: `GEM 1` | `Read SYSMON from OptoHybrid board's FPGA`
 - Choose GEM: `GEM 1` | `Program OptoHybrid board's FPGA`
/home/liu/firmware/ccb/gem_ohv2.mcs
 - Choose GEM: `GEM 1` | `Load firmware to OptoHybrid board's EPROM`
/home/liu/firmware/ccb/gem_ohv2.svf
 - `HardReset to all OptoHybrid boards`
 - `Set MUX bit to GBT` | `Set MUX bit to CCB`
- CCB Tests output:

```
CCB Tests output:
FPGA IDCODE=6424a093
FPGA STATUS=5d07cfc, Done bit=1
FPGA Core Temperature: 38.8814
FPGA Voltage(ccint): 0.993164
FPGA Voltage(ccaux): 2.48438
```
- Buttons: `Log output` | `Clear`

- **Part of EMU online software (CCB tests)**

- **Access to 6 OHs**
 - **Read FPGA IDCODE and Status register**
 - **Read SYSMON from FPGA (voltages, core temperature)**
 - **Program FPGA (~3 min)**
 - **Program EPROM (~24 min)**
 - **Hard Reset**
 - **Set MUX bit on OH board to either CCB or GBT paths for JTAG access**