LCT Comparator Production & Testing

USCMS Muon Upgrade Meeting

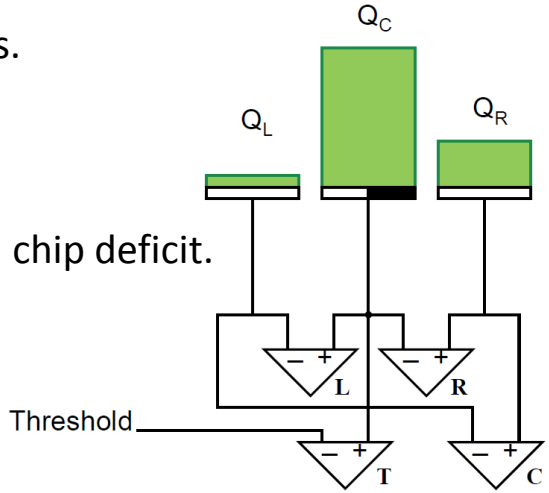
December 6, 2016

Introduction

- Inner chamber CFEBs (ME234/1) will need to be replaced:
  - Limitations in SCA storage and DAQ bandwidth
  - Will be retrofitted with 540 “DCFEB+”s.

- CFEB triggering is based on the LCT-Comparator chip:
  (Designed by UCLA and J-C Santiard at the CERN electronics group around 1997 – 2001)

- Each chip comprises a network of 50 comparators (3 per channel + 1 each to connect to neighboring boards) and a digital logic section
- Infers a half-strip position, and generate serialized “triad” trigger outputs for 32 half-strips.
- Despite its age, still performs well compared to digital options:
  - ADCs introduce latency---DCFEBs already slow due to optical links.
  - (cf. B. Bylsma “DCFEB+ design considerations”).



- The only problem: **not enough comparator ASICs..** We have an ~883 chip deficit.

- Fortunately: the process and IP for the original chip still exist and, and we can make more without difficulty or very expensive reengineering.

Fabrication

- The LCT-Comparator was designed in a now very old 0.7um CMOS n-well process.
  - Process created circa 1994 by Alcatel-Mietec in Belgium. Has since changed hands multiple times, and now owned by ON-Semiconductor.

- Original mask set was scrapped in late 2013, but the GDSII layout files were found in ON-Semi's archive.

- We have been working with the Belgian institute IMEC (who handled the original chips) to arrange for fabrication and encapsulation of new LCT-Comparators.

- Chip will be identical to the original.
- Encapsulation by ASE Inc., in Taiwan.
  - Some differences in encapsulation material/die bond/coating from the original production
  - Original fabrication just used the standard material and coating --- no special requirements were noted.

Fabrication

- Submitted the order more than 1 year ago, only to find out that ASE had discontinued the TQFP-64 package as an “open-tool” option (“open tool” options are already setup, minimizing NRE)
- After searching for (and failing to find) another vendor offering the same package, we decided to pay for retooling (an extra ~$30,000).
    - Alternative packages were available and explored but the engineering challenges presented by layout changes are significant.

- New order is submitted… processing through UCLA’s finance department.

- Order is for 11 wafers total
    - Approximately 290 chips each (depends on losses in the dicing scheme---actual wafer has more).
    - 11*290 = 3190.. Accounting for a worst case yield of 50% leaves 1595 (enough for our new DCFEBs + spares)
    - Likely yields will be higher --- this is a very mature process.

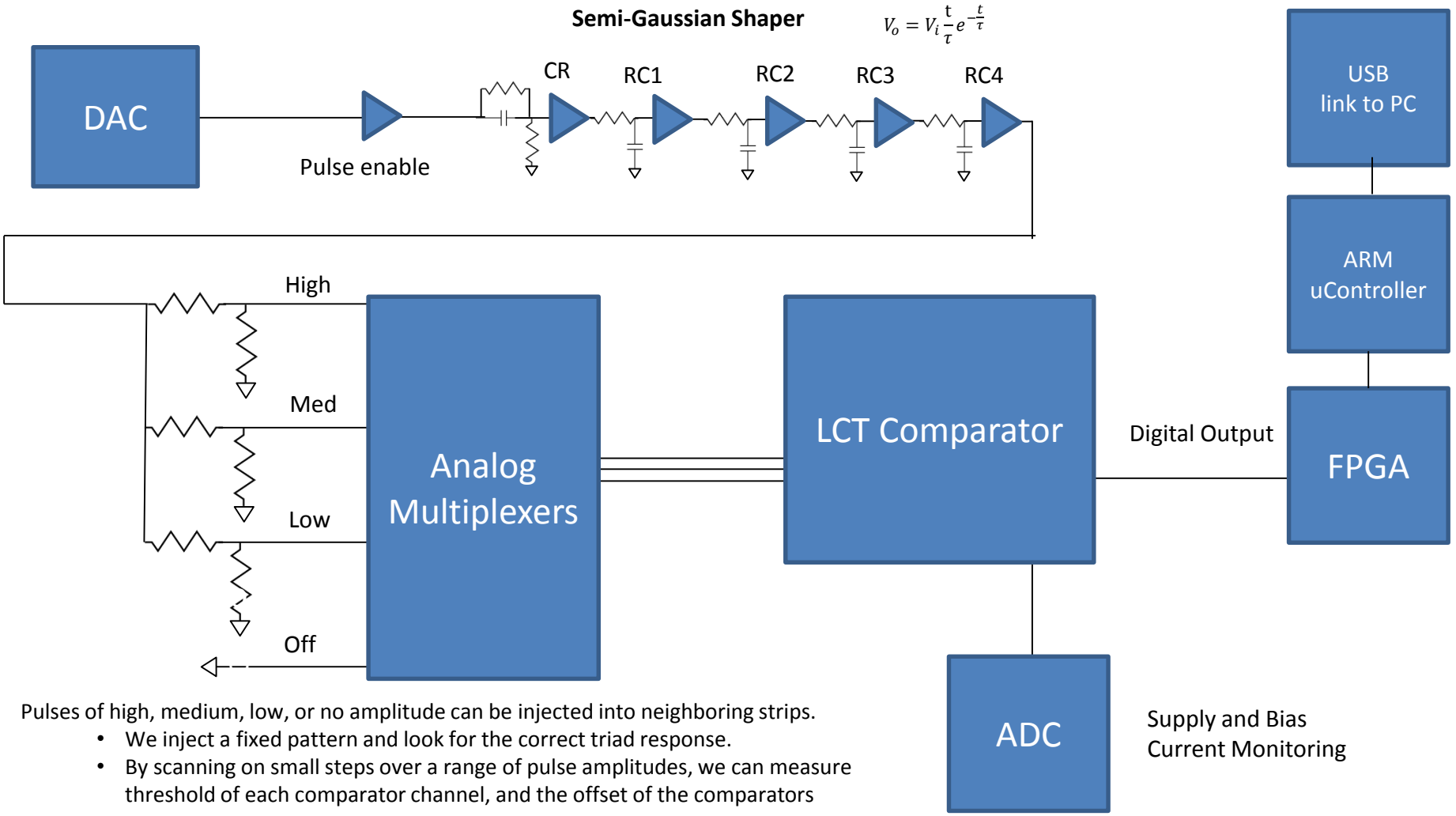
Testing

- Original comparator testing was based around a custom test PCB, controlled by digital chip testing system in the CERN electronics group, with pulses generated by a high speed DAC module.
  - The schematics and some documentation from the test PCB were found, but the remainder of the test setup is long gone.
  - New test board was designed based on the original schematics and test routines.
  - Replaced chip testing mainframe with a small Spartan-6 FPGA + microcontroller

- Basics of firmware and software are developed (communication, pulsing, readout)
- Need to continue software development of the actual test (I've been procrastinating)

- Testing procedure measures and logs:
  - Channel thresholds (for a fixed threshold, how large does the pulse need to be to see strip response?)
  - Comparator offsets (how large does the L>R amplitude difference need to be to see the correct halfstrip response)
  - Supply currents (+3.3VD, +5VA)
  - Bias currents

Simplified Schematic



Pulses of high, medium, low, or no amplitude can be injected into neighboring strips.

- We inject a fixed pattern and look for the correct triad response.
- By scanning on small steps over a range of pulse amplitudes, we can measure threshold of each comparator channel, and the offset of the comparators