GEM Opto-Hybrid Board Design for GE1/1

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USCMS Phase-2

Forward Muon Upgrade Workshop

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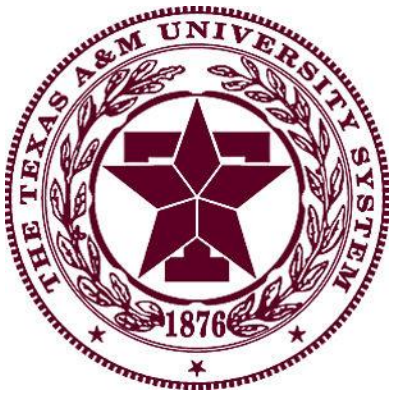
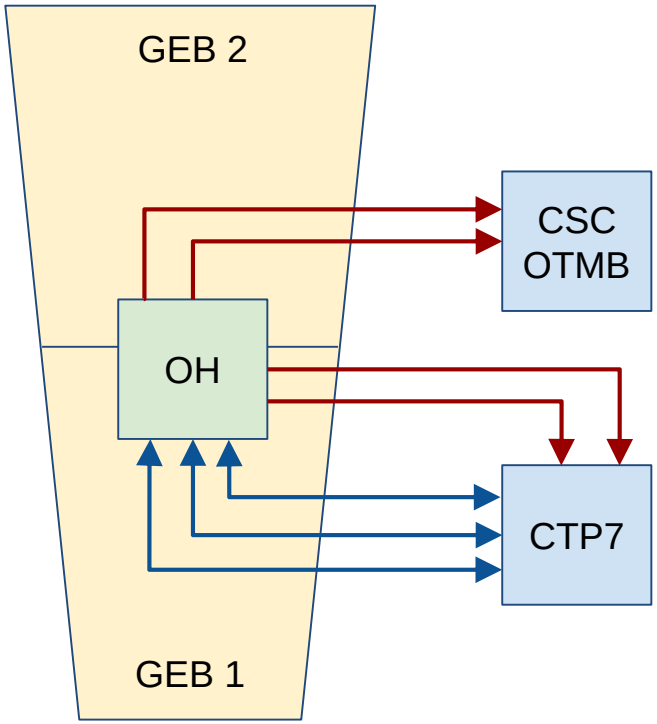


Opto-Hybrid Fiber Link Connection Requirements

GE1/1:
10 degree chamber
Total: 144 chambers

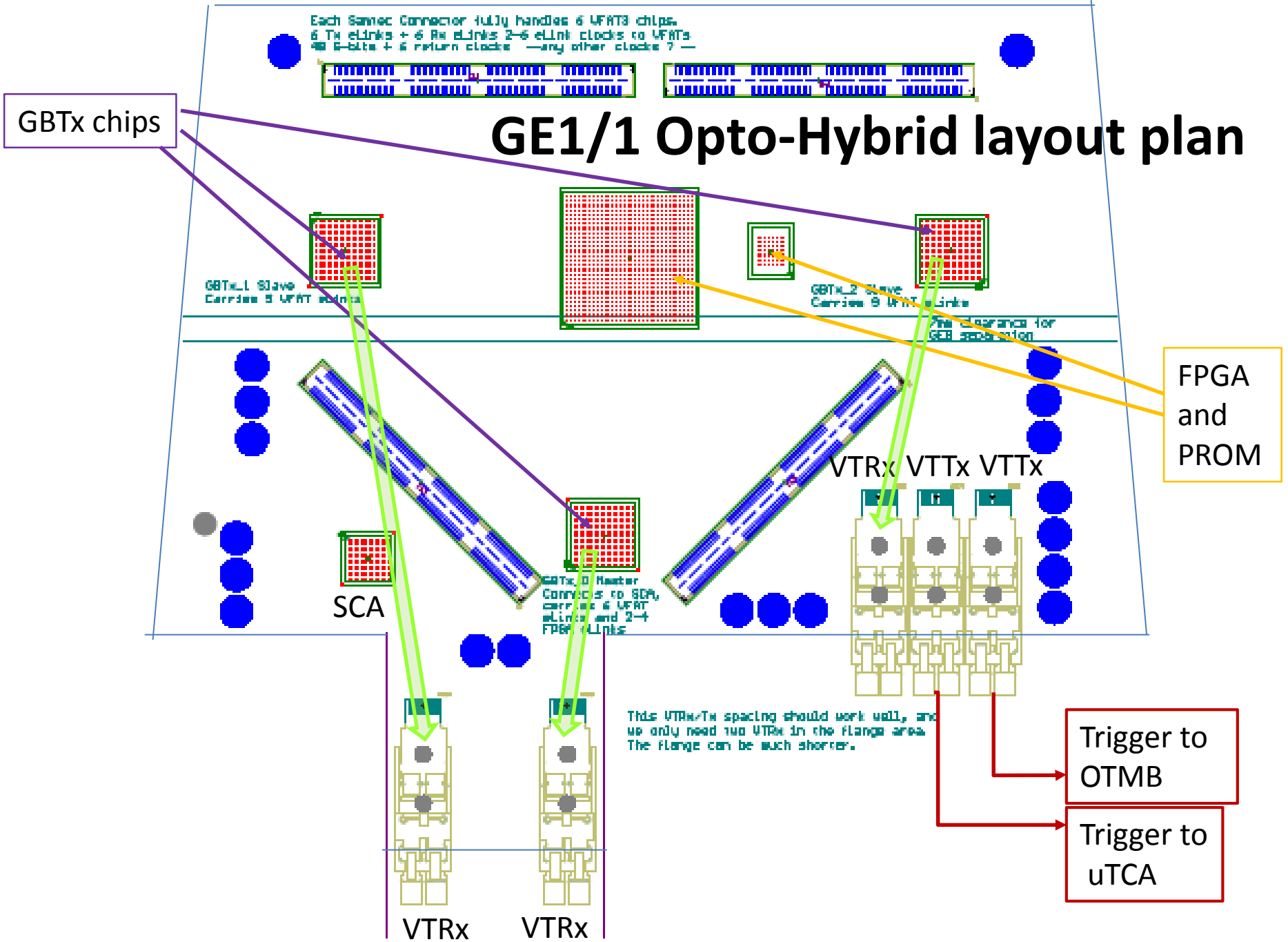


Trigger links

GBT links

- GE1/1 OH boards have 3 GBTx chips and 3 VTRx
  - Bidirectional duplex
  - Uses Versalink protocol, not 8b10b
  - These are dedicated for VFAT3 data & control interface
    - ➢ Each GBTx supports 10 e-link groups
      - A GBTx can handle data and control for maximum 10 VFAT3 chips
- OH also has a pair of VTTx devices
  - These carry trigger cluster data to OTMB and GEM uTCA
  - Each fiber can carry 4 trigger clusters per BX
    - ➢ 3.2 gbps 8b10b links

GE1/1 Opto-Hybrid layout plan



The Technical Complexities -- I

- GBTx uses an embedded Versalink protocol for the fiber link transfers
  - 4.8 gbps → 3.2 gbps data + 1.6 gbps control
    - Data and control fields in the stream are precisely defined
- GBTx i/o at the OH side include 10 e-link pairs (transmit and receive) that run at 320 mpbs (on GE1/1 and GE2/1)
  - There is also a clock output for each e-link
    - So one e-link is really 3 differential pairs
- Each VFAT3 ASIC requires an e-link pair for control and tracking data transmission
  - Thus, each GBTx can handle up to 10 VFAT3 chips

- The hard part: the 320 mbps e-link signals run from VFAT3, across the GEB (~40 cm) through the Samtec high-speed connectors onto the OH board, and finally to the GBTx
  - Impedance balance and signal quality area a big concern

→ For GE1/1 with split GEB, it should be OK

The Technical Complexities -- II

- The trigger pad bits (called s-bits) come from each VFAT3 at 320 mbps and go to the FPGA: i/o constraints are tight
  - It is 8 differential data pairs plus one clock from each VFAT3
    - That is 432 i/o pins at the FPGA already, plus we have ~50 dedicated PROM BPI pins, a few clock inputs, and other control signals for FPGA
    - We probably need to go a bit beyond 500 i/o altogether in baseline design
  - For sure we can fit this in a Virtex-6, but trying to conserve i/o to use an Artix-7 (only has 500 pins max)
    - Motivated by potential PROM radiation problem
  - Maybe we could use free GBTx e-link groups in place of PROM
    - Slowed down to 40 MHz with 16-bits, it can directly drive FPGA data/program pins
      - In this way we would not even need any PROM! This also saves i/o pins.
        - » This is the best solution for time constraints: no rad testing required!
- Inside FPGA, s-bit signals must be deserialized at every BX
  - The s-bit signal distances from VFAT3 to FPGA are all different
    - There will be phase differences to compensate
    - Somehow we need to deserialize all 8*24 VFAT3 s-bits signals and syne them to the LHC clock inside the FPGA
      - Probably will use iodelay option for 1-3 ns delay in the FPGA inputs

Summary

- We are in sort of holding pattern for now while waiting for confirmed PROM rad test results
  - We know what to do if the Xilinx PROM is OK
    - In this case nothing needs rad testing
  - Also have some ideas if the Xilinx PROM is bad
    - This will require rad testing for some new parts, or...
    - ….maybe we remove the PROM and use GBTx e-link groups instead?

- We hope to have 2 prototype V3 boards in Feb 2017
  - If they pass performance tests then we'll build 6 more for other test stands to use in R&D efforts
    - We will need GEBv3 and VFAT3 boards to do the performance testing

- Goal is to have first production OH boards delivered to Cern early in summer 2017

Bonus slides follow….

GEM V3 LV Supply Guidelines

Voltage Supply Name	Max Voltage Tolerance & Range	Max (Min) Current Required, worst case	Suggested Minimum Track Width on GEB	Predicted Worst Case Voltage Drop Across GEB*	Maximum Safe Voltage Drop**
1.0V_int	5% 0.95 - 1.05 V	4.0 A (0.5 A)	63 mm	40 mV	40 mV
1.0V_mgt	5% 0.95 - 1.05 V	2.0 A (0 A)	27 mm	35 mV	40 mV
1.2V_mgt	5% 1.14 - 1.26 V	2.0 A (0 A)	23 mm	40 mV	48 mV
1.5V_gbt	5% ? 1.42 - 1.58 V	3.0 A ? (0.6 A)	40 mm	50 mV ?	60 mV ?
1.8V_prom	5% 1.71 - 1.89 V	1.5 A (0 A)	16 mm	65 mV	72 mV
2.5V_io	5% 2.38 – 2.62 V	3.5 A (0.2 A)	30 mm	80 mV	100 mV
1.2V_vfat	+10%/-5% 1.14 – 1.32 V	3.5 A (0.5A) ? Total for 6 VFATs	30 mm	80 mV ?	80 mV

* Worst Case Voltage Drop assumes tracks with maximum length of 650 mm.
** Maximum Safe Voltage Drop is estimated for reliable operation, assumes that the voltage supply output is tuned nearly at the upper end of the allowed range.