CSC Management goals for workshop

1. Check schedule and update as necessary to reflect technical reality
   A. Are there significant tasks or technical decisions that are not yet included in the schedule?
2. Review milestones and critical decisions
3. Review resource needs

The goals are secondary to the main goals of the workshop regarding technical solutions

These slides are mostly for reference

External constraints

- Muon TDR due Fall 2017
- LS2:
  - Funding for LS2 upgrade production expected to be available around April 2018
    - R&D and prototyping can occur before then
  - Refurbishing of MEX/1 chambers with new electronics expected around April 2019
- LS3:
  - Funding for LS3 upgrade expected around 2020
  - LS3 installation before October 2024

CSC milestone/decisions up to TDR and EDR

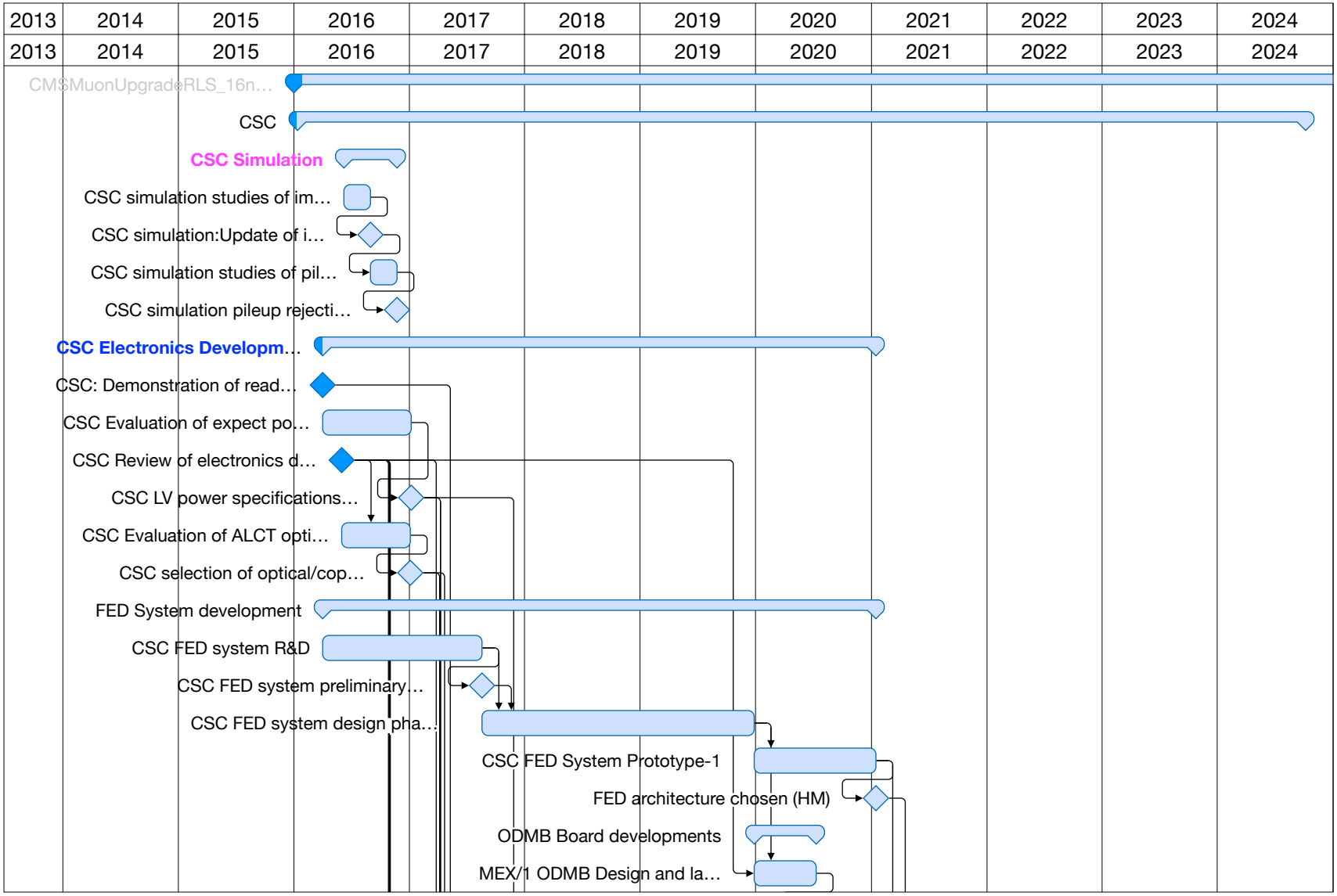
Design demo - ON-DETECTOR Electronics			
3.2.1	141	CSC: Demonstration of readout of upgraded Cathode Front End Board (DCFEB) with present Data Mother Board (DMB) (HM) • Validate the readout scheme to be used between LS2 and LS3	04/01/16 08:00
3.2.3	143	CSC Review of electronics design completed (HM) •Complete two-day internal review by the CSC community of the plans for the electronics upgrades	06/01/16 00:00
3.2.4	144	CSC LV power specifications defined (HM) •Define voltage and current needs of upgrade electronics so that LV infrastructure design can be finalized	01/05/17 17:00
3.4	**279**	**CSC On-chamber and trigger electronics EDR (EM)**	**01/05/18 00:00**
Design demo -OFF-DETECTOR Electronics			
3.2.6.2	152	ODMB optical transmitter and FPGA chosen (HM) •Technical choice made on which optical transceiver and which FPGA to use in the ODMBv2 boards	07/09/20 17:00
3.2.5.4	149	FED architecture chosen (HM) •Technical choice made on which processor boards (CTP7, etc.) to adopt as the building block of the CSC FED system	12/03/20 17:00
3.5	**280**	**CSC Readout electronics EDR (EM)**	**18/11/21 17:00**

CSC upgrade milestones

Milestone Title	expected date	Milestone description
CSC: Demonstration of readout of upgraded Cathode Front End Board (DCFEB) with present Data Mother Board (DMB) (HM)	4/1/16 8:00	Validate the readout scheme to be used between LS2 and LS3
CSC Review of electronics design completed (HM)	6/1/16 0:00	Complete two-day internal review by the CSC community of the plans for the electronics upgrades
CSC LV power specifications defined (HM)	1/5/17 17:00	Define voltage and current needs of upgrade electronics so that LV infrastructure design can be finalized
CSC FED system preliminary specs assessment (HM)	8/17/17 0:00	Define a baseline configuration for the FED system that meets the data-flow requirements for HL-LHC
ODMB optical transmitter and FPGA chosen (HM)	7/9/20 17:00	Technical choice made on which optical transceiver and which FPGA to use in the ODMBv2 boards
FED architecture chosen (HM)	12/3/20 17:00	Technical choice made on which processor boards (CTP7, etc.) to adopt as the building block of the CSC FED system
CSC LVDB prototype validation completed (HM)	2/8/18 0:00	Bench testing completed of LVDB prototype with LVMB and realistic load
CSC Front-end Prototypes validated (HM)	1/10/18 0:00	Integration test completed for prototype ALCT, DCFEB, and OTMB”
CSC On-chamber and trigger electronics EDR (EM)	5/1/18 0:00	
CSC Readout electronics EDR (EM)	2/11/21 0:00	

PRR/ESR dates

System	PRR/ESR date
DCFEB	Nov, 2017
OTMB	Jan, 2018
LVDB	Feb, 2018
ALCT	Apr, 2018
ODMB	May, 2021
FED	Feb, 2021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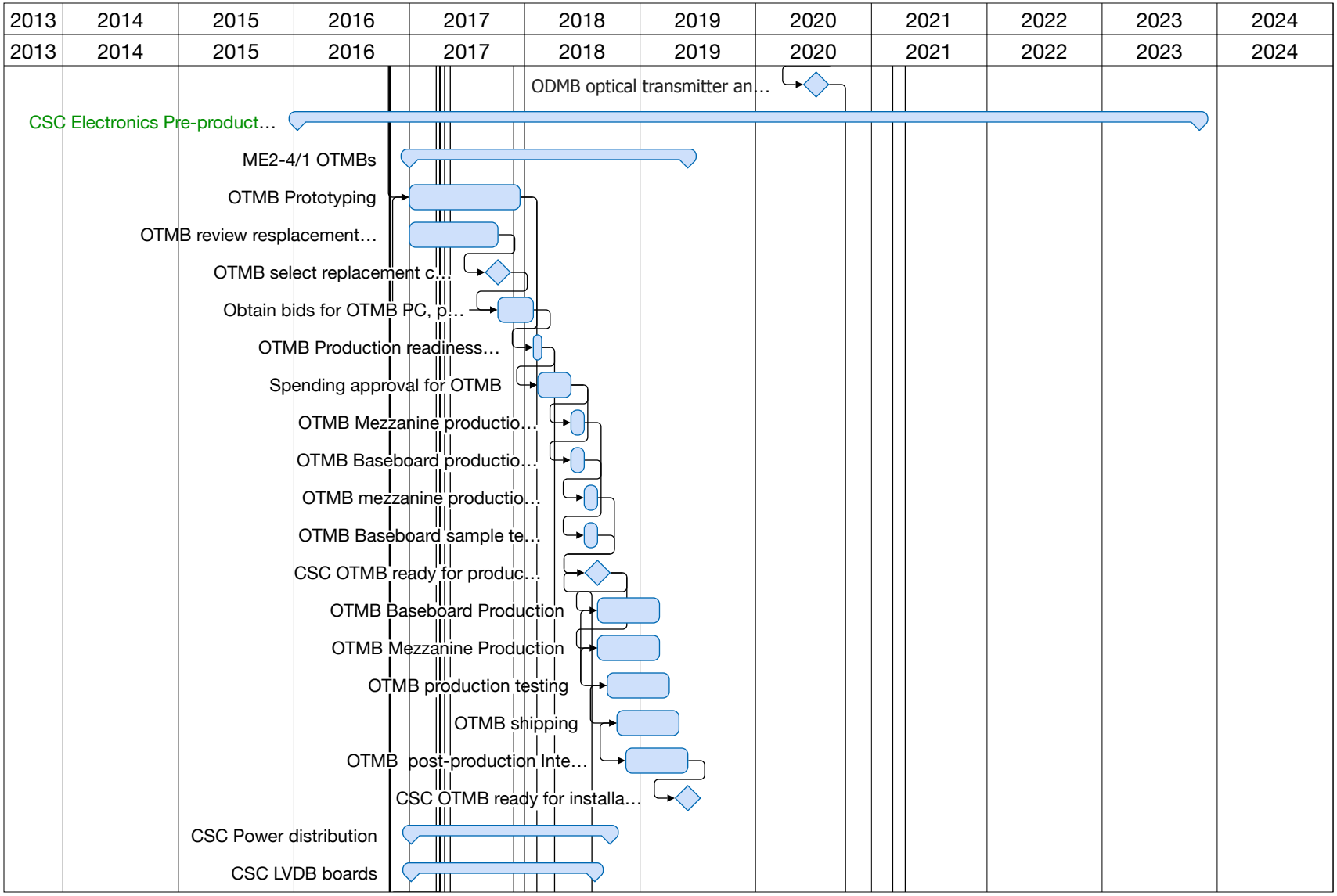
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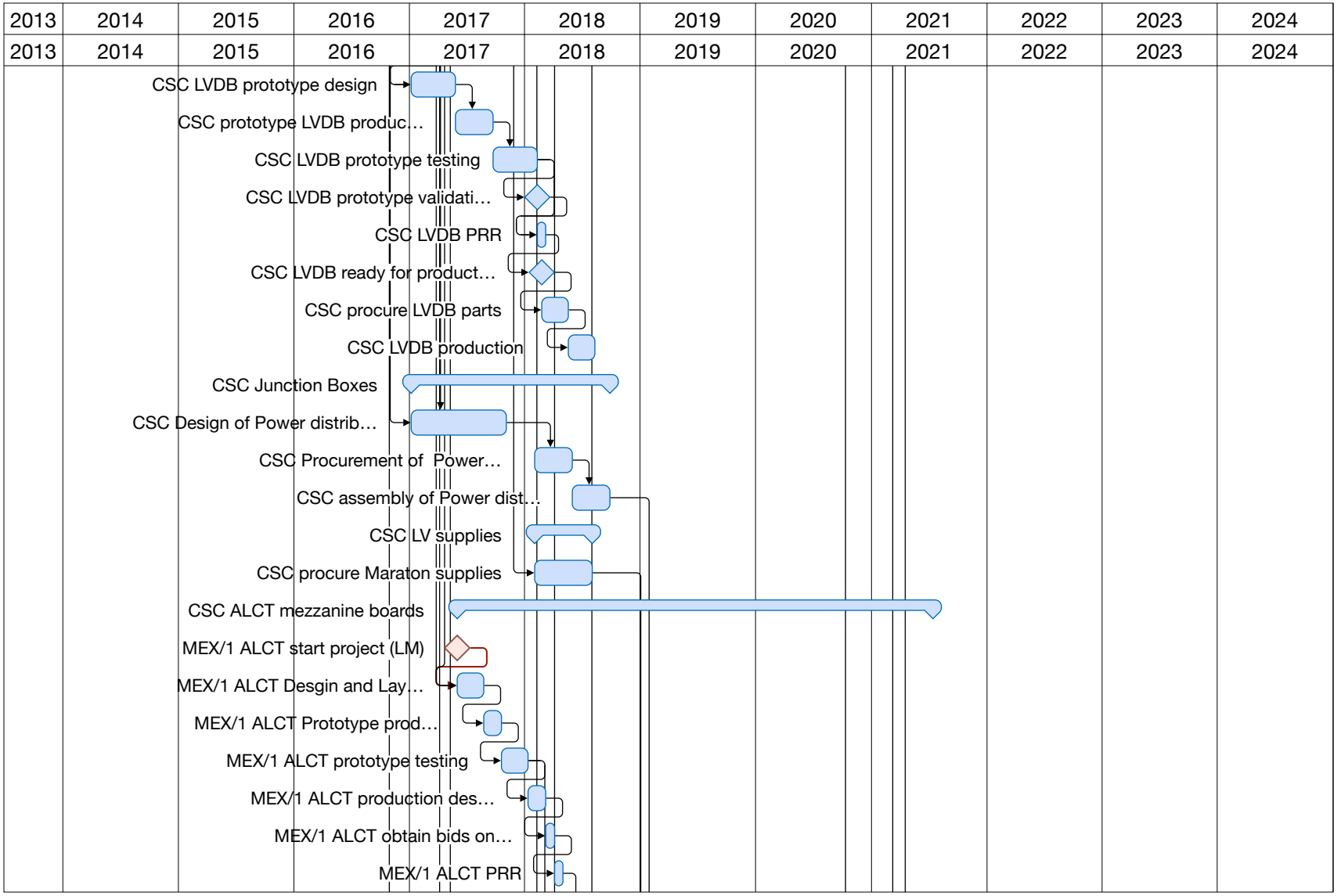
CSC Power distribution
CSC LVDB boards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CSC procure LVDB parts
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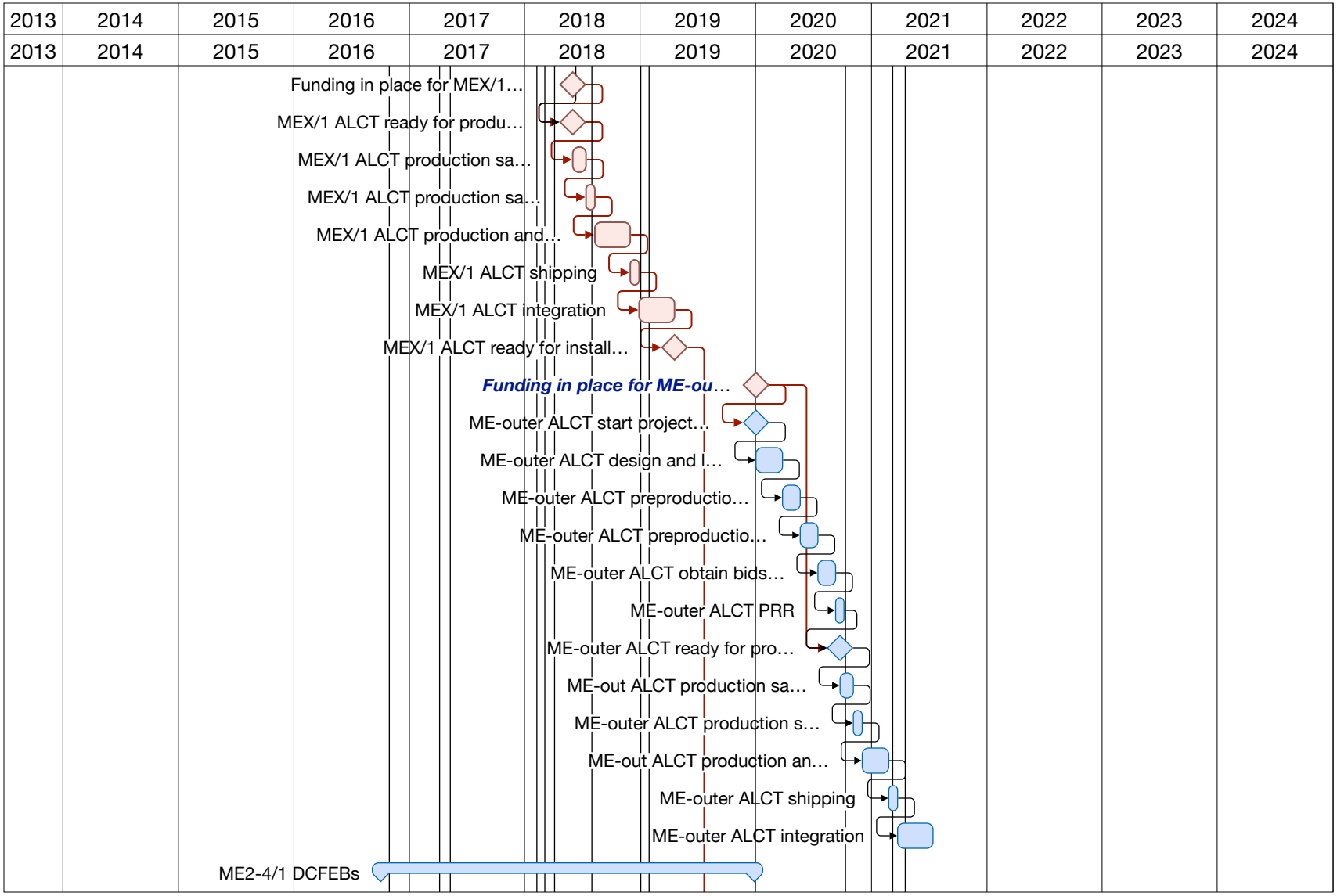
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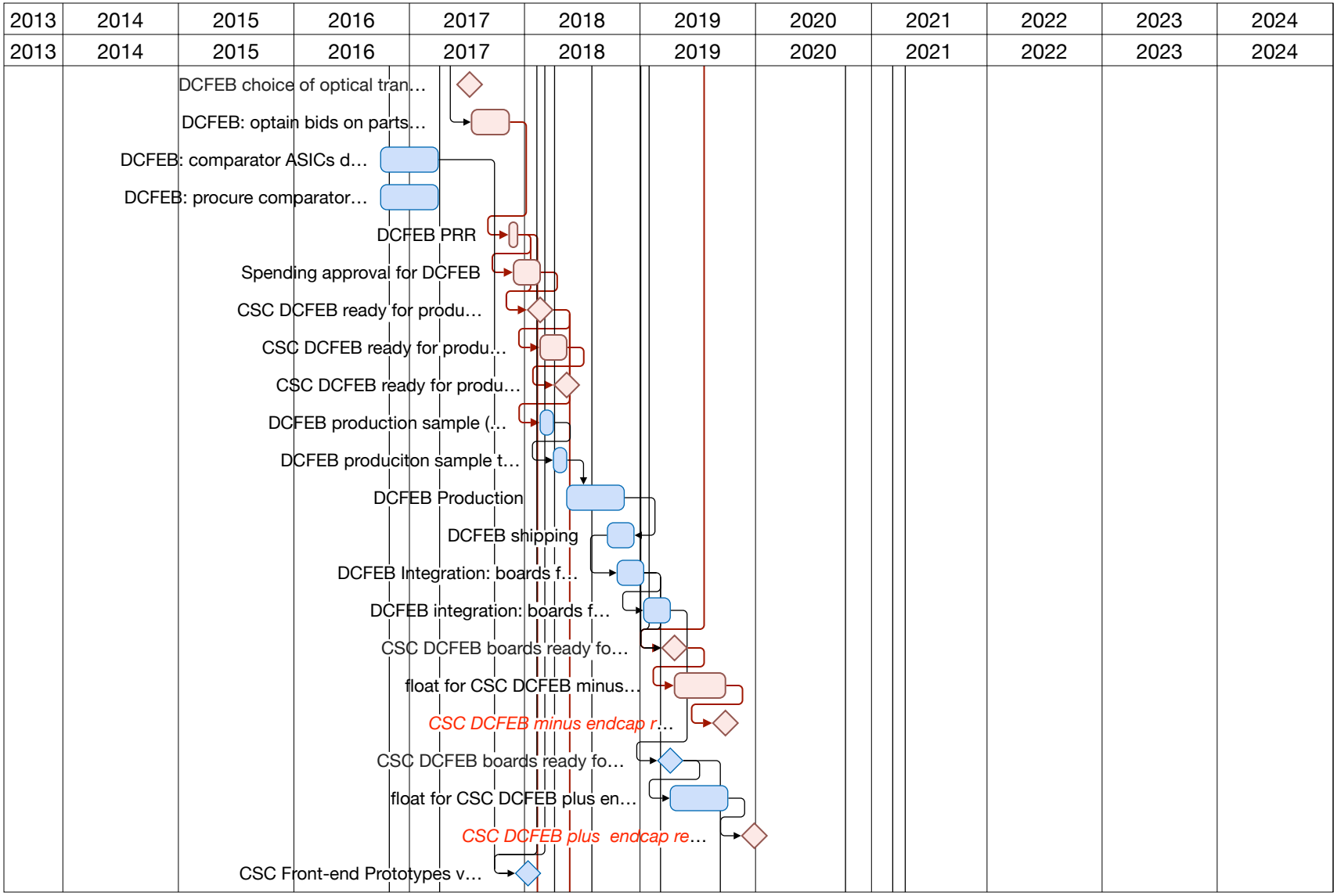
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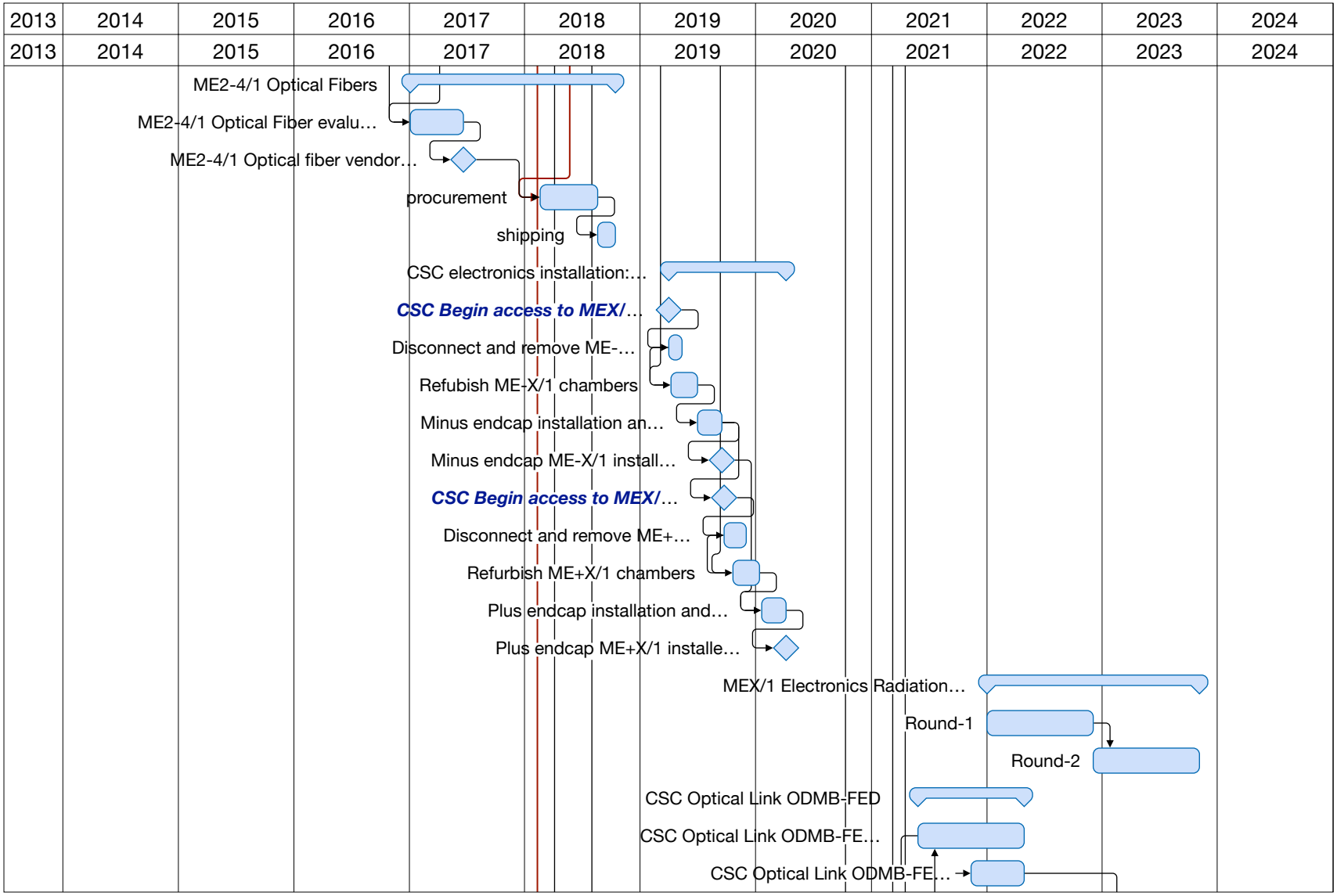
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CSC electronics installation:…
CSC Begin access to MEX/…
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Minus endcap ME-X/1 install…
CSC Begin access to MEX/…
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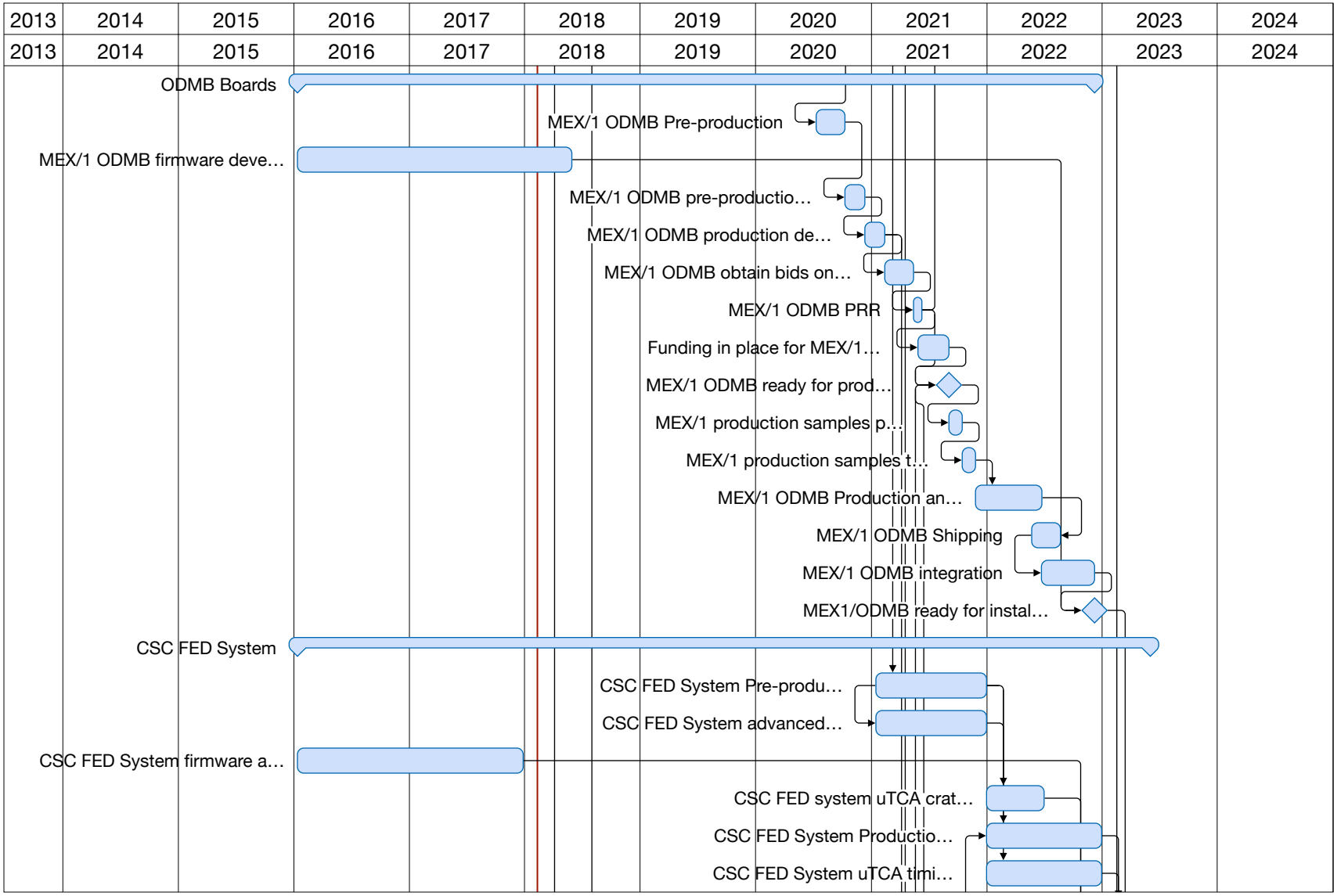
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