ALCT Mezzanine Upgrade

USCMS Muon Upgrade Meeting

December 6, 2016

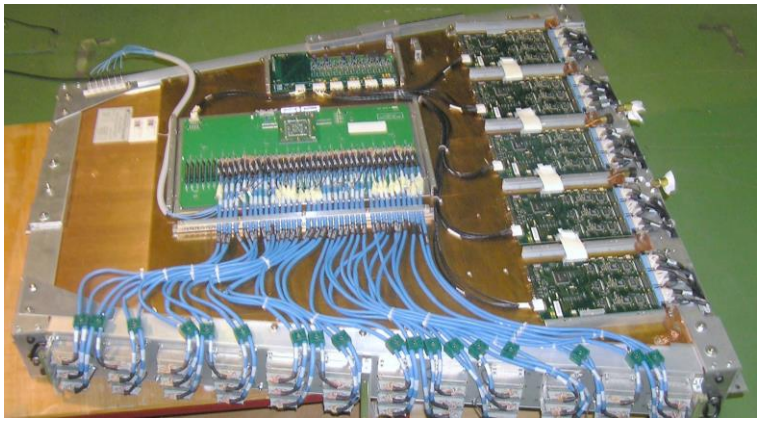
Introduction

- Current ALCT Virtex-E mezzanines facing two problems:
  - Buffer depth is too limited for increased L1 latency (on ALL chambers).
  - DAQ bandwidth is too limited for increased rates. (on INNER chambers).

- There is a uncertain *possibility* that existing copper DAQ bandwidth would be sufficient.
  - New FPGAs may allow for more sophisticated readout algorithms to better utilize existing bandwidth (zero suppression, etc).
  - But we don't know for sure. Need to develop a new mezzanine with optical DAQ option included.

Chamber	ALCT*L1A Rate (kHZ)
ME1/2	27.6
ME1/3	5.6
ME2/1	245.8
ME3/1	151.9
ME4/1	150.8
ME2/2	20.8
ME3/2	23.6
ME4/2	41.1

(thanks to Stan for slide material)



FPGA on Mezzanine board
Upgraded LS1: ME1/1 and ME4/2 equipped with Spartan 6s
All other chambers have Virtex E (limited resources)

Although data volume smaller than (D)CFEBs
ALCT*CLCT*L1A rates 5X Higher!

Optical Design

Not 100% certain that an optical link is needed if more sophisticated readout algorithms are used, but production timelines require us to proceed with designing an optical board before we know with certainty.

Baseline plan:

- Design a new board with optical transceiver option. If we can establish that an optical path is unnecessary, we can leave the components unstuffed.

Need to choose transceiver: commercial vs. vttx vs. vtrx

Baseline plan:

- Nominal choice of transmitter is CERN's VTRX (rad hard by design, transmit/receive).
  Optical RX will be unneeded on detector, but can be used for loopback testing.

Alternative plan:

- Board can be designed to be relatively compatible with VRTX and commercial SFP
  (needs minor board modifications to switch, but this has been done before by Jason)
- VTTX is also an option (a little bit cheaper).. 2nd transceiver is probably not useful

MGT Reference

Need a low-jitter reference clock source for the Multi-gigbabit transceivers (MGT)

Baseline design:

- Use an oscillator matched on the ODMB. (e.g. ODMB's 80MHz FXO-LC725-80).
  - If we use the same oscillator as the current ODMB, could use the DDU link for testing boards during production/
  - Regardless of oscillator, we can also use loopback testing.

Alternative designs:

1. Commercial clock multiplier: e.g. CDC5801A
2. Fixed oscillator + CDC5801A (MGTs can switch reference clocks --- allows for most flexibility)
3. QPLL

Regulators

There is some concern about radiation hardness of the LDOs.

ALCT mezzanine has two regulators models:

- MIC49500WR
  - Was owned by Micrel, now purchased by microchip. Don't know if they are still good.
- LP38501ATJ-ADJ
  - No reason to suspect the chip.. No reason to trust it either.

Baseline design:

- Assume they are still OK and reuse.
- If replacement LDOs are tested for DCFEB / OTMB / ODMB etc., update the design to use the same component.

FPGA + PROM Choice

Radiation issues with the EEPROMs may necessitate change of components.

- Pending an understanding of CHARM test results (there may be no problem—we don't know)

Baseline plan:

- Use LX150T + XCF32/8P (current design)

Alternative plans:

1. Artix-7 + COTs EEPROM
2. Spartan-6 + COTs EEPROM (longer, non-deterministic startup time)

Baseboard Aging

Radiation issues have already been discovered in the calibration pulsing circuit

Other problems seen at P5 with active test strips.. unknown cause
(could just be corrupted firmware… PROMs never reprogrammed)

Baseline plan:

- As components fail, perform board replacement and repair whenever possible.

Alternative plans:

1. Eventually may need baseboard replacement:
   e.g., Alex outlines an interesting plan for a new ALCT baseboard design:
   https://indico.cern.ch/event/533594/contributions/2182277/attachments/1282992/1906935/ALCT_rates_2016_06_01_c.pdf)

Schedule

- Need finished boards at CERN in Q1 2019
  - Assume ~1 year for production --- needs to start in Q1 2018.
  - Assume ~1 year for design, prototype, test --- needs to start in early 2017, finish prototype by the end of the year.

- If FPGA/PROM needs to change, have to start ASAP!
  - Spartan-6 or Artix-7 ?
  - XCF32P/XCF08P vs. cots..?

From Ben's DCFEB production schedule:
for DCFEBs to be installed in LS2 production needs to start in early 2018

Event	ME1/1 Prod. Dates	Week
Production Review	12/6/12	0
Money to OSU	1/6/13	4.5
OSU OK's Money	1/25/13	7
10 bare PCBs arrive	3/1/13	12
10 Boards Assembled	3/18/13	14.5
PCB production starts	4/1/13	16.5
Assembled boards arrive	4/30/13	21
Final Board to CERN	12/6/13	52

Backup

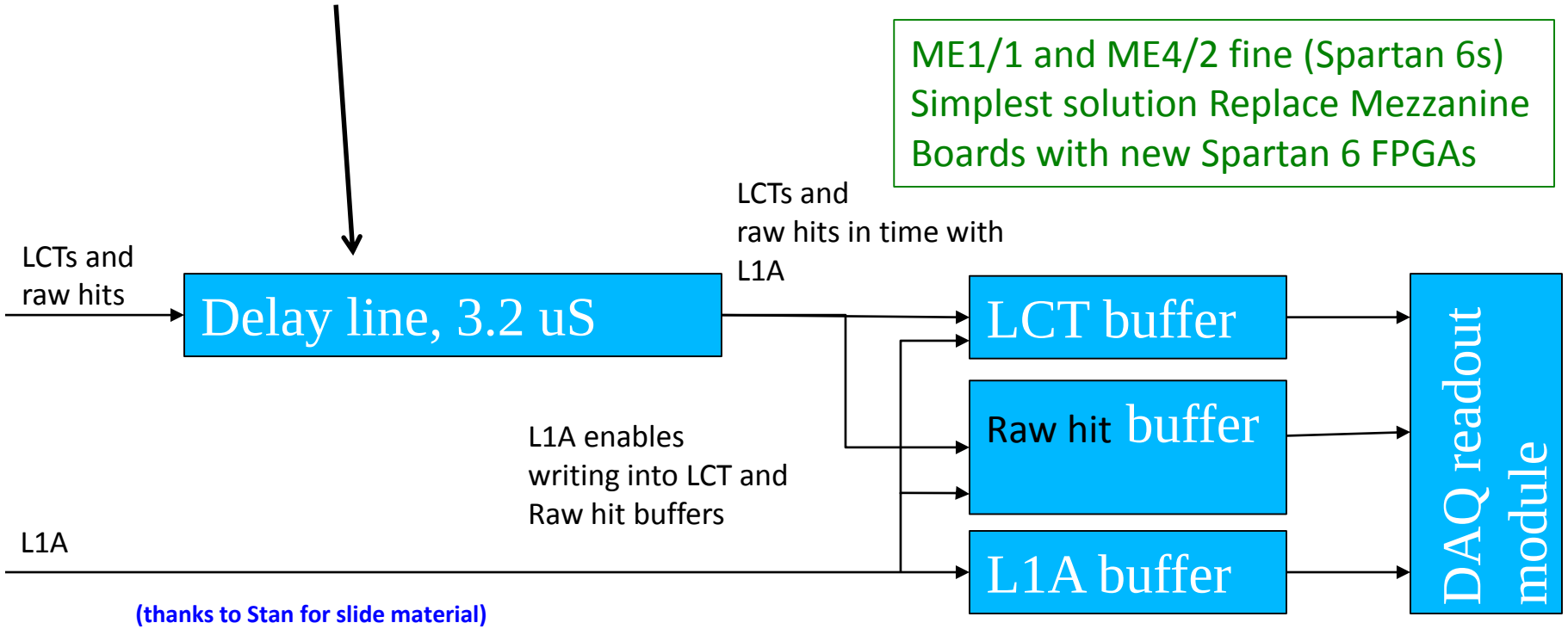
ALCT FPGA Readout Implementation

Pipeline Latency Problem

LH LHC Latency 12.5 µsec
Pipeline Length cannot be extended
(not enough BRAM in Virtex E)

	Time, uS	25-ns clocks
Currently	3.2	128
HL-LHC	12.5	500
ALCT delay line	6.4	256

ME1/1 and ME4/2 fine (Spartan 6s)
Simplest solution Replace Mezzanine Boards with new Spartan 6 FPGAs



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Chamber Accessibility

A Spartan 6 replacements with a fiber output solves Pipeline and Rate problems

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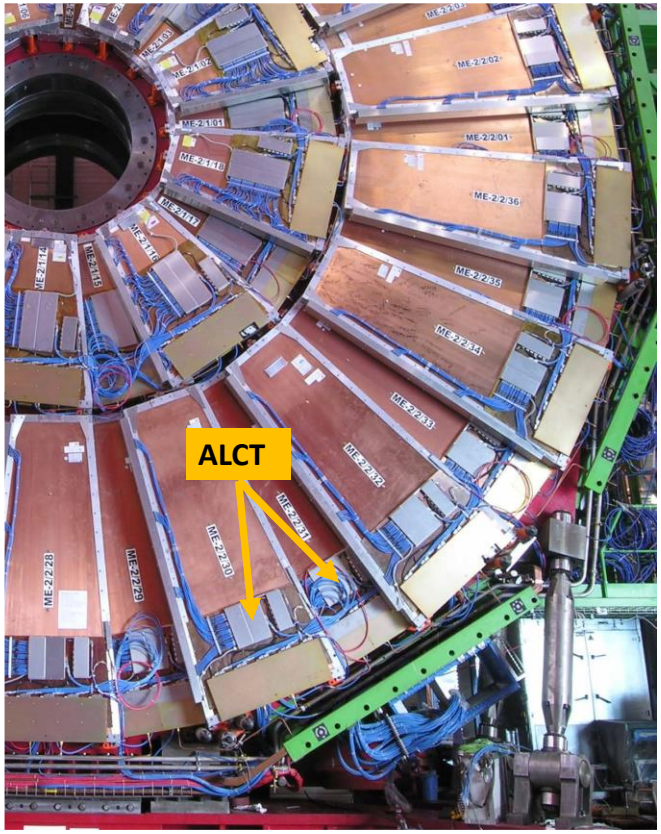

ME2/2 and ME3/2 can install Spartan 6 without removing chambers! (Armando)

EYETS 2016/17: 1st possibility to do ME1/1 (cooling circuits)

LS2: will do ME2/1, ME3/1, ME4/1 (if MEx/1 upgrade goes forward)

LS3: will do ME1/1, ME1/2, ME1/3

ME2/2 and ME3/2 done when access available