# GEM Opto-Hybrid Board Design for GE2/1 and ME0

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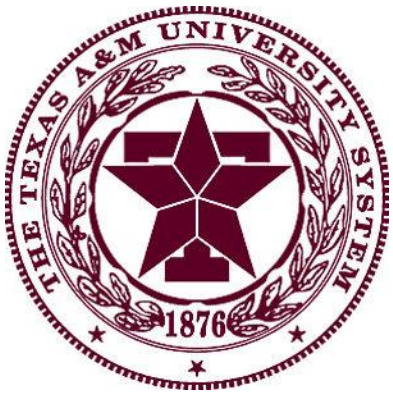
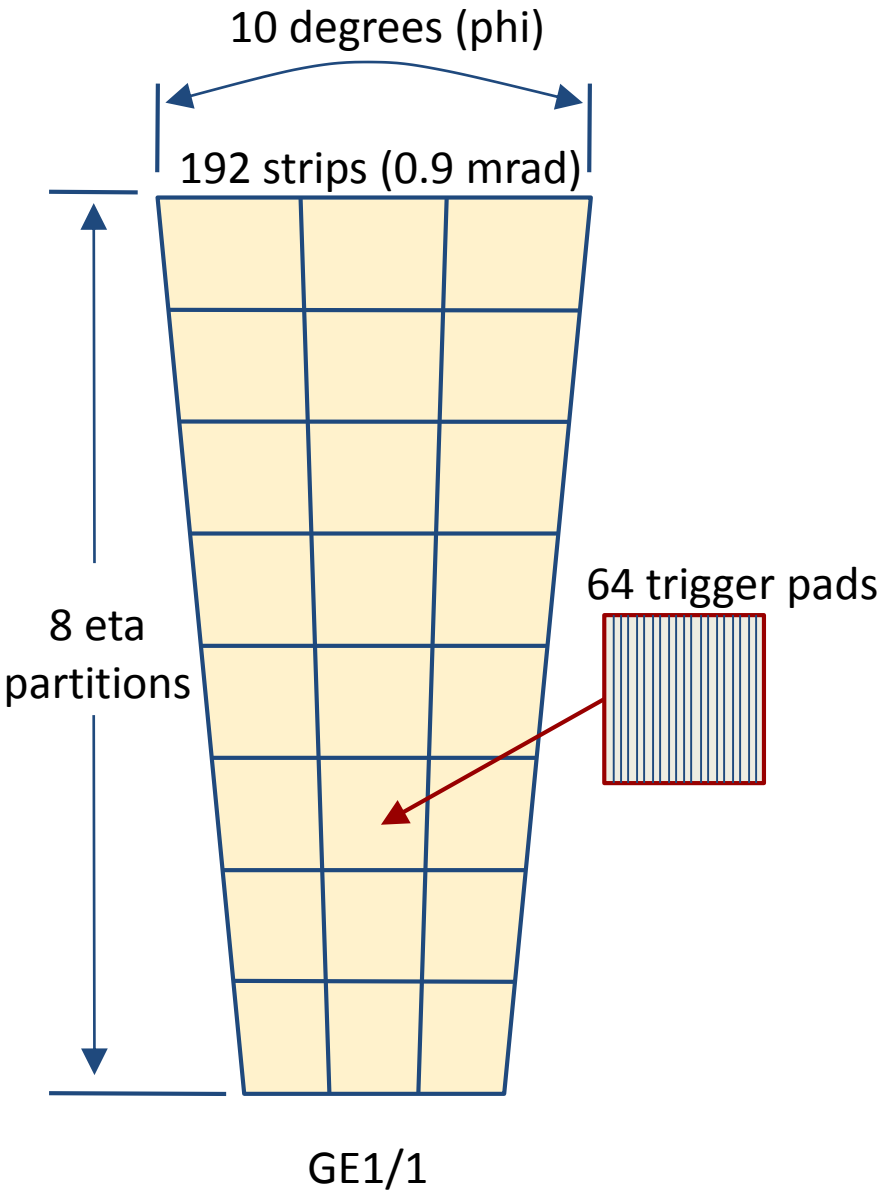
USCMS Phase-2

Forward Muon Upgrade Workshop

6 December 2016



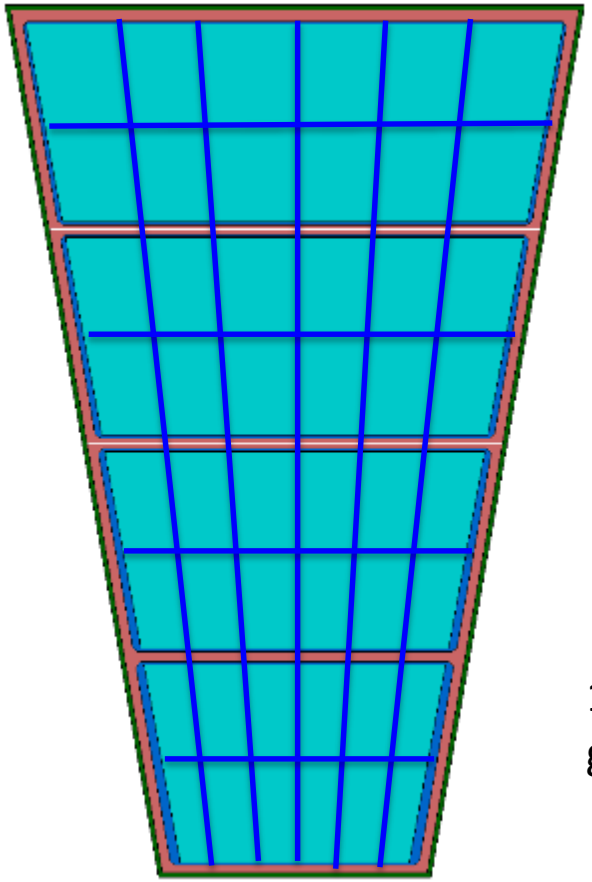
# Basic GEM Geometry & Trigger Primitives




- **All GEM detector types have the same trigger granularity (GE1/1, GE2/1, ME0)**
  - Phi granularity = 0.9 mrad
  - 8 eta partitions
  - ME0 is being decided now...
- **GEM Layers installed in CMS**
  - 10-degree GE1/1: 2 layers + CSC
  - 20-degree GE2/1: 2 layers + CSC
  - 20-degree ME0: 6 layers, no CSC
- **GEM trigger cluster finder**
  - On-chamber electronics can find up to 8 hit strip clusters in the whole chamber (1536 pads)
    - Cluster size up to 8 pads
    - Latency = 3 BX
- **Opto-Hybrid boards handle all the data and control on the chambers**

# GE2/1 GEMs: GEB and Opto-Hybrid Partitions

**Not really projective eta segmentation, Higher trigger resolution**



12 Strips groups

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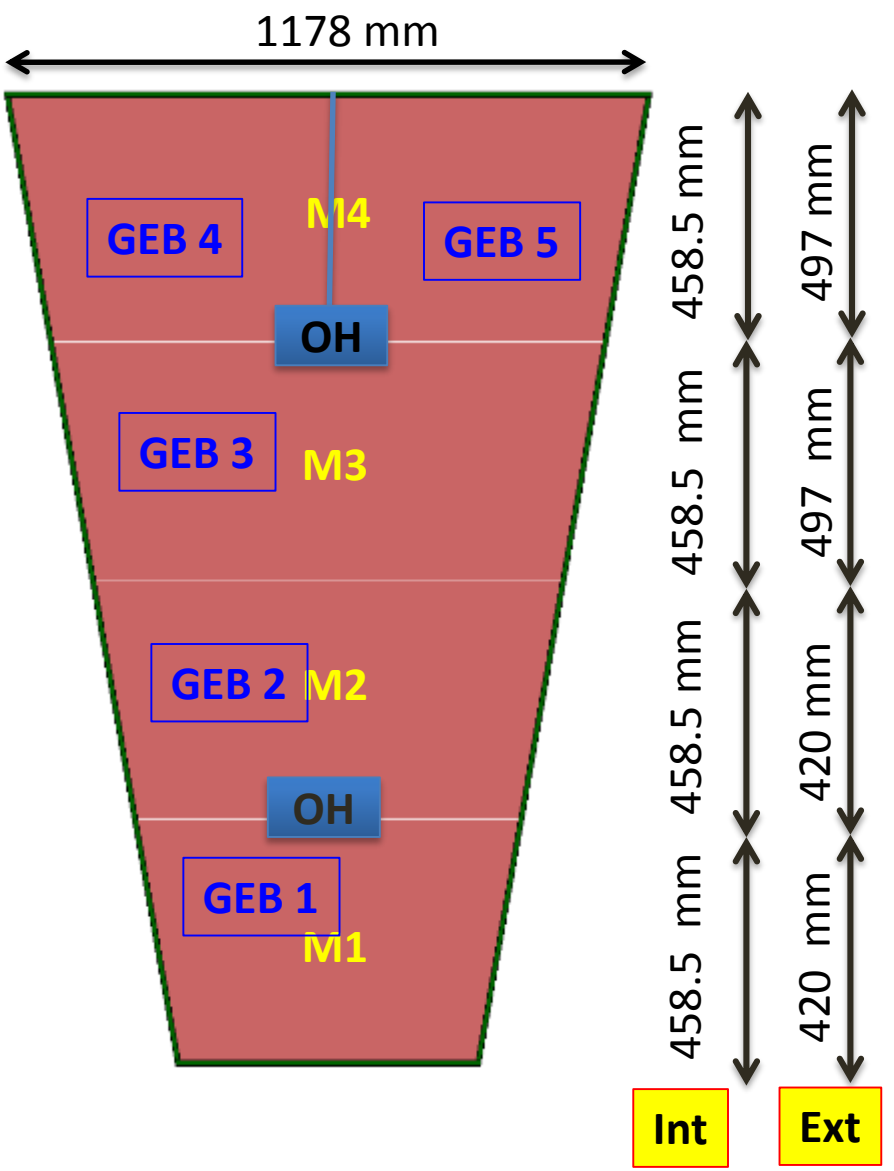
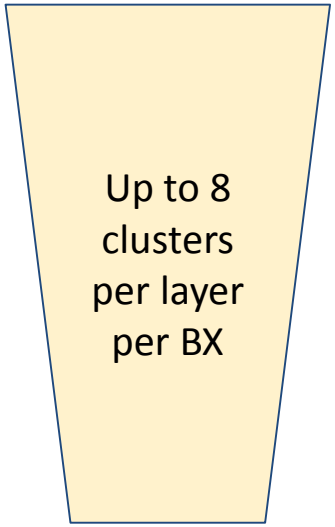



Version 14 Sept 2016

# GEM Chamber Geometry by Type

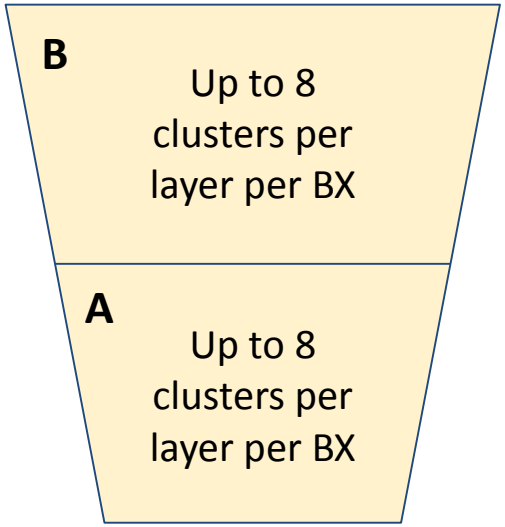
- Each GEM station has different size chambers, varies OH count
  - The GEM DAQ design is driven by the regions covered by each OH board
    - Basic building block: each Opto-Hybrid handles 24 VFAT front-end chips
  - The "24-VFAT" regions are outlined in these diagrams for each station

**GE1/1**
10 degree chamber
2 layers



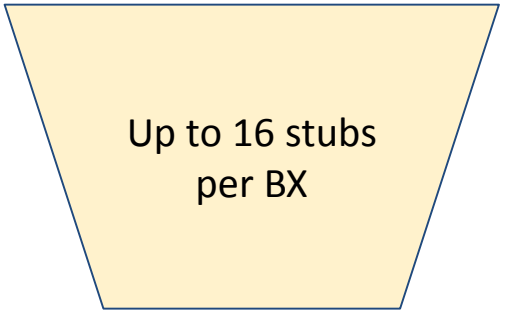

Phi granularity 0.9mrad
8 eta partitions

**GE2/1**
20 degree chamber
2 layers




Phi granularity 0.9mrad
8 eta partitions

**ME0**
20 degree chamber
6 layers




Phi granularity TBD:
0.9mrad or 1.8mrad

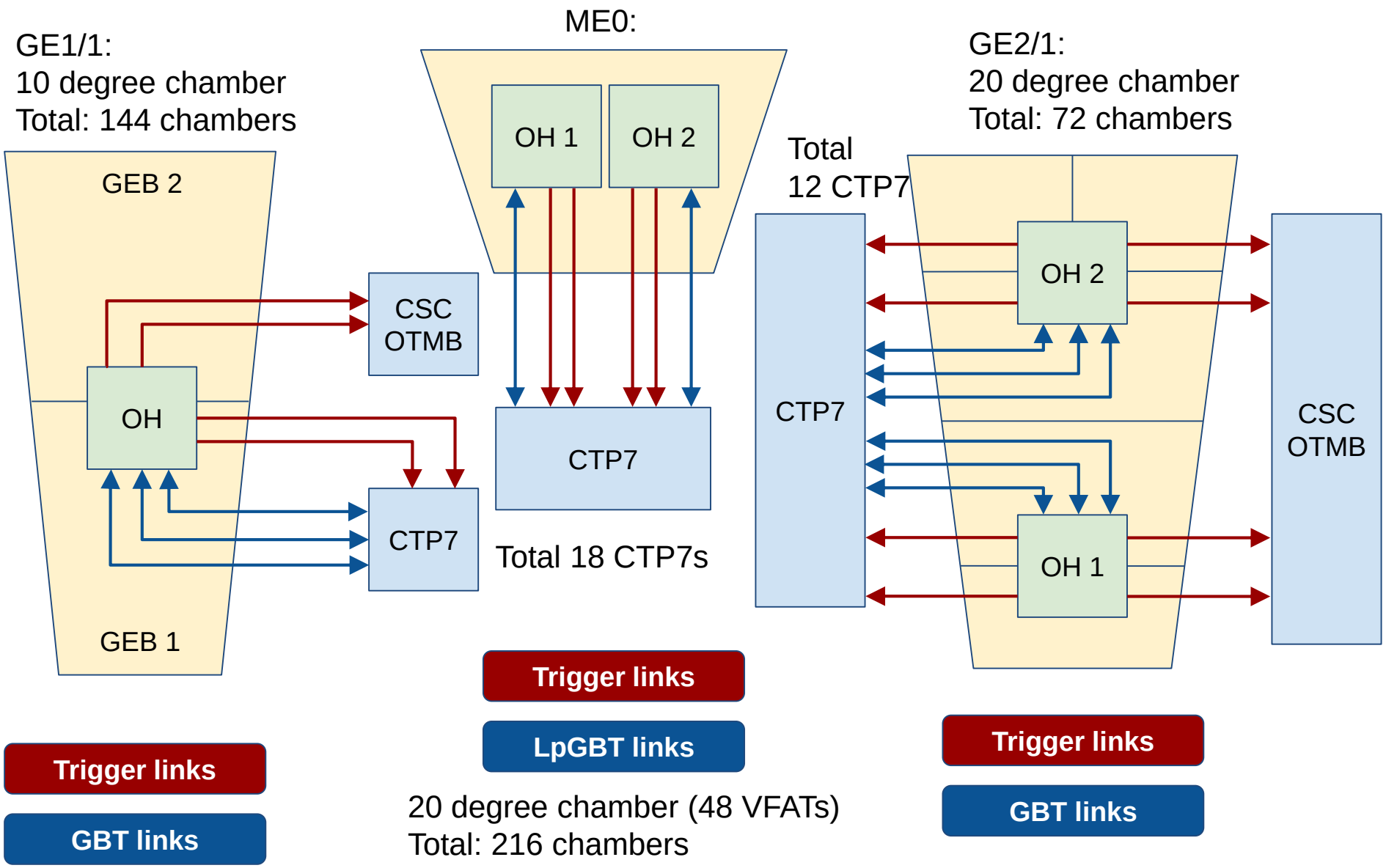
8 or 4 eta partitions
-do stub finding in CTP7-

# Opto-Hybrids are not all the same

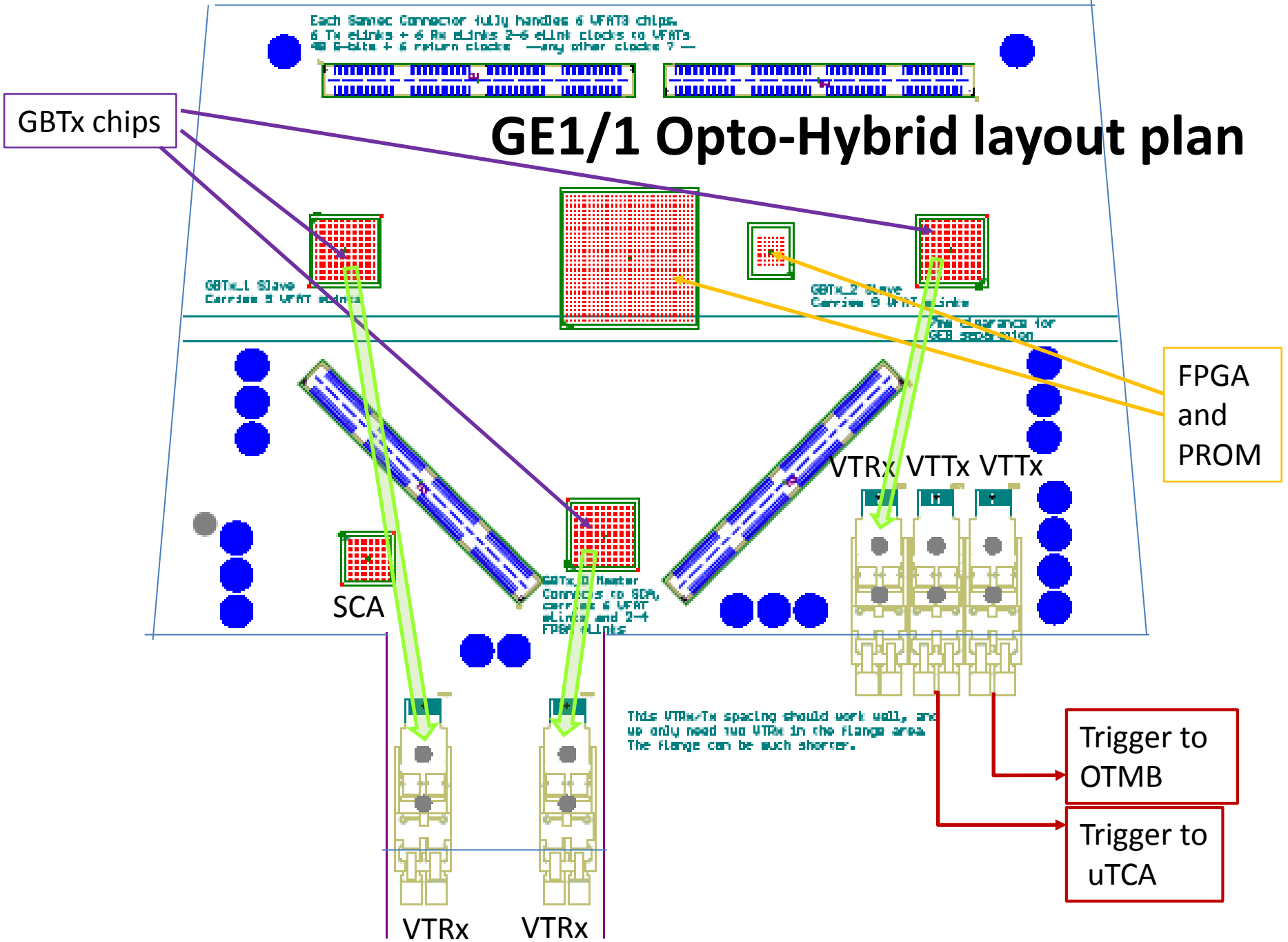
- GE1/1 OH boards have 3 GBTx chips and 3 VTRx
  - These are dedicated for VFAT3 data & control interface
    - One GBTx can handle data and control for maximum 10 VFAT3 chips
  - With just 2 GEM layers, the link count is manageable
- GE2/1 OH is nearly the same as GE1/1
  - Only mechanical changes to match GEM chamber and GEB changes
- Both of these OH types have a pair of VTTx devices
  - These carry trigger cluster data to OTMB and GEM uTCA

- In 6-layer ME0 the link count becomes unmanageable
  - However, if we use LpGBT instead of slower GBTx it helps…
- Each LpGBT can handle data from 24 VFAT3 chips
  - The control however is another issue, but probably workable
  - It seems possible to have just one LpGBT and on VTRx per OH!

# Opto-Hybrid Fiber Link Connection Requirements



# GE1/1 Opto-Hybrid layout plan



# The Technical Complexities -- I

- GBTx uses an embedded Versalink protocol for the fiber link transfers
  - 4.8 gbps → 3.2 gbps data + 1.6 gbps control
  - Data and control fields in the stream are precisely defined
- GBTx i/o at the OH side include 10 e-link pairs (transmit and receive) that run at 320 mpbs (on GE1/1 and GE2/1)
  - There is also a clock output for each e-link
    - So one e-link is really 3 differential pairs
- Each VFAT3 ASIC requires an e-link pair for control and tracking data transmission
  - Thus, each GBTx can handle up to 10 VFAT3 chips

- The hard part: the 320 mbps e-link signals run from VFAT3, across the GEB (~40 cm) through the Samtec high-speed connectors onto the OH board, and finally to the GBTx
  - Impedance balance and signal quality area a big concern

# The Technical Complexities -- II

- ME0 will use LpGBT, rated at 10 gbps
- LpGBTx i/o at the OH side include 24 e-link inputs at 320 mbps, but only 16 outputs running at 80 mbps

- The hard part: how do we get 24 VFAT3 chips to share 16 LpGBT outputs?
  - This is critical for VFAT3 control (L1 trigger, resets and registers) as well as monitoring
  - Can we put two VFAT3 on each LpGBT output e-link and address them independently?

- Also note that for all OH boards we are concerned about the rad-hard PROM issue

# The Technical Complexities -- III

- The trigger pad bits (called s-bits) come from each VFAT3 at 320 mbps and go to the FPGA
  - It is 8 differential data pairs plus one clock from each VFAT3
    - That is 432 i/o pins at the FPGA already, plus we have the dedicated PROM BPI pins, clock inputs and other control signals for FPGA
  - For sure we can fit this in a Virtex-6, but trying to conserve i/o to use an Artix-7
    - Maybe we could use some GBTx e-link outputs (slowed down to 40 MHz) to directly drive FPGA data/program pins
      - In this way we would not even need any PROM!
- Inside the FPGA, each signal must be deserialized to an 8-bit number every BX
  - The s-bit signal length from VFAT3 to FPGA are all different: there will be phase differences to compensate
    - Somehow we need to sync all 8*24 VFAT3 s-bits signals to the LHC clock inside the FPGA

# The Technical Complexities -- IV

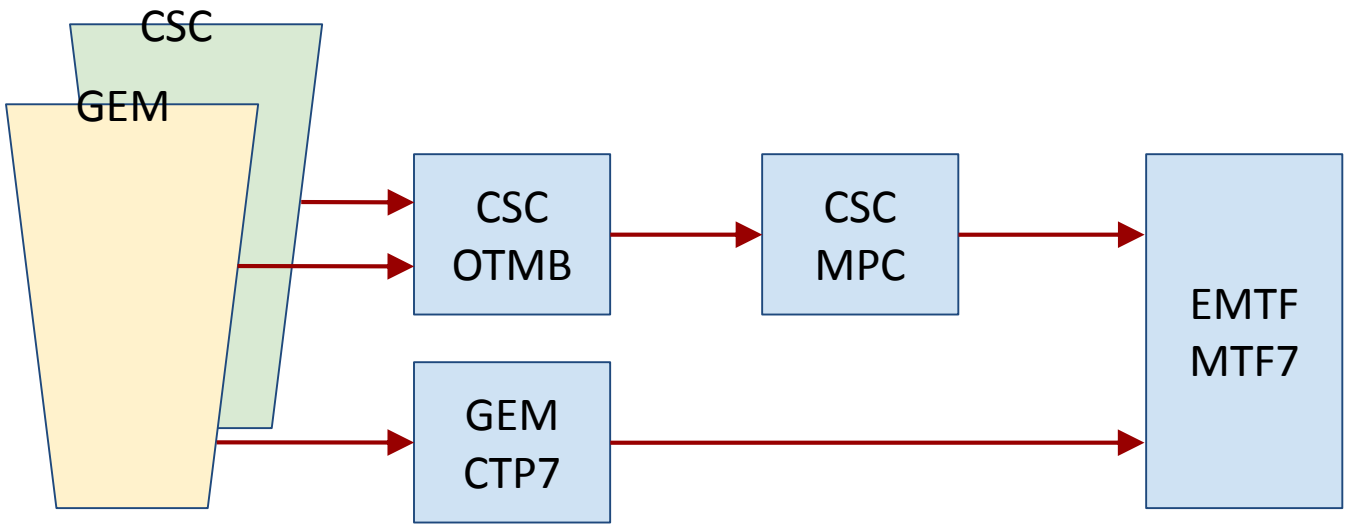
- ME0 has no good space for typical GEB+OH connections to the GEM
  - Only has 17 mm clearance in the narrow chimney area
  - Elsewhere it is ~0 mm (maybe ~@mm for GEB/RO board combination PCB)
  - We need to get 320 mbps signals to the OH without severe signal degradation the can occur with very narrow PCB tracks that are ~90 cm long
    - Maybe a long, narrow OH board stacked above the VFAT chips in the chimney area?

# The End

- Bonus slides follow….

# Overview of CSC + GEM Combination

- OTMB will receive GEM hits from GE1/1 and GE2/1
  - Combined time coincidence and pattern finding
    - Including GEM will improve OTMB bending resolution
  - GEM is seen as 2 extra layers in the OTMB
    - Basically, OTMB generates 8-layer trigger primitives



# GEM V3 LV Supply Guidelines

| Voltage Supply Name | Max Voltage Tolerance & Range | Max (Min) Current Required, worst case | Suggested Minimum Track Width on GEB | Predicted Worst Case Voltage Drop Across GEB* | Maximum Safe Voltage Drop** |
|---|---|---|---|---|---|
| 1.0V_int | 5%<br>0.95 - 1.05 V | 4.0 A (0.5 A) | 63 mm | 40 mV | 40 mV |
| 1.0V_mgt | 5%<br>0.95 - 1.05 V | 2.0 A (0 A) | 27 mm | 35 mV | 40 mV |
| 1.2V_mgt | 5%<br>1.14 - 1.26 V | 2.0 A (0 A) | 23 mm | 40 mV | 48 mV |
| 1.5V_gbt | 5% ?<br>1.42 - 1.58 V | 3.0 A ? (0.6 A) | 40 mm | 50 mV ? | 60 mV ? |
| 1.8V_prom | 5%<br>1.71 - 1.89 V | 1.5 A (0 A) | 16 mm | 65 mV | 72 mV |
| 2.5V_io | 5%<br>2.38 – 2.62 V | 3.5 A (0.2 A) | 30 mm | 80 mV | 100 mV |
| 1.2V_vfat | +10%/-5%<br>1.14 – 1.32 V | 3.5 A (0.5A) ?<br>Total for 6 VFATs | 30 mm | 80 mV ? | 80 mV |

* Worst Case Voltage Drop assumes tracks with maximum length of 650 mm.
** Maximum Safe Voltage Drop is estimated for reliable operation, assumes that the voltage supply output is tuned nearly at the upper end of the allowed range.