# Overview of the GE2/1 and ME0 Electronics

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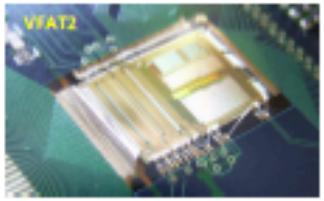
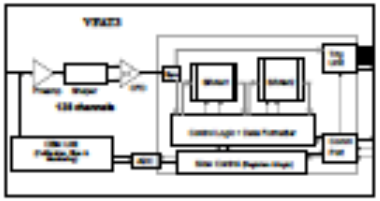
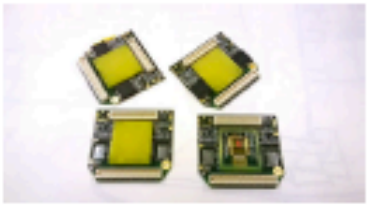
# GE1/1 Electronics System

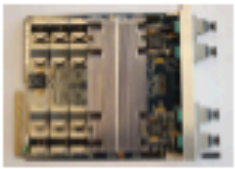


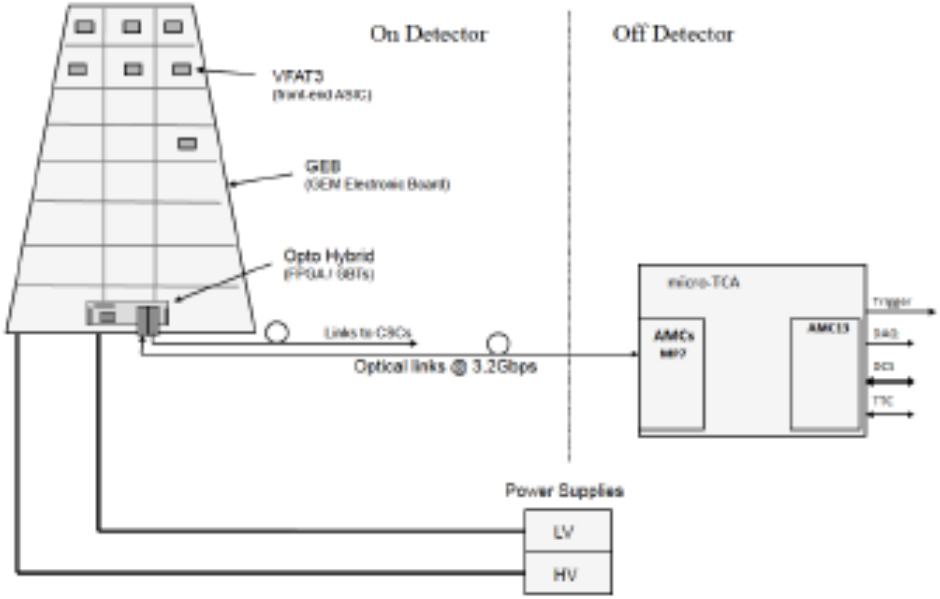



VFAT3 front-end ASIC development

Xxx7 (MP7/FC7/CTP7)

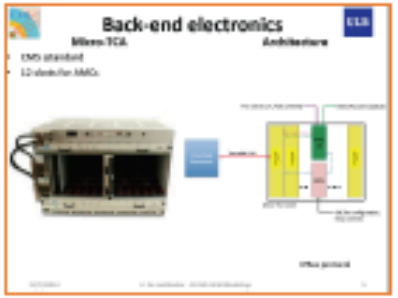


GEM Electronic Board (GEB)

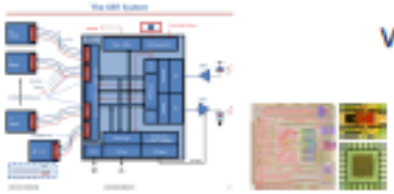



Opto-Hybrid (OH)


µTCA
AMC13, MCH




GBT



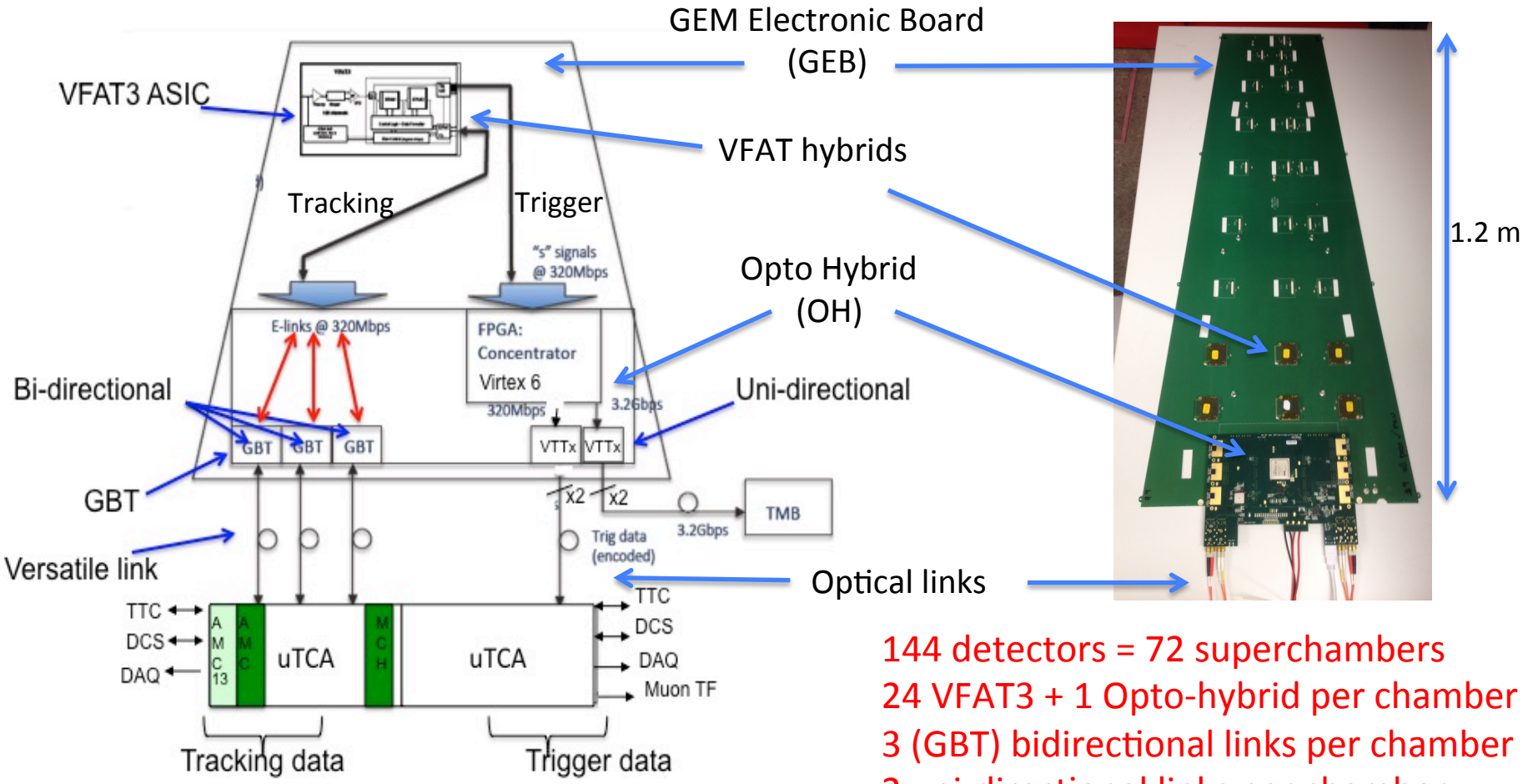
Versatile Link

Installation in CMS in 2019-20

Use of many common developments such as GBT, Versatile Link, µTCA backend

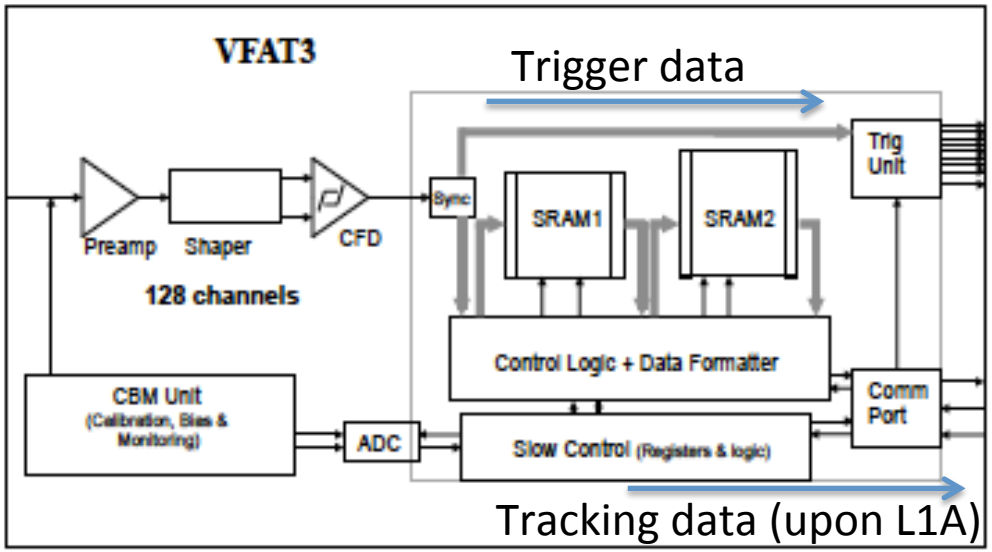
LS2 : GE1/1 Installation
LS3: GE2/1 and ME0

# GE1/1 Electronics



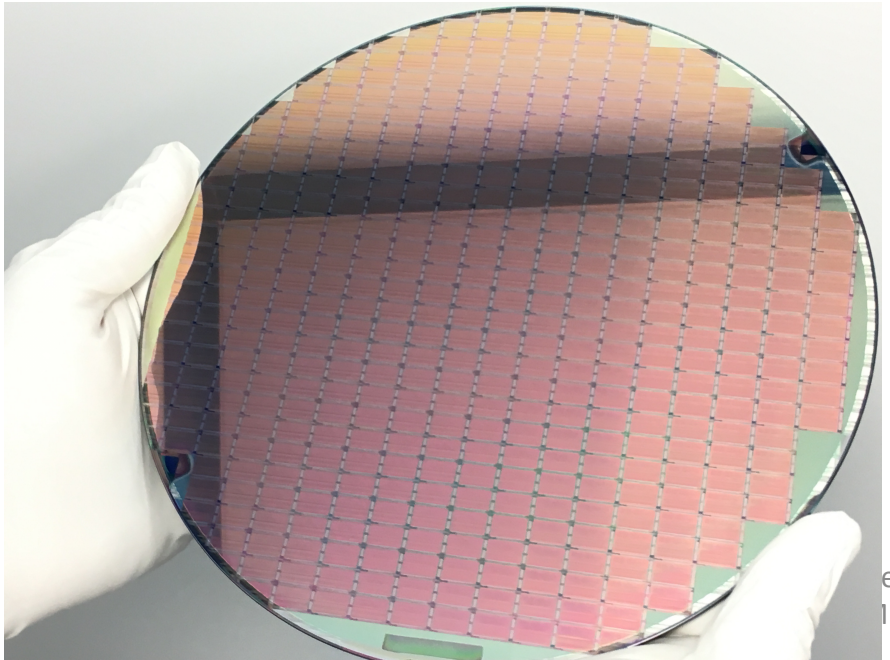

144 detectors = 72 superchambers
24 VFAT3 + 1 Opto-hybrid per chamber
3 (GBT) bidirectional links per chamber
2 uni-directional links per chamber
6 CTP7, 1 microTCA crate

# VFAT3



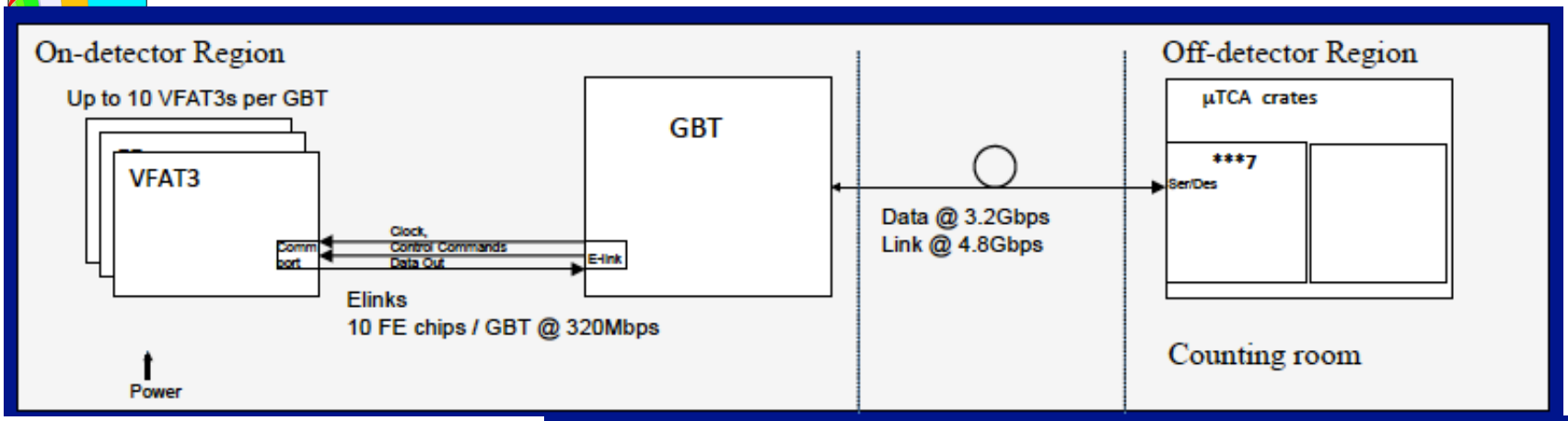

**VFAT3 characteristics**

- 128 analog channels binary chip
- 25ns – 100ns programmable shaping
- Trigger data granularity (2 strips)
- SRAM1 256 cell deep
  - L1 latency up to 25 us
- SRAM2 512 deep
  - To store up to 512 BX
- Tracking data
  - 1-8 BX per trigger
- L1A rate up to 1MHz
- Interfaces to suit GBTx
  - 320 MHz slvs

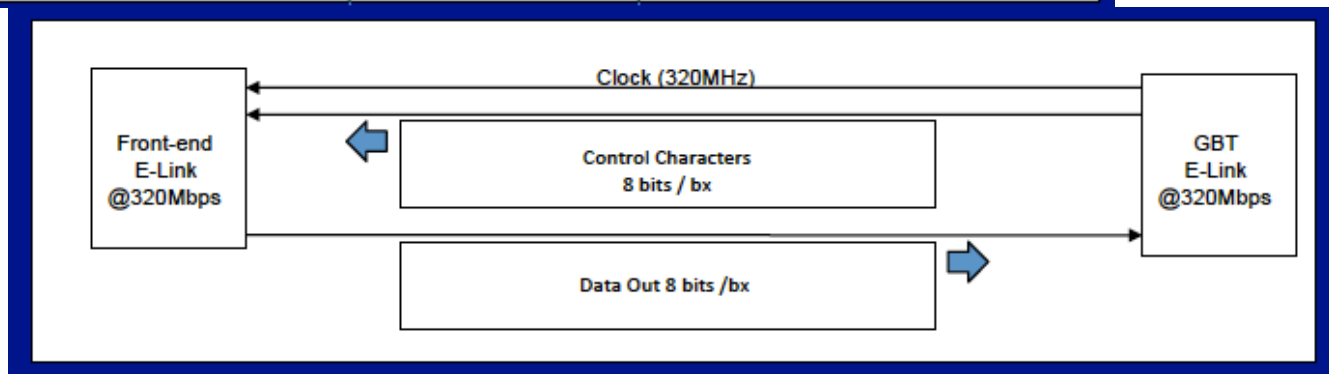


*Delivered to CERN mid-Nov.*
*TSMC 130 nm*

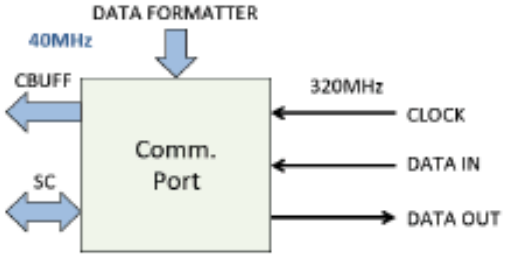
# VFAT3 – GBT communication




- Designed to be compatible with the GBT chipset
- Generates and synchronizes internal 40MHz clock, which is used by other digital blocks
- Receives encoded commands from the outside, and executes them
- Transmits data from the Data Formatter and the Slow Control to the outside
- Can operate in two different modes:
  - SC Only (Data from DF are not transmitted)
  - Run mode (DF has priority)



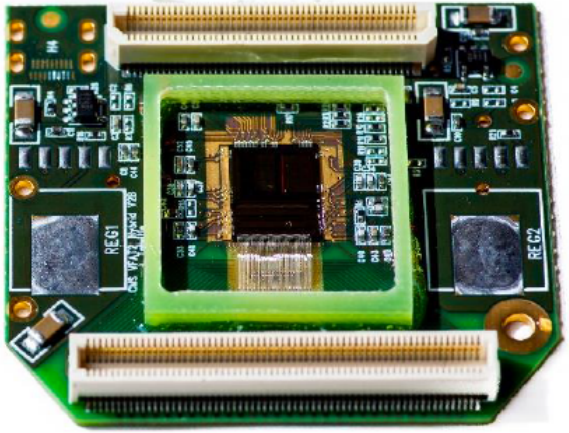

Communication Port




1 GBT chipset can handle 10 VFAT3s

# VFTAT Hybrid versus packaging

- Hybrid



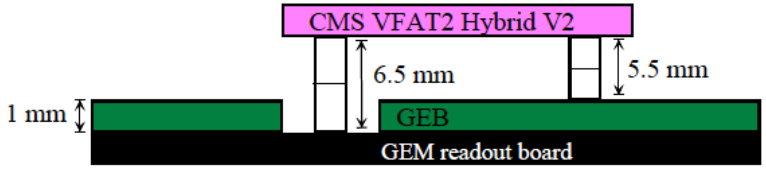
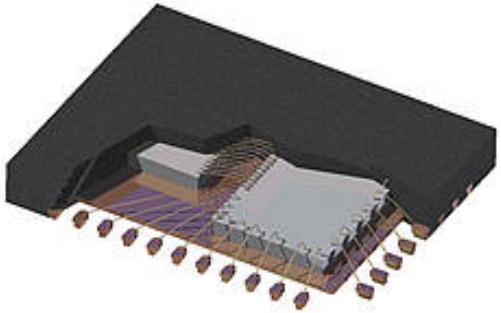
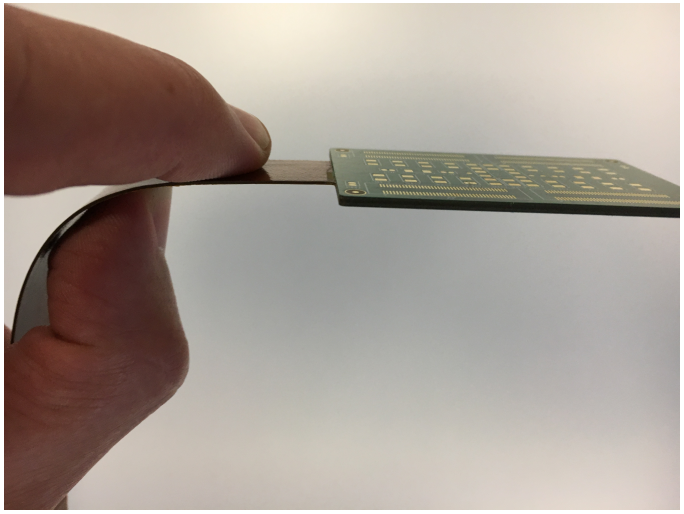



Figure 10. Cross section of the GEM, GEB and hybrid assembly.

- Packaging + Flex PCB





(more in my talk of tomorrow)

# VFAT3 constraints

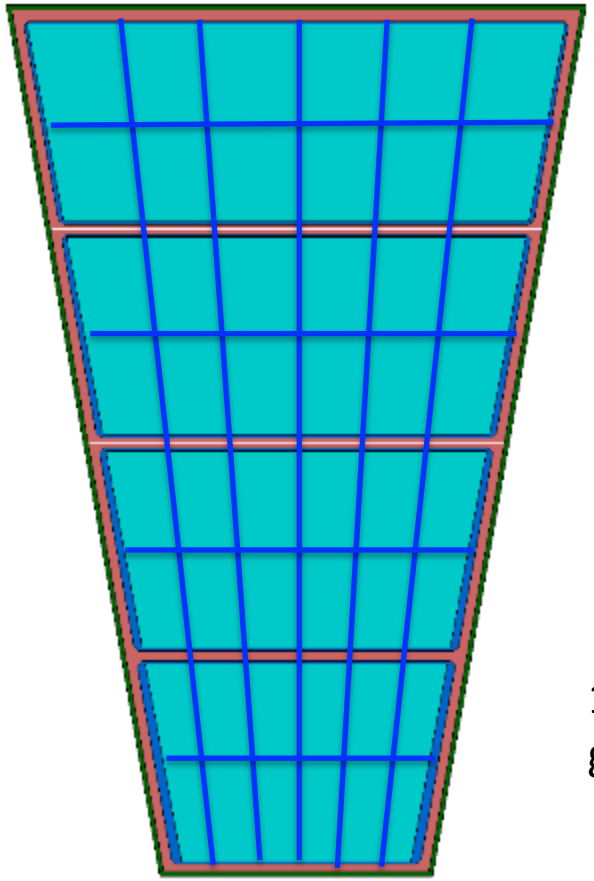
- Trigger data:
  - 8 differential pairs at 320 MHz (slvs)
    -> 2.5Gbps of data
    -> Need processing (zero suppression) on detector
    -> FPGA
- Clock:
  - 1 clock line (diff.)
- RESET:
  - 1 Hard Reset line (single ended)
- TOTAL of lines to FPGA : 456

- Tracking data (eLink):
  - 3 differential pairs at 320 MHz (slvs)
  - Directly connected to GBT
- 1 GBTx can handle up to 10 VFAT3s

# GEB and OH constraints

- GEB
  - 1m - 1.2m multilayer PCB are difficult to produce
  - Running signals at 320MHz over a 1m-long PCB is challenging
- OH
  - Need FPGA with large number of I/Os: 500-600
    - 456 pins needed to control and read-out sbits from 24 VFAT3
    - Currently Virtex-6 is the best candidate

# GE2/1



12 Strips groups

12 Strips groups

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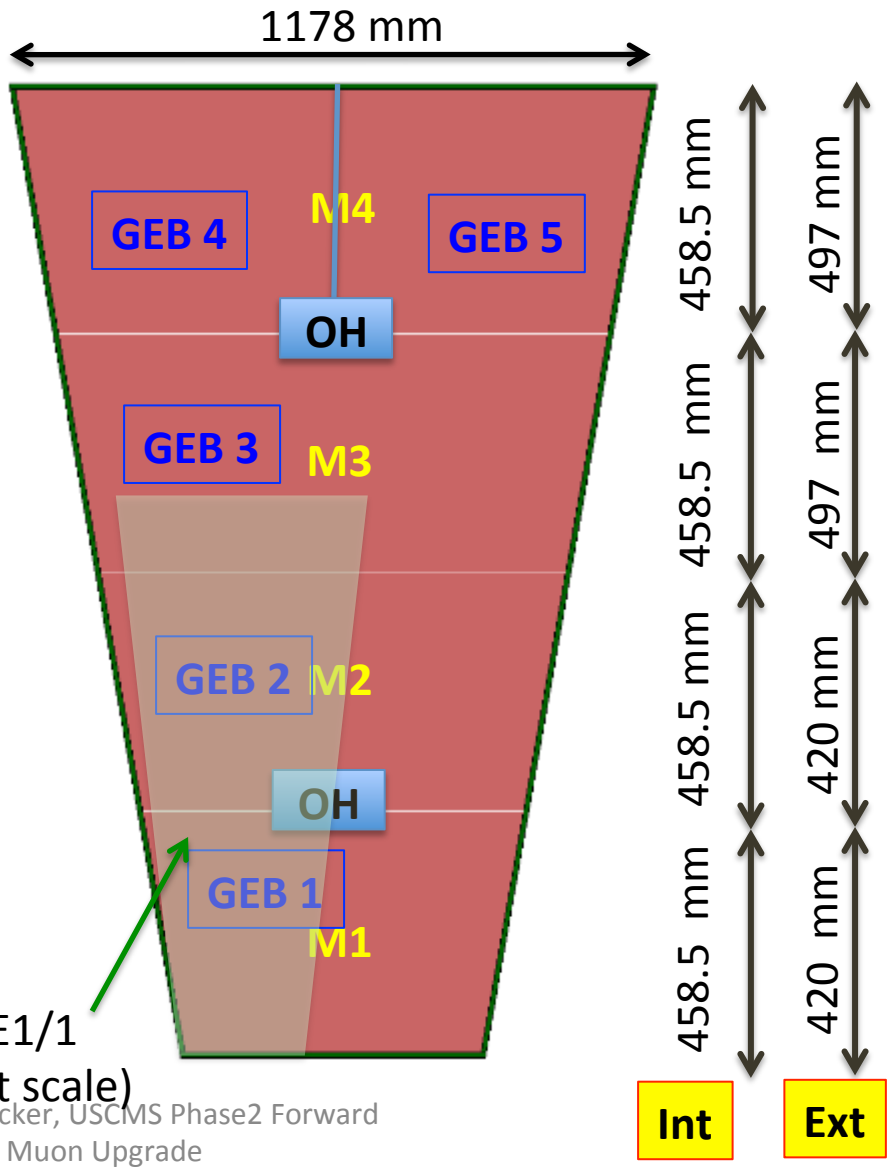
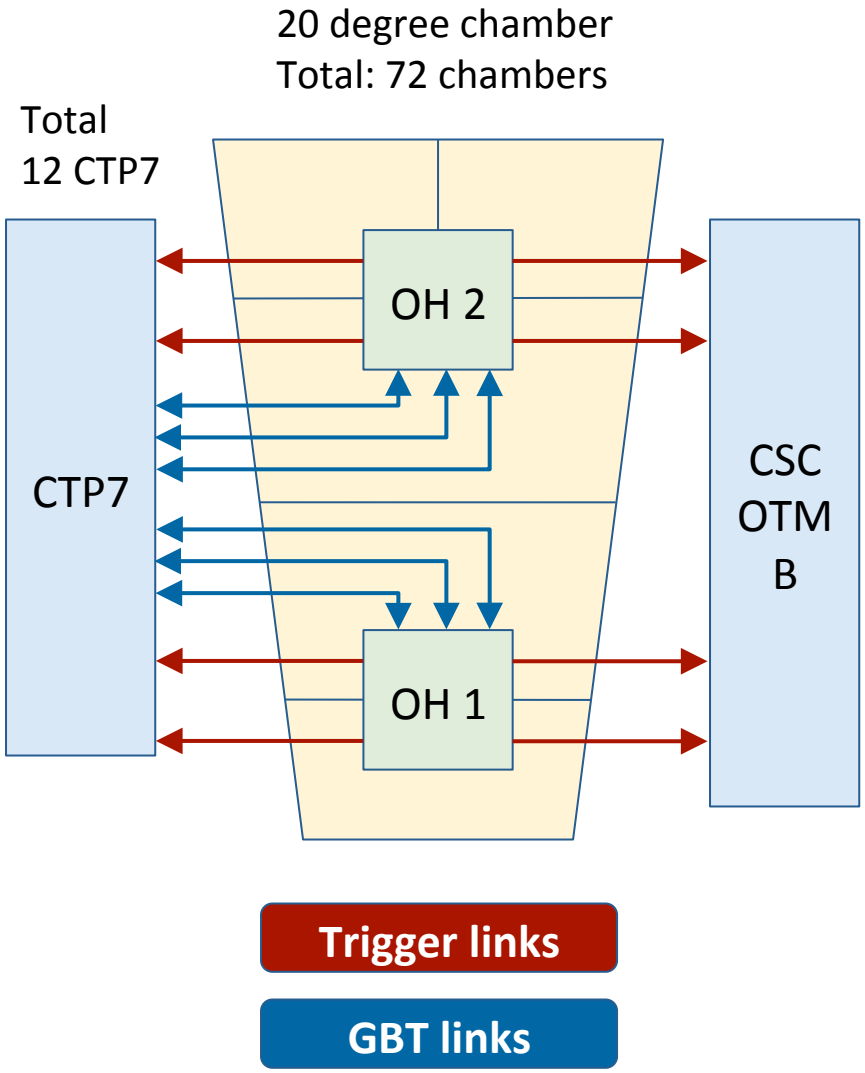
12 Strips groups



# GE2/1 electronics system




- **48 VFATs per chamber**
- **Total 12 CTP7s**

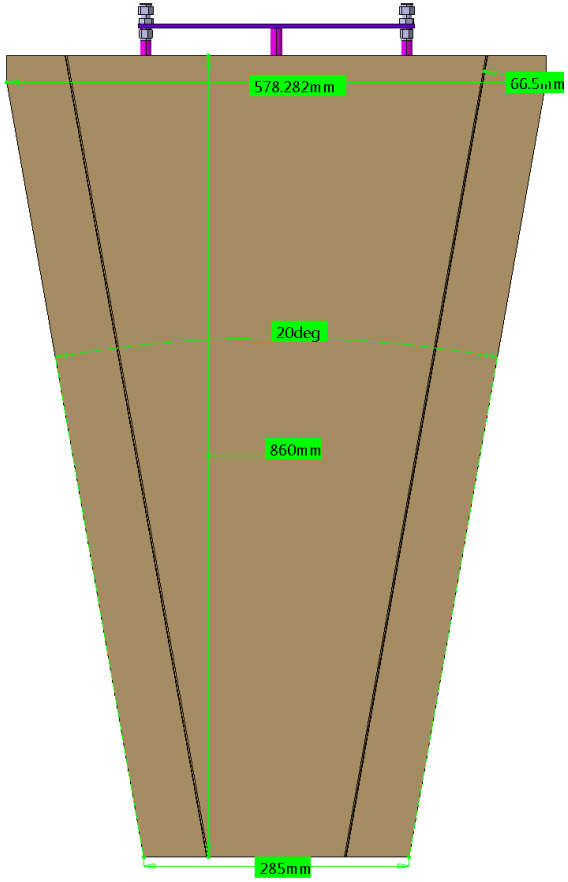
- **Total link count per chamber**
  - 6 bi-directional links (GBT)
  - 8 uni-directional links (trigger)

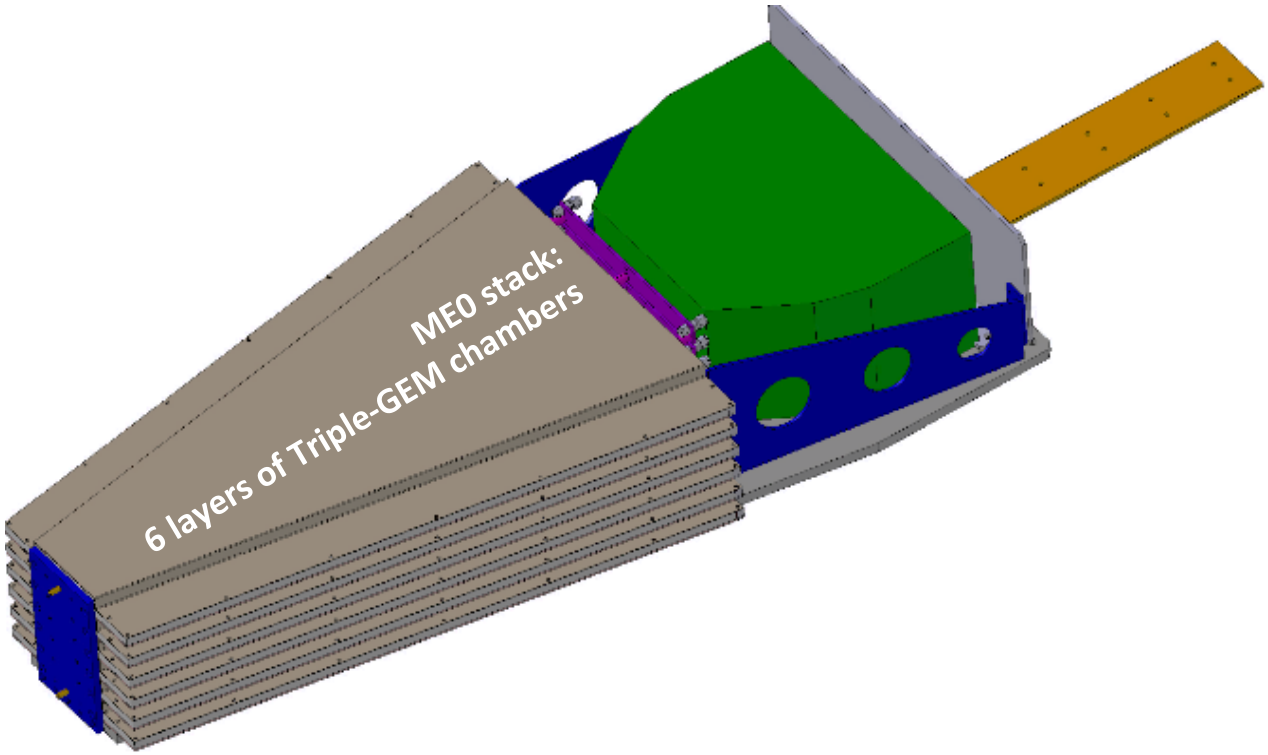
# GE2/1

- The system has the same features as GE1/1
  - One chamber has 2 Opto-hybrids but one chamber spans 20° in $\phi$.
  - Each OH is connected to 24 VFAT3s
- In total, same number of OH and VFAT3
- Optical links can be optimized
  - More details on OH design considerations in Jason talk
- CTP7 is a natural candidate for the backend, but we may want to go to ATCA board
  - More about back-end considerations and links to MTF in Evaldas talk.

# ME0

- 6 layers of **Triple-GEM chambers very similar to the GE1/1 chambers** are expected to satisfy all minimum requirements and consequently constitute the **baseline design for ME0:**



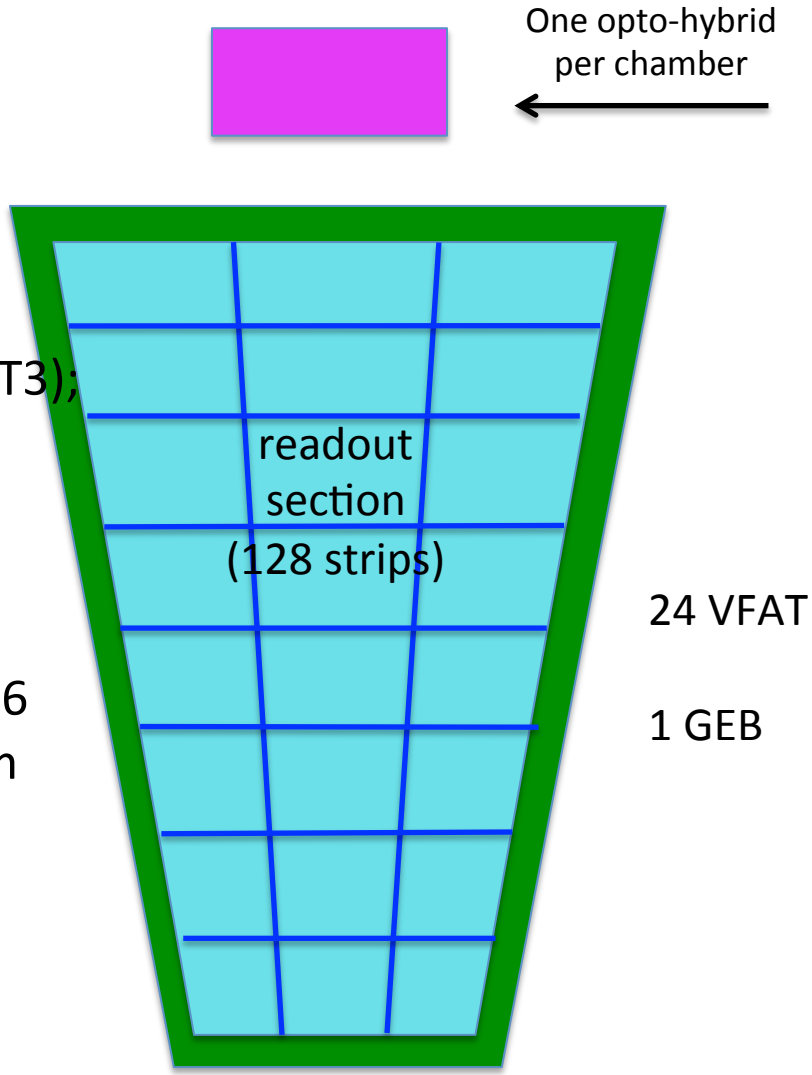




**Triple-GEM chamber (similar to GE1/1)**

# ME0 baseline electronics

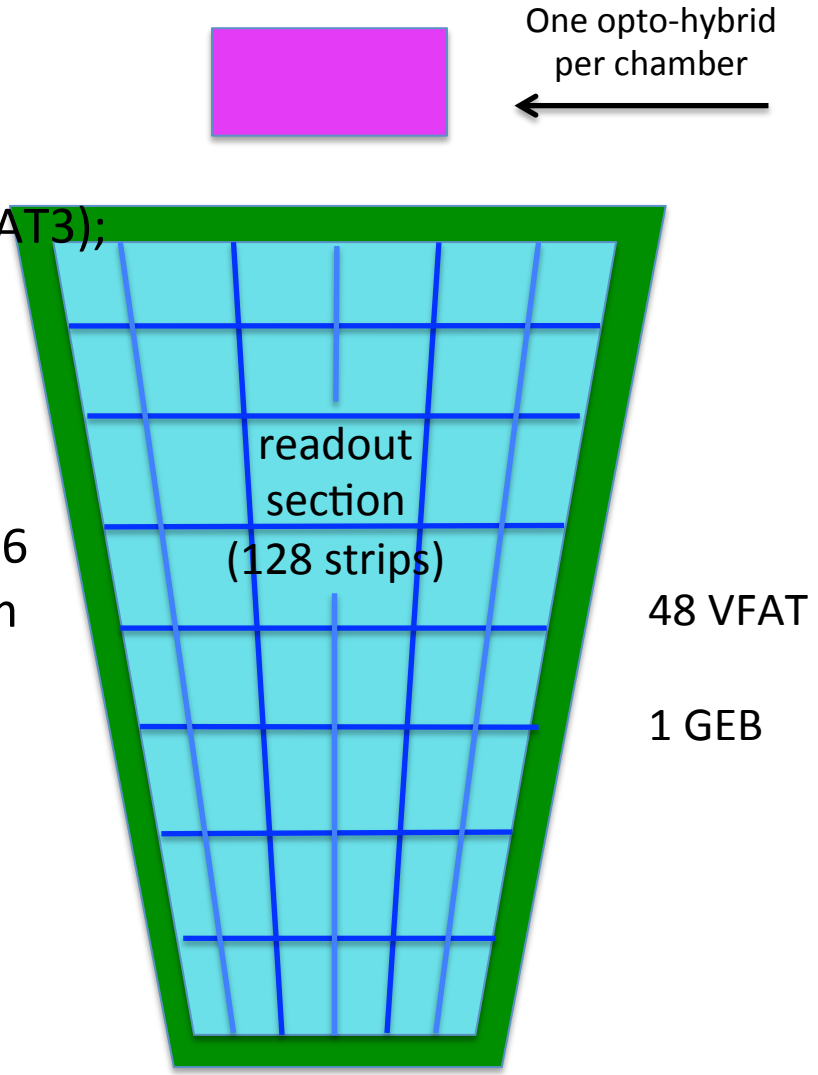
ME0 baseline electronics design closely follows GE1/1 electronics design:

- Current design uses 8η × 3ϕ readout sections (exact segmentation under study)
- 5184 (24 x 6 x 36) binary front-end chips (VFAT3); 128 channels (strips) per VFAT
- 216 opto-hybrids w/ 24 VFAT inputs each
- 1 GEM Electronics Board (GEB) per chamber, 6 GEBs per stack; 216 GEBs total for ME0 system
- If we keep GE1/1 components (GBT, CTP7):
  - 3 GBT links per OH; 648 GBT for ME0
  - 18 CTP7



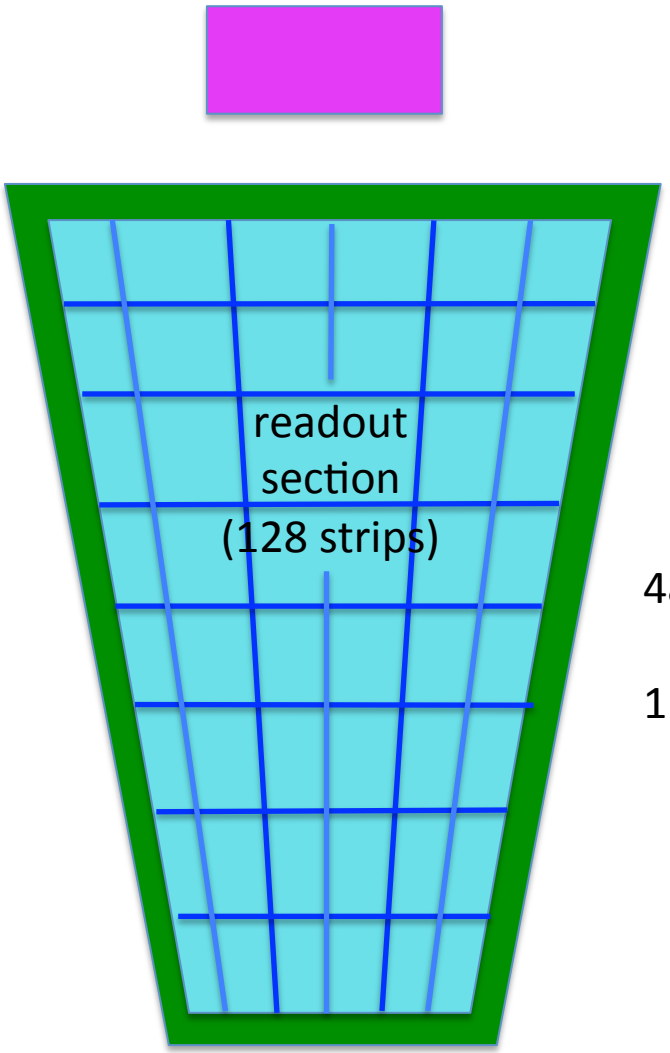
# ME0 electronics option I

- Design uses 8η × 6ϕ readout sections (exact segmentation under study)
- 10368 (48 x 6 x 36) binary front-end chips (VFAT3); 128 channels (strips) per VFAT
- 216 opto-hybrids w/ 48 VFAT inputs each
- 1 GEM Electronics Board (GEB) per chamber, 6 GEBs per stack; 216 GEBs total for ME0 system
- If we use no LpGBT and CTP7:
  - 2 GBT links per OH; 432 LpGBT for ME0
  - But additional non GBT trigger link
  - 18 CTP7



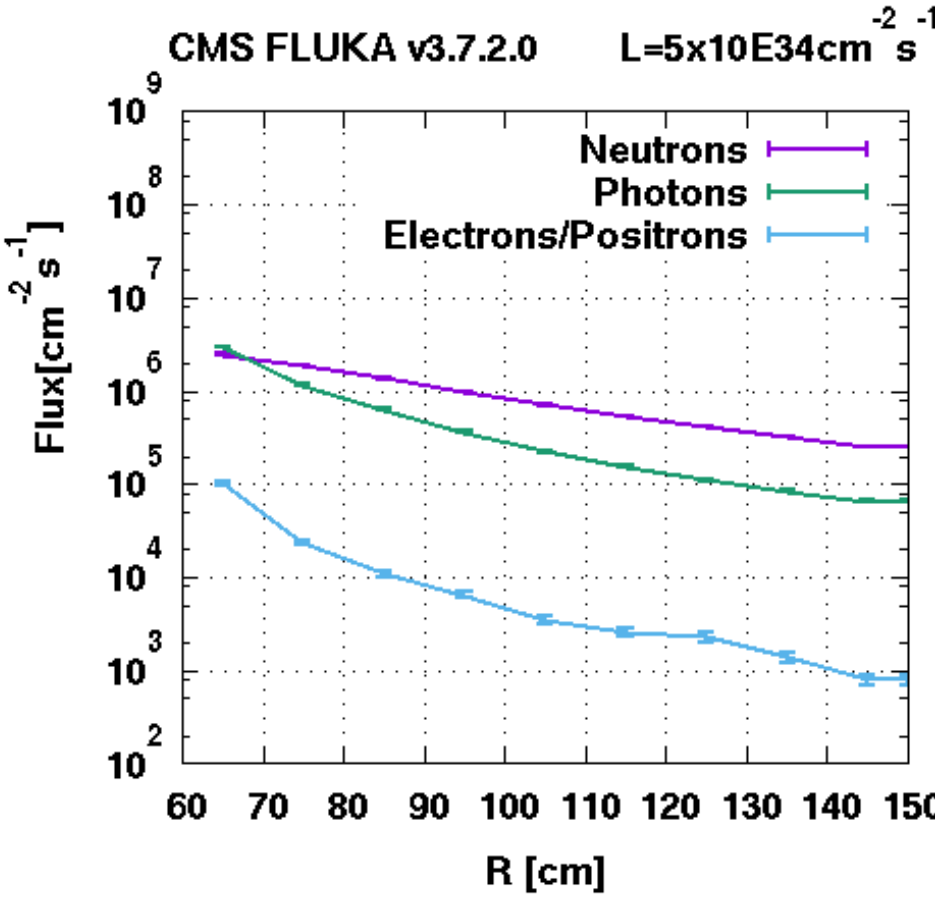
# ME0 electronics option 2

- Design one master OH to reconstruct stubs on superchamber directly
  - Would reduce the number of trigger links and data as well as the number of CTP7 (or equivalent).

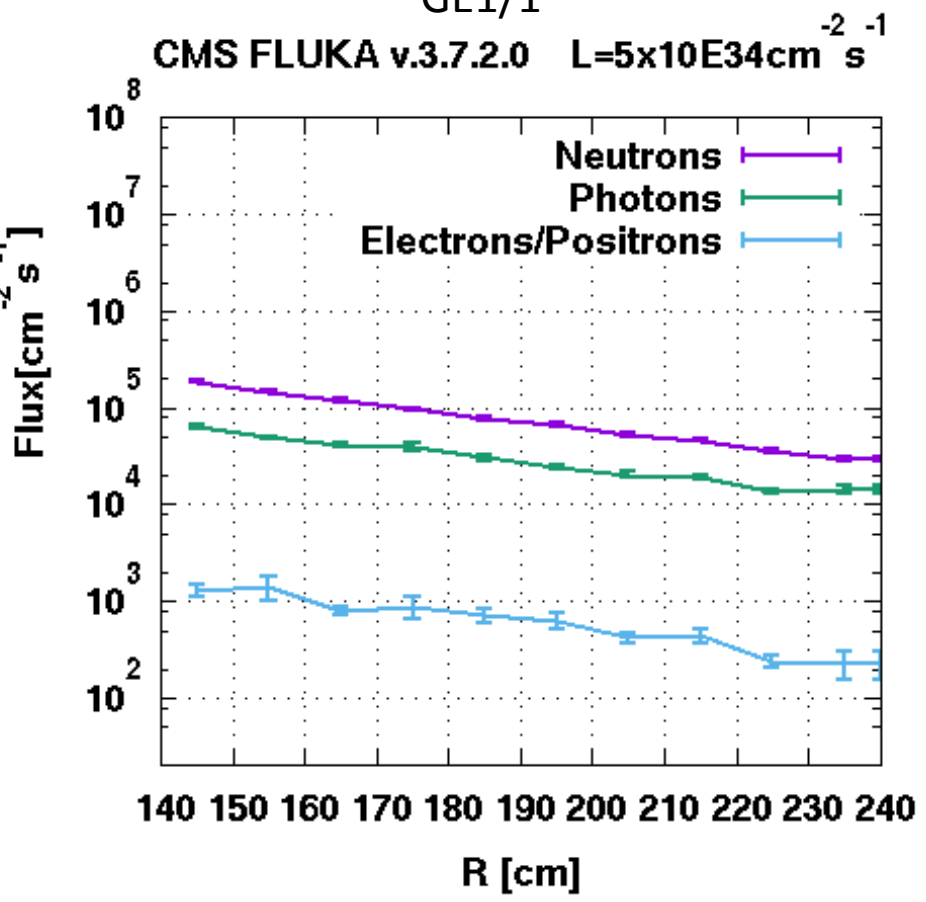


# Radiation

ME0



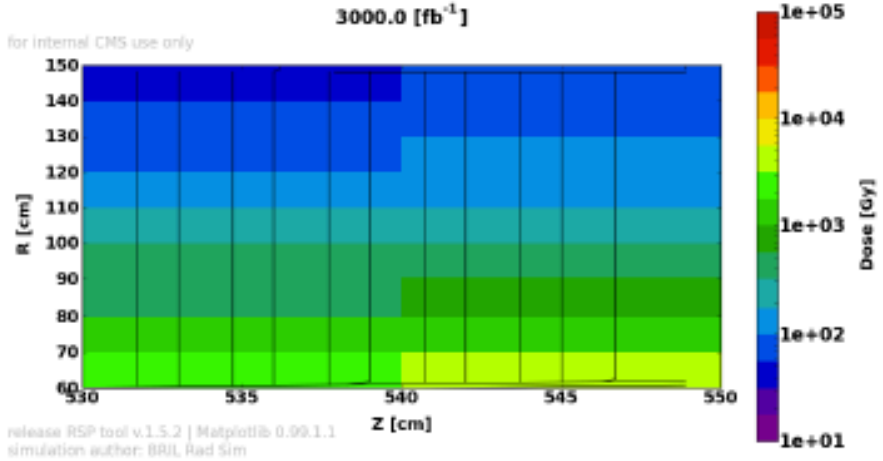

GE1/1



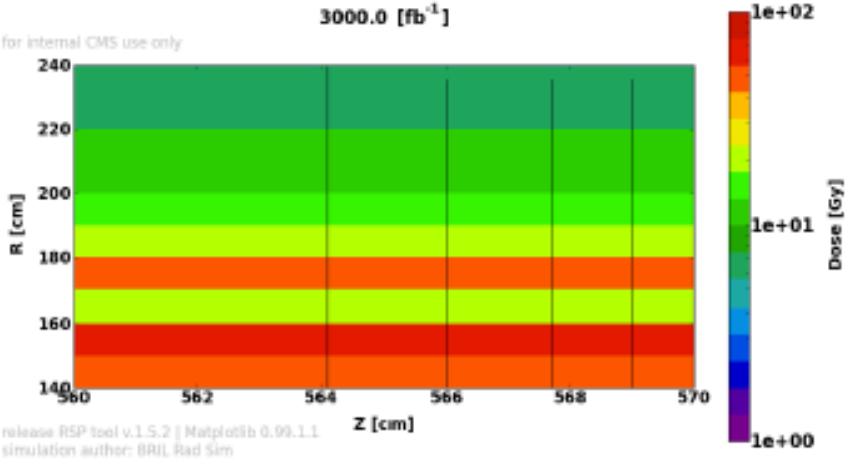

One order of magnitude higher in ME0 !
Need to check rate of SEU on FPGA

# Integrated dose

## ME0




## GE1/1




- Absorbed dose for an integrated luminosity of 3000 fb-1

Need to check that OH FPGA can sustain such dose
(lowest dose in ME0 = 10 krad)

# Conclusions

- GE2/1 electronics system is basically similar to GE1/1 system. Globally it counts the same number of VFAT3 and OH than GE1/1
  - Same hardware (VFAT3, FPGA, GBT, CTP7) could be used
  - However there is room for optical links optimisation
- The system has his own challenges:
  - Large GEB (concerns about signal integrity)
  - OH spanning up to 3 (4?) GEBs
- ME0
  - Should investigate LpGBT to reduce the nbr. of optical links
  - Study in detail background rates -> trigger data rate
    - Is VFAT3 fast enough ? Dead time ?
  - Total dose and FPGA hardness (as well as other OH components)
  - Local stub reconstruction