Xillinx XCFxx EPROM Irradiation Tests

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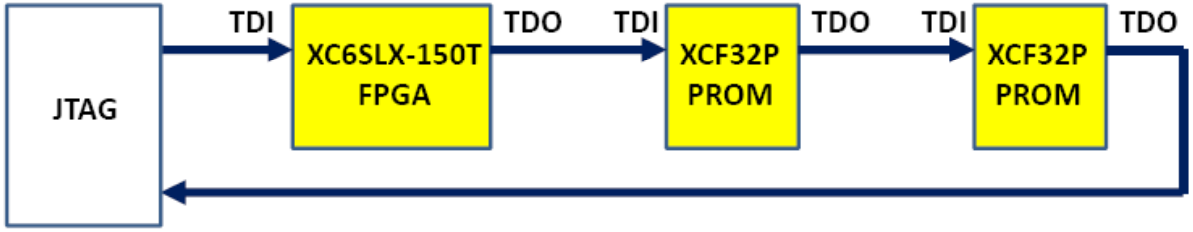
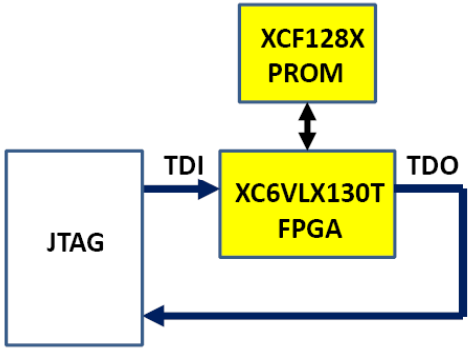
XCFxx EPROMs on EMU boards

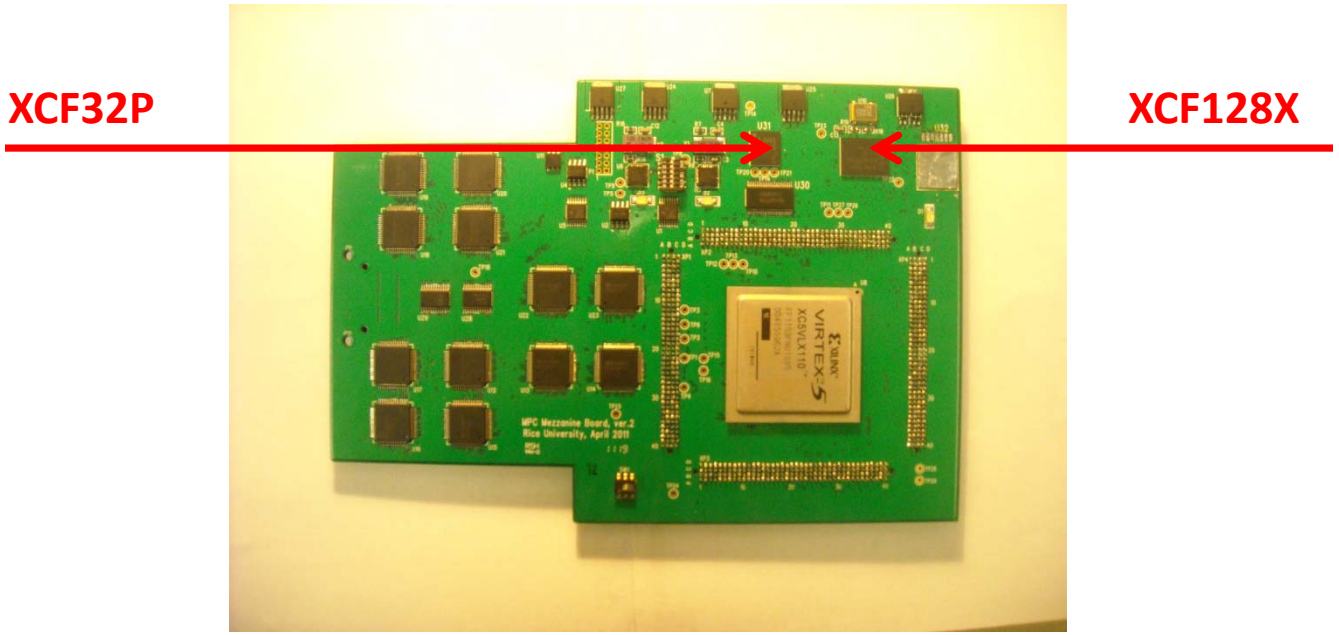




- **XCF08P/32P:**
  - ALCT mezzanines for ME1/1 and ME4/2 (144 boards, 288 EPROMs: XCF32P+XCF08P)
  - MPC mezzanines (60 boards, 120 EPROMs: XCF32P+XCF32P)

- **XCF128X:**
  - DCFEB (504 boards, 504 EPROMs)
  - OTMB mezzanines (72 boards, 72 EPROMs)
  - ODMB baseboards (72 boards, 72 EPROMs)

Previous Irradiation Tests

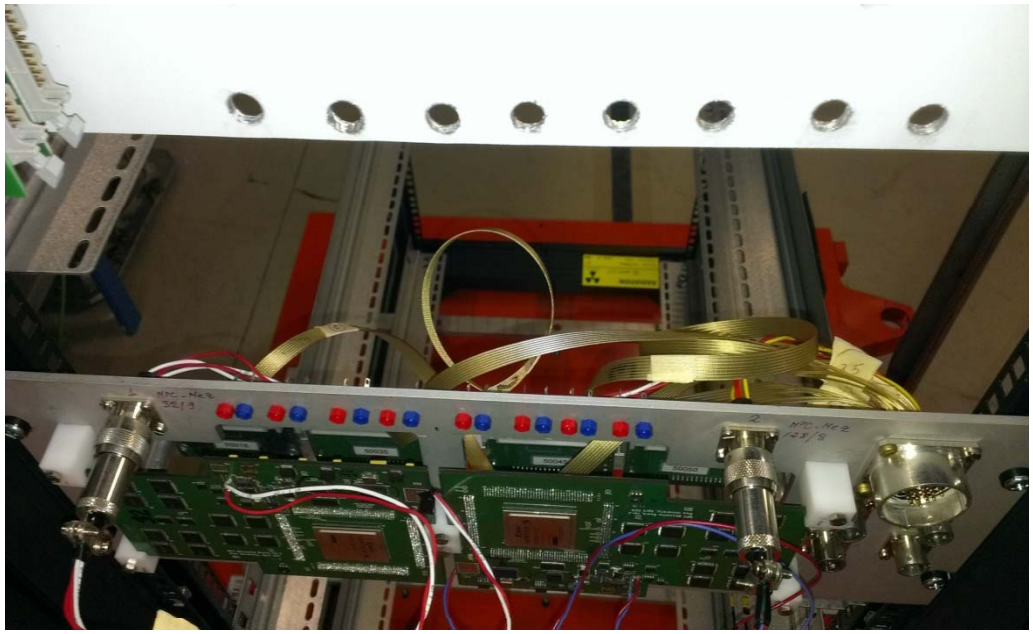


- Both Xilinx EPROMs have been irradiated and showed no bit errors after reading back
  - XCF32P up to 30 kRad without power (TAMU reactor, 2013)
  - XCF128X up to 3.7 kRad under power (TAMU cyclotron, 2011)

- New tests at CHARM, TID >30kRad (HL-LHC), devices under power

- Old Muon Port Card mezzanine board with Virtex-5 FPGA has both EPROMs installed

Irradiation Tests at CHARM



- Two identical mezzanines under test, both powered from a remote Maraton power supply (+3.3V and +1.8V)

- One week of irradiation 26 October – 3 November 2016 at CHARM to reach ~35 kRad

Preliminary Results from CHARM

- Sharp PQ070XZ02ZxH voltage regulator (2.5V VCCAUX) failed on both boards (one produces 2.2V and another 1.3V). These parts were used on prototype boards only. Both regulators were replaced.

- Board 1:
  - XC5VLX110 FPGA: JTAG Readings: IDCODE correct
  - XCF32P programming/verification mostly OK, but on few occasions saw error

Failed at address 3145728'1' verification terminated

  - XCF128X programming and erase failed with a message

Unable to load "erase" instruction to device

- Board 2:
  - Few bit flips on both EPROMS after irradiation
  - XC5VLX110 FPGA: JTAG Readings: IDCODE correct
  - XCF32P: programmed and verified several times with different files, always OK.
  - XCF128X: programming and erase failed with a message

Unable to load "erase" instruction to device