

Plans for Rad Testing New Components (LS2)

1. Produce Artix 7 based test boards
 - a) Mezzanine board for test PROMs (PC28F128P30T, XCF128X, XCF32P(JTAG connection only))
 - b) Connectors/socket options for optical transceivers (need specifications)
 - c) Options for testing Artix 7 features
 - d) Produce enough for rad testing at TAMU and UC Davis, and general testing at multiple sites.
2. Exposure plan
 - a) Tests at TAMU (neutrons up to 10 MeV)
 - 1) Incremental exposure up to 30 KRads (5 KRad increments?)
 - 2) Powered with ability to test at intervals
 - 3) Test multiple PROMs of each type (how many?) (simultaneous testing with multiple boards?)
 - b) Tests at UC Davis (Protons at 63 MeV)
 - 1) TID and SEU testing (continuous read back of PROM)
 - 2) Erase/Reprogram tests at incremental stages up to 30 KRads
 - 3) Test multiple PROMs of each type (simultaneous testing with multiple boards?)
 - 4) Test Artix 7 FPGA for TID (SEU testing of CRAM, BRAM, fabric ?)
3. Other components need testing?

ME1/1 DCFEBs, OTMBs, and ODMBs

1. ME1/1 DCFEBs
 - a) Retrieve DCFEBs from extracted chambers during YETS
 - b) Ship DCFEBs to OSU for study (OSU RP requests CERN for transport)
 - c) Ship MPC mezzanine boards to Rice for study (Rice RP requests CERN for transport)
 - d) Firmware updates during Run2 and Run3 (Weigh importance against risk)
2. OTMB design for LS2 – choose PROM option for mezzanine board
3. OTMB/ODMB during Run 2 and Run 3
 - a) If PROM issues arise, Swap boards, replace PROM
 - b) Implies need to buy XCF128's while we can (qty ?)
4. DCFEBs on ME1/1 during LS3 (options if PROM issues continue)
 - a) Replace DCFEBs with upgraded version:
 - Would be most economical to double production now
 - b) Replace all PROMs with new XCF128, (need to buy >504 now)
 - c) Replace all PROMs with PC28F128PC30T (requires adapter board, feasibility?)