GE1/1 backend electronics

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1. GE1/1 backend -- CTP7

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- **CTP7 selected as GE1/1 backend**
- **Powerful FPGA**
  - Virtex 7 690T (690k logic cells), speed grade -2
    - 53Mb block RAM → large DAQ buffers
      - Additional 36Mb external RAM chip is available for FIFO use
  - Optical interface: 67 RX and 48 TX (up to 10Gbs)
- **Zynq 7000 processor as on-board controller (unique feature)**
  - Embedded linux, powerful monitoring & control features
    - Fast AXI bus to Virtex 7 FPGA (32bit @ 50MHz)
    - Remote programming and debugging (virtual Xilinx cable)
    - Embedded applications (monitoring, control, readout, web server)
    - Remote procedure call service
    - uHAL via TCP/IP interface
- **Great support from University of Wisconsin**
  - Thomas Gorski, Aleš Svetek, Marcelo Vicente, Jesra Tikalsky
  - Provided 3 boards with demo firmware (TAMU, b904, TIF)
  - Setup all infrastructure needed to use the boards
  - Provided support for firmware development
  - Solved some critical issues (e.g. deterministic clock phase)

2. CTP7 in GE1/1 system

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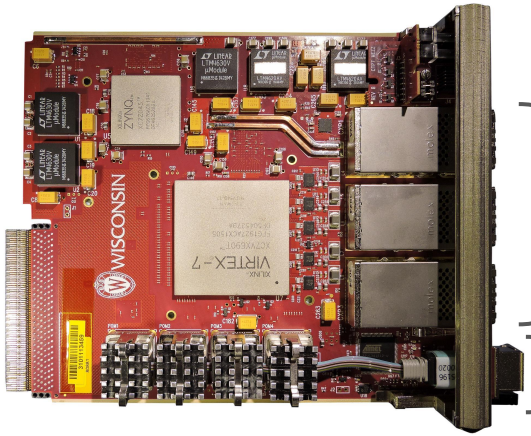
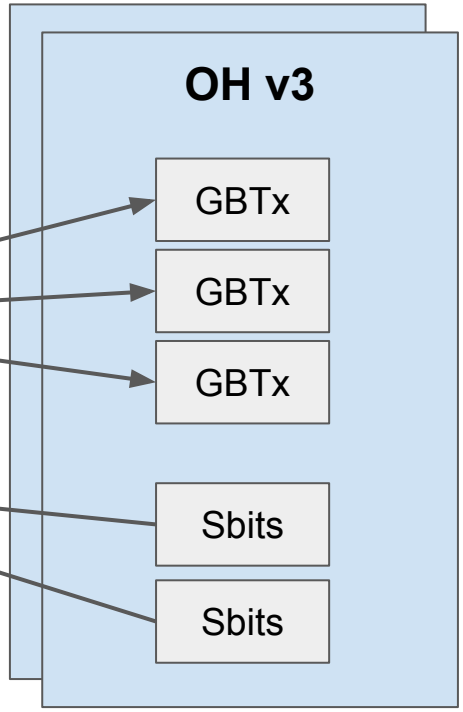
6 CTP7 per endcap
60 degrees per board



12x OHs per CTP7



4.8Gbs

3.2Gbs

9.8Gbs

EMTF Sector Processor

One CTP7 for one SP
6 MTF7s per endcap
60 degrees per MTF7

- One CTP7 runs 36 GBT cores
- 12 CTP7 for full GE1/1 system
  - One board can handle all slice test
- SBit data will be concentrated
  - 24 x 3.2Gbs from OH 8 x 9.8Gbs to EMTF

3. GE1/1 experience with CTP7

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- **Fully functional CTP7 firmware**
  - Supports 12 OHs
    - 36 GBT links with fixed clock phase
    - Fast control
    - Slow control
    - SCA: hard-reset, JTAG, monitoring
    - DAQ
      - Data readout
      - Buffering
      - Processing
      - Error checking, status reporting (TTS)
    - Receives trigger data
      - Monitoring, simple local trigger
      - Sbit connectivity scan

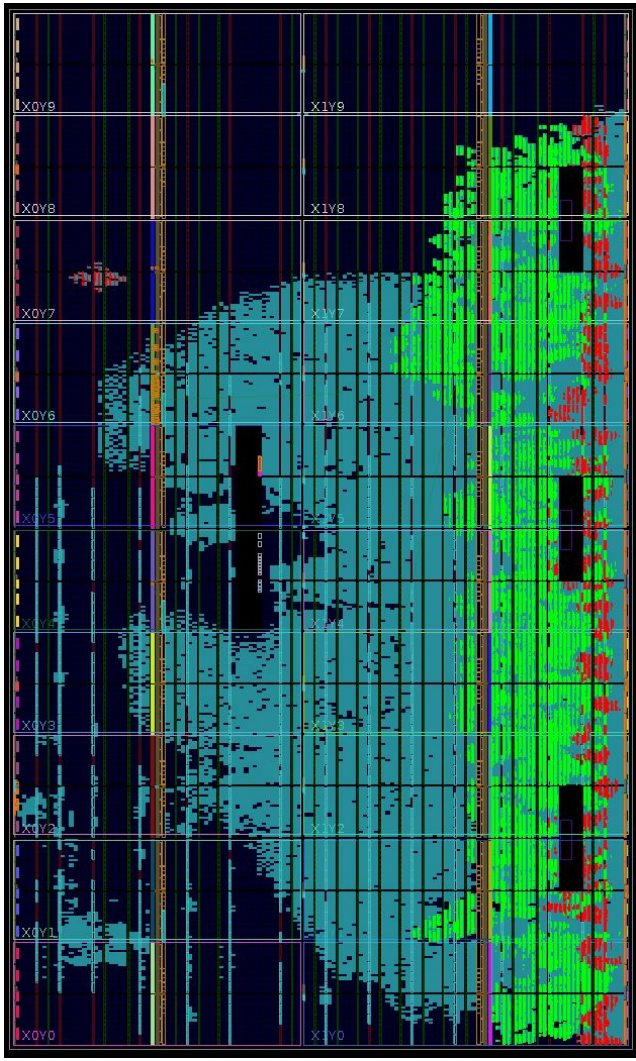
DONE

  - TODO:
    - Trigger data readout through DAQ
    - Trigger synchronization and concentration
    - MiniPOD links being tested

TODO

  - Chip utilization is very good
  - Easily portable to different boards (e.g. ATCA)
    - GLIB implementation exists (same code)

CTP7 firmware with 36 GBT links



Green = GBT RX cores
Red = GBT TX cores (fixed latency)
The rest is mostly DAQ, ctrl and Trigger

4. CTP7 stability tests with GE1/1

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- **Loopback tests through fiber (no OH)**
  - Trillions of bits transmitted, no errors detected
  - Stable 8b10b links -- 12 links simultaneously
  - Stable GBT links -- 36 links simultaneously
- **Loopbacks through fiber with OH in the loop**
  - Send data to OH through control link
    - OH retransmits all data back through control link + 2 trigger links
    - Ran simultaneously on 9 OHs
    - 51 TeraBit transmitted, no errors detected
  - Send data to OH GBTx, all data looped back at GBTx chip
    - Ran simultaneously on 9 OHs
    - 800 TeraBits transmitted, no errors detected
  - Send data to OH GBTx -> OH FPGA -> OH GBTx -> CTP7
    - Trillions of bits transmitted, no error detected
- **Register access stress test over GBT link**
  - 5 million write -> readback transactions done on 9 OHs -- no errors
- **DAQ stable with 12 OH data up to 4Gbs throughput**
  - Data replicated 12 times from 1 OH
  - 4Gbs is a limitation of AMC13

10. DAQ considerations for post-LS3

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- **Higher luminosity: 7 * 10^34**
  - ~4x higher than pre-LS3
- **Higher L1A rate: 750kHz**
  - 7.5x higher than pre-LS3
- **DAQ data rate scales linearly with both of these variables**
  - Assuming the same muon “richness” in L1 trigger
  - Post-LS3 data rate = pre-LS3 data rate x 4 x 7.5
    - **That’s 30 times higher!**
- **Nick’s occupancy estimation for GE1/1**
  - 0.077 PU hits per layer per BX
  - 0.087 background hits per layer per BX
  - Total = 0.164 hits
    - But hits on the edge of two VFATs will generate two VFAT packets
    - Not sure what the fraction of these hits is exactly, but it’s not very high
  - Rounding up to 0.2 VFAT blocks per layer per BX
  - Per CTP7: 0.2 hits * 12 layers * 192bits * 750kHz L1A rate = **330Mbit/s**
    - No problem -- backplane can handle 4Gbs (safety factor = 12)
  - Per AMC13: 330Mbit/s * 12 = **3.9Gbs**
    - No problem -- AMC13 output is 24Gbs (safety factor = 6)

11. Summary

- **Main functions of the firmware are already implemented and well tested**
  - Trigger path needs some work, but requirements are well understood and fit the current hardware architecture
  - Plug-and-play for GE2/1

- **Enough bandwidth for post-LS3**