Velopix, a new hybrid pixel readout ASIC for the LHCB VELO LS2 upgrade

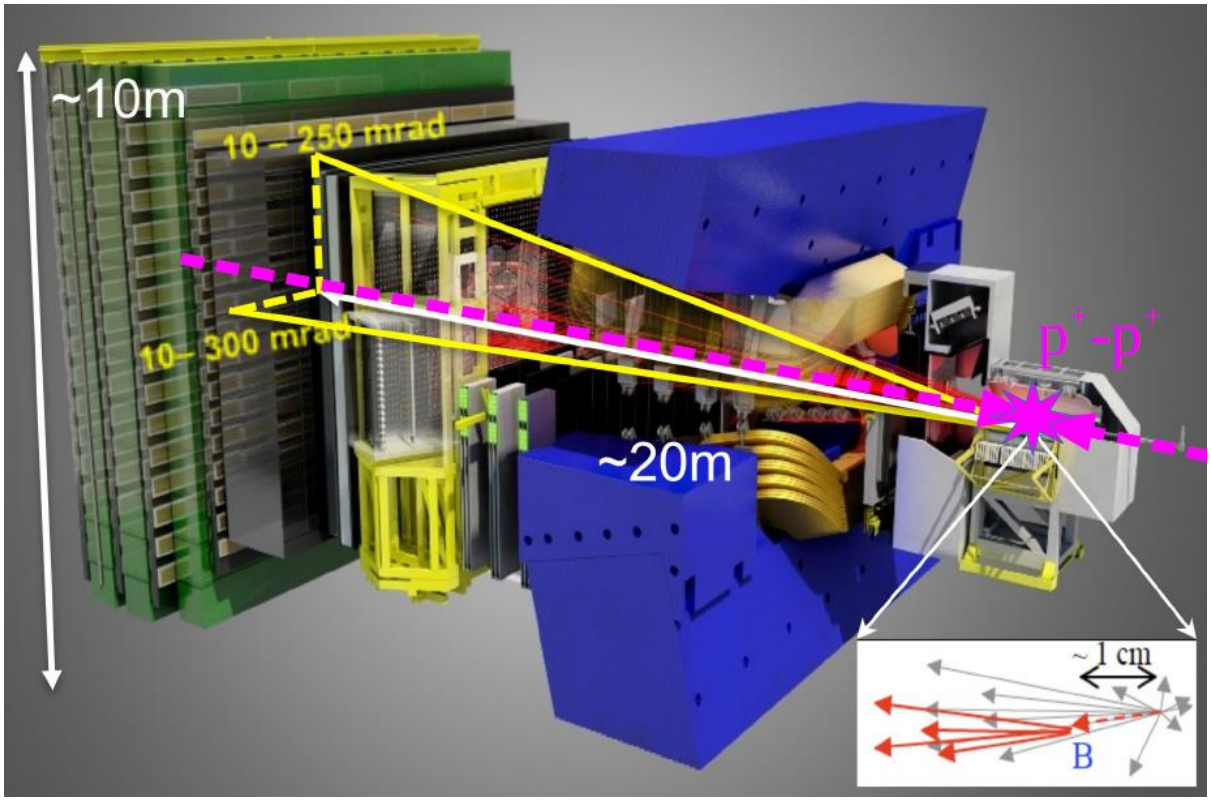
CERN, NIKHEF and USC

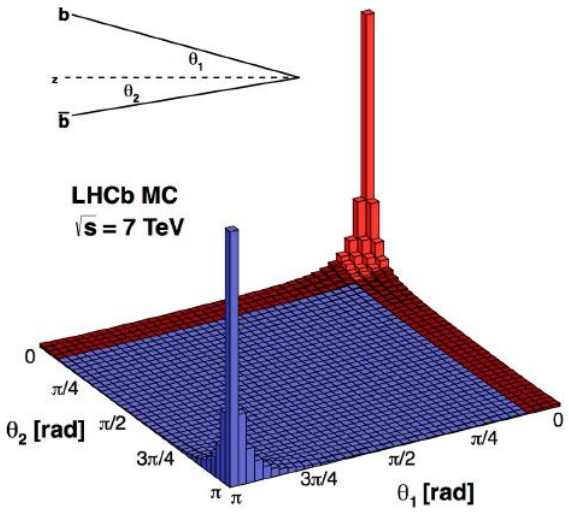
Outline

- Introduction to the VELO upgrade (Martin)
- The VeloPix chip (Martin):
  - Velopix FE (Rafa)
  - Digital pixel (+eCDRPLL) (Xavi)
  - Super Pixel, EOC, periphery and GWT (Tuomas)
- Measurements (Jan)
- Conclusion (Jan)

M. VAN BEUZEKOM

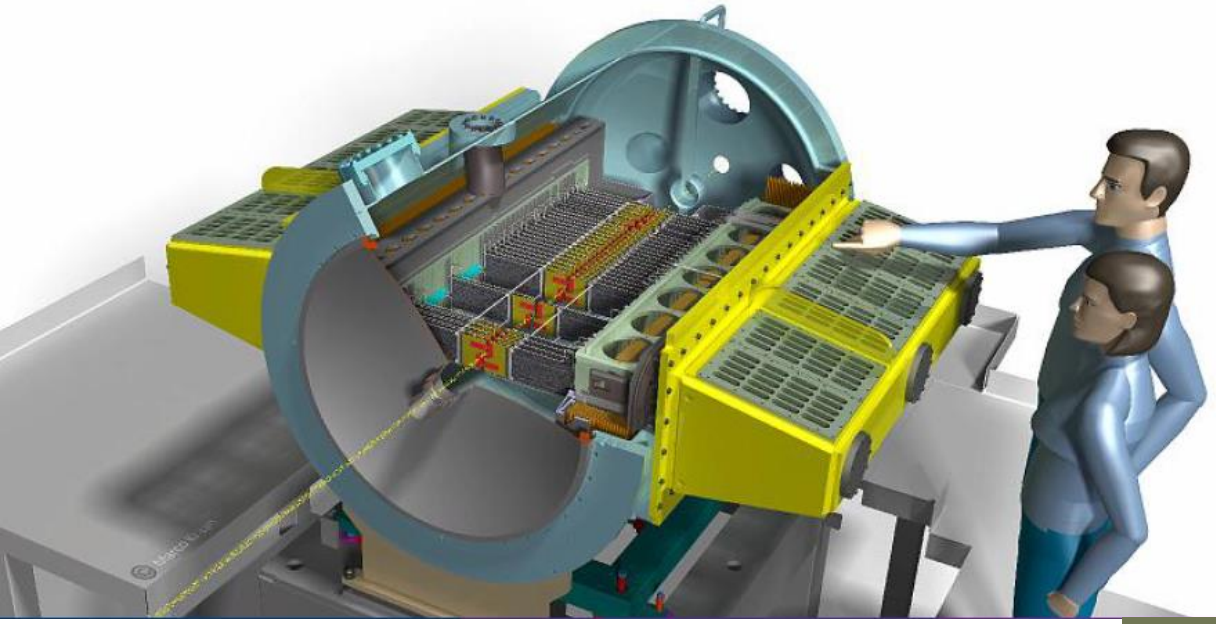
Introduction to LHCb and its upgrade





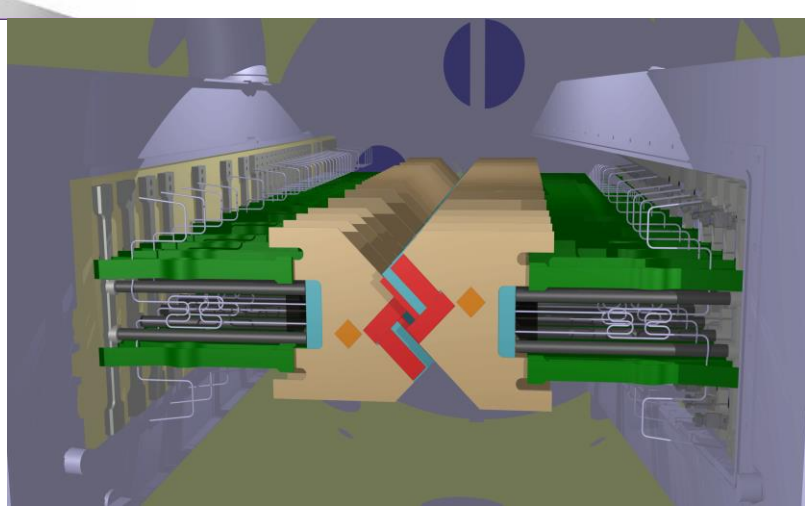
- LHCb is a dedicated experiment searching for new physics by studying CP violation and rare decays of b and c quarks
- Forward angle spectrometer with excellent vertex resolution and PID
- Detector upgrade in 2019→2020 for 5x higher luminosity and improved efficiency
- No more hardware trigger → all data data read out and sent to CPU farm

Vertex Locator Upgrade



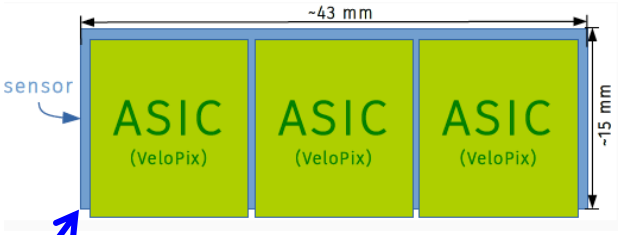
LHCb will be upgraded in 2019→2020
→ very tight planning

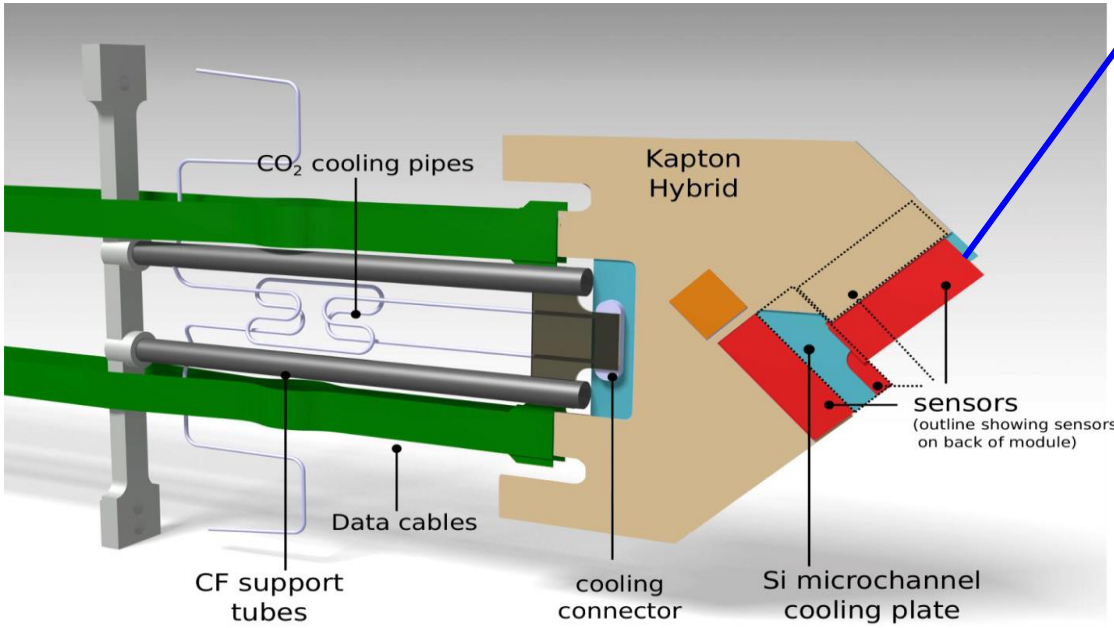
- Vertex detector surrounding collision region
  - In vacuum
  - Close to the beam: 5.1 mm
- From silicon strips to pixels
- New R/O chip VeloPix, derived from Timepix3
- In total 624 ASICs, ~41 Mpixels
- Trigger-less readout (~2.9 Tbits/s)

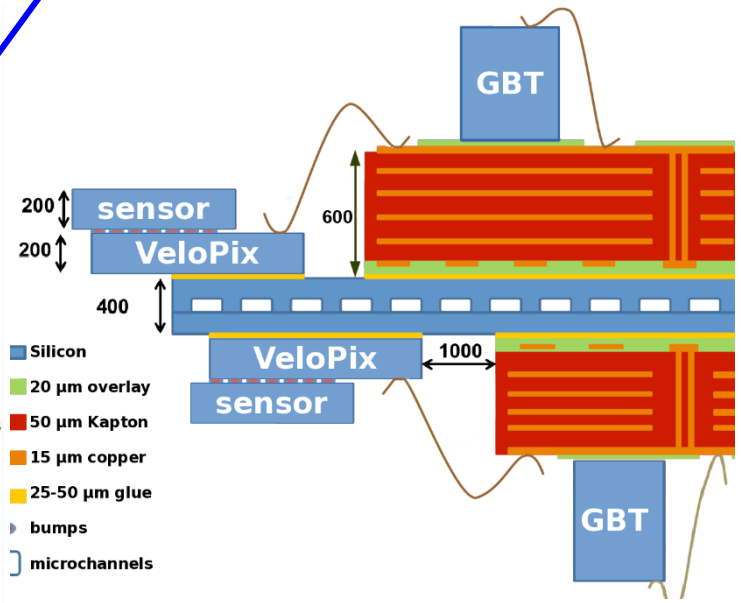


VELO module

- One module = 4 sensors with 3 VeloPix ASICs each
- 256x256 pixels/ASIC, 55 x 55 µm^2 pixels
- ASICs thinned to 200 µm
- All silicon module, minimal CTE mismatch
- Si substrate with m-channel evaporative CO_2 cooling
  - sensors < -25 °C
- Sensor signal at end-of-life ~7000 e-







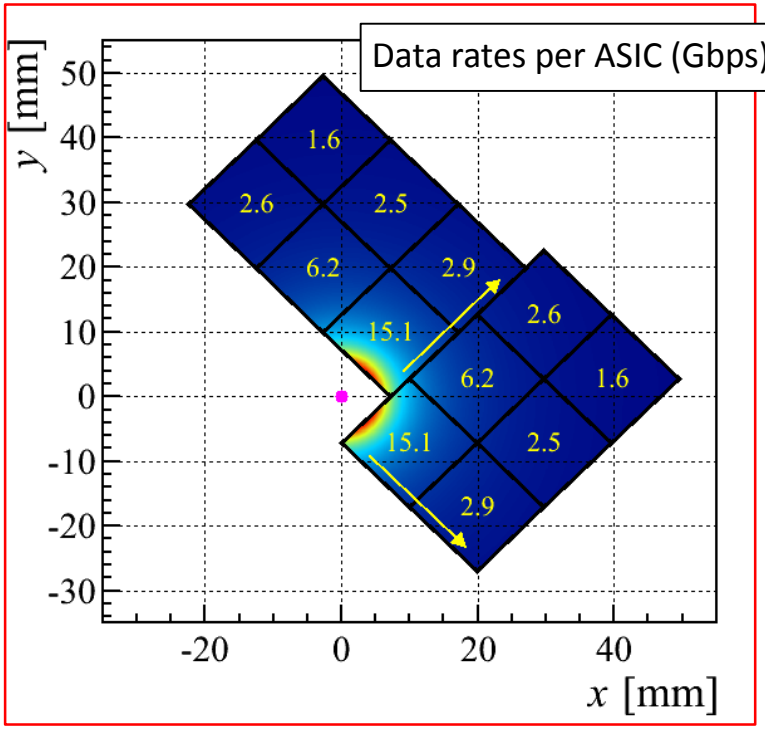
ASIC challenges: data rate & radiation hardness

- Sensor and ASIC exposed to high, non-homogeneous, radiation fluence
  - Only part of the pixel matrix gets the full dose of ~ 370 Mrad
  - TID at periphery of chip is factor 10 lower

- For data rates calc. we assume collisions in every LHCb bunch crossing
  - in reality only 2/3 of bunches collide
  - would require a lot of memory to level out
  - → assume peak rates for ASIC design
- Data flow simulations using physics Monte Carlo data

- No trigger, all data sent off chip
- Hottest ASIC gives ~15 Gbps

- ASIC design starting point: Timepix3

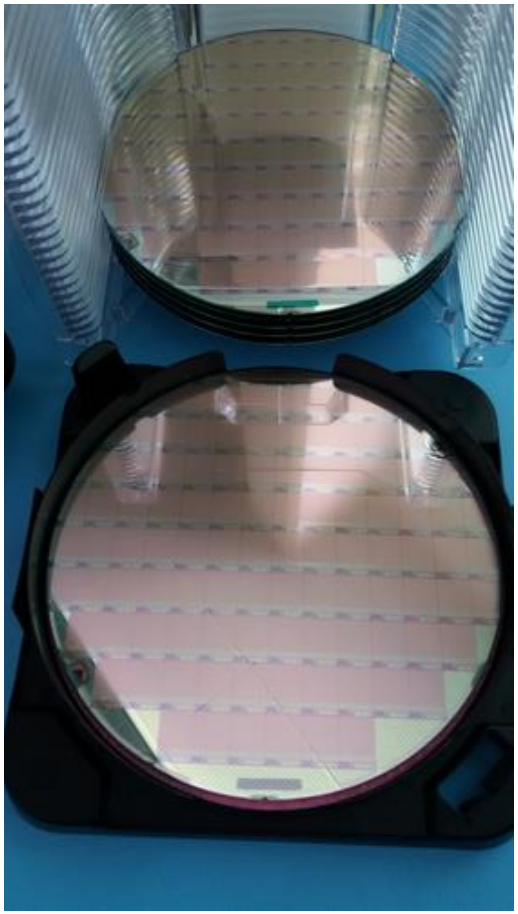


From Timepix3 → Velopix

	Timepix3 (2013)	VeloPix (2016)
Pixel arrangement	256 x 256	
Pixel size	55 x 55 µm²	
Peak hit rate	80 Mhits/s/ASIC	800 Mhits/s/ASIC 50 khits/s/pixel
Readout type	Continuous, trigger-less, TOT	Continuous, trigger-less, binary
Timing resolution/range	1.5625 ns, 18 bits	25 ns, 9 bits
Total Power consumption	<1.5 W	< 3 W
Radiation hardness		400 Mrad, SEU tolerant
Sensor type	Various, e- and h+ collection	Planar silicon, e- collection
Max. data rate	5.12 Gbps	20.48 Gbps
Technology	IBM 130 nm CMOS	TSMC 130 nm CMOS

VeloPix Project Overview

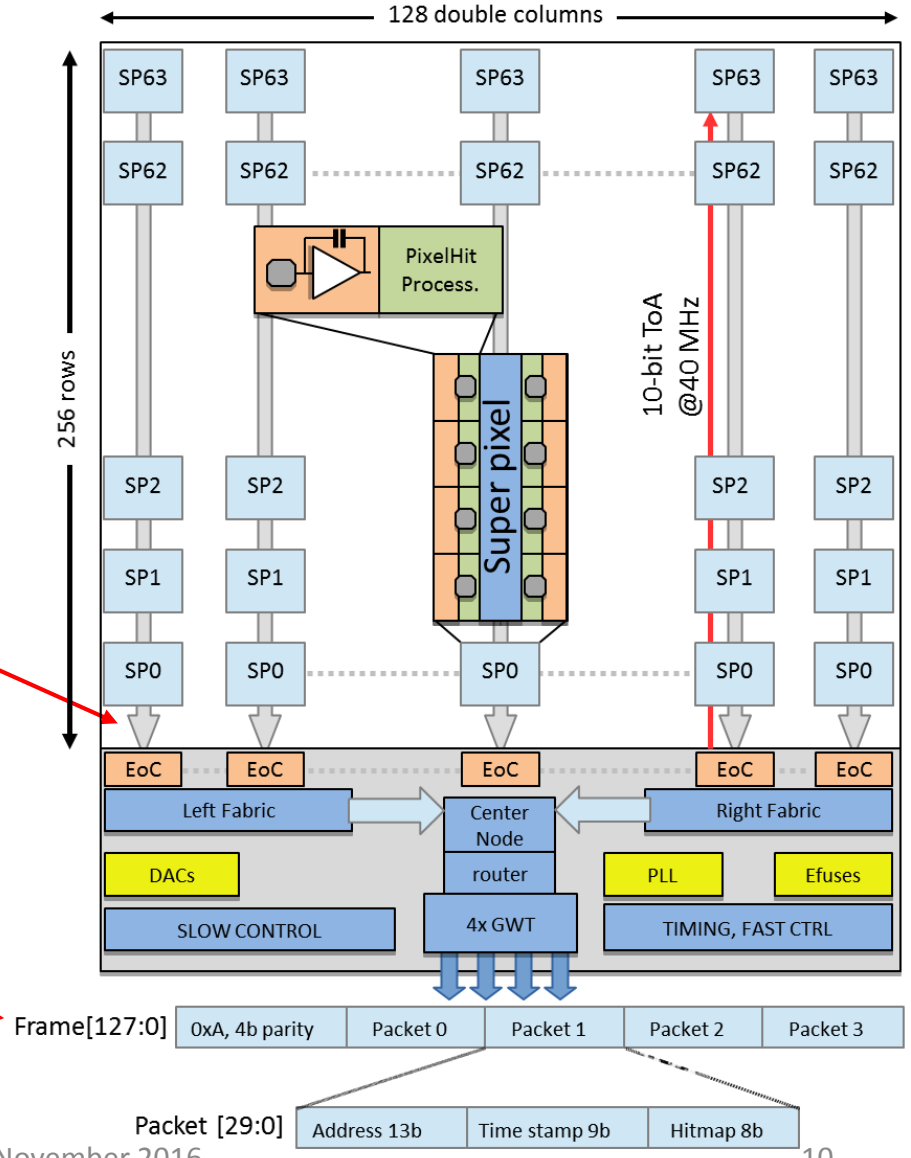
- Design started in June 2013 (after Timepix3 submission)
- Change of technology (IBM 130nm → TSMC 130nm)
- The chip was submitted as an engineering run on May 2016
- First wafers received on 31st August
- Fabricated (and diced) chips back at CERN on 7th September
- First beam tests done on 6th November
- Production testing later this year (624 chips)
- Irradiation campaign in the future with sensors bonded



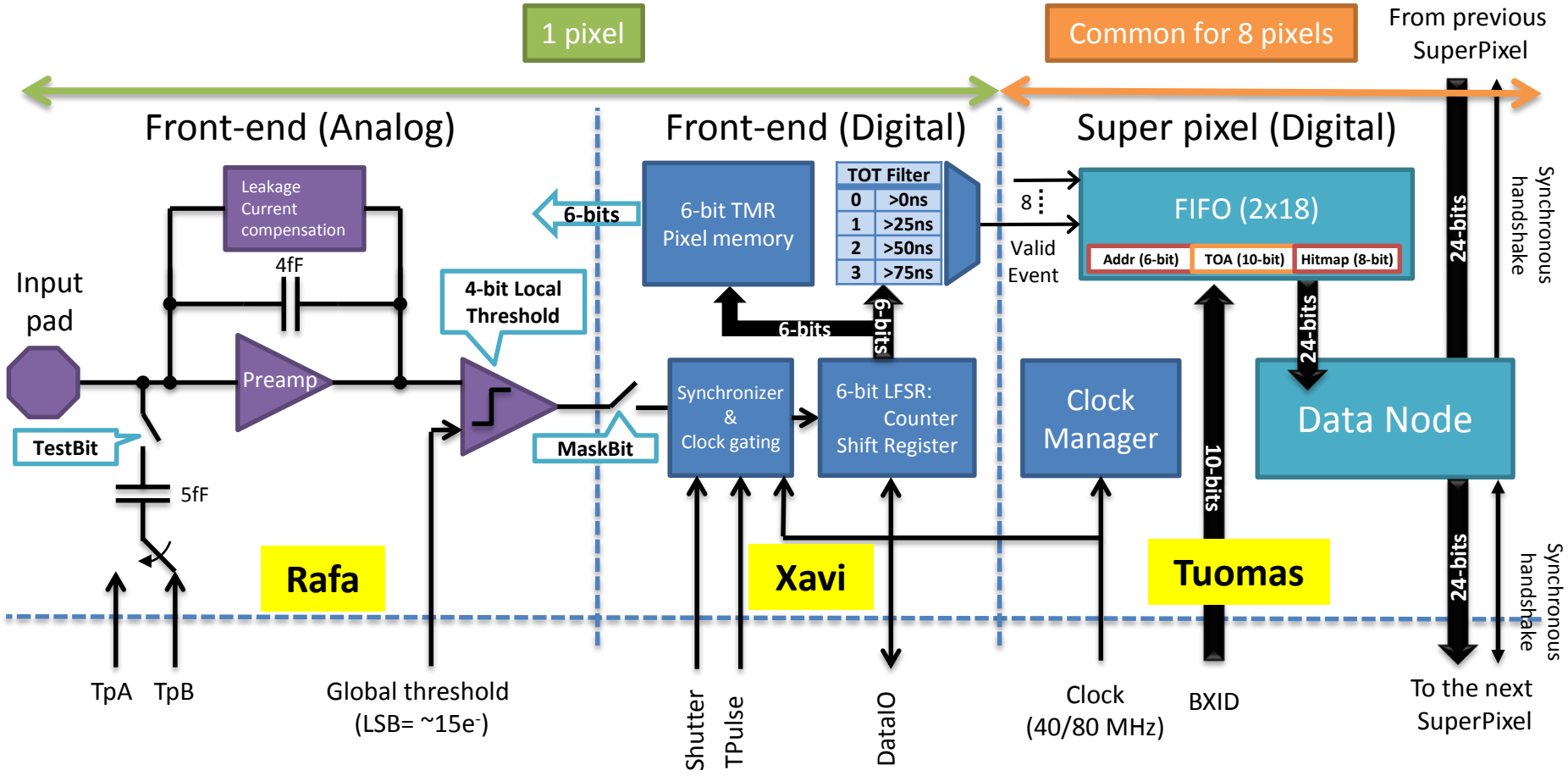
VeloPix wafers

VeloPix Chip Architecture

- Pixel matrix:
  - 256 x 256 pixels
  - 128 x 64 super pixels (2x4 pixels each)
  - @40MHz
- Packet-based architecture:
  - 8 pixels/packet + 9 bit time stamp → 30% reduction in data rate
- Data-driven readout:
  - 20 Mpackets/s/double column
- 40, 80, 160 and 320 MHz TMR clock domains in the periphery
- 1 to 4 configurable serializers (GWT)
- Similar to the GBT frame



VeloPix pixel schematic

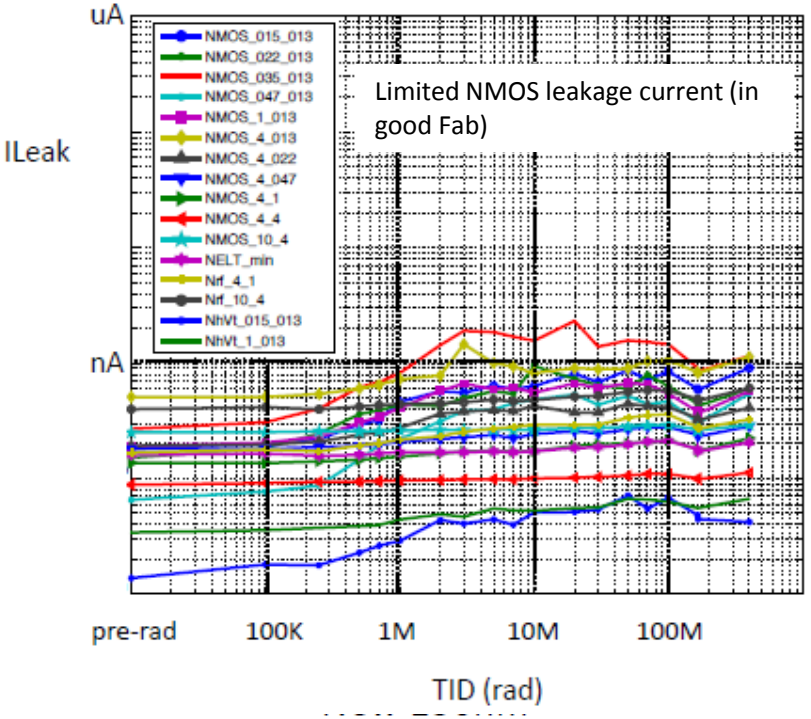


R.BALLABRIGA

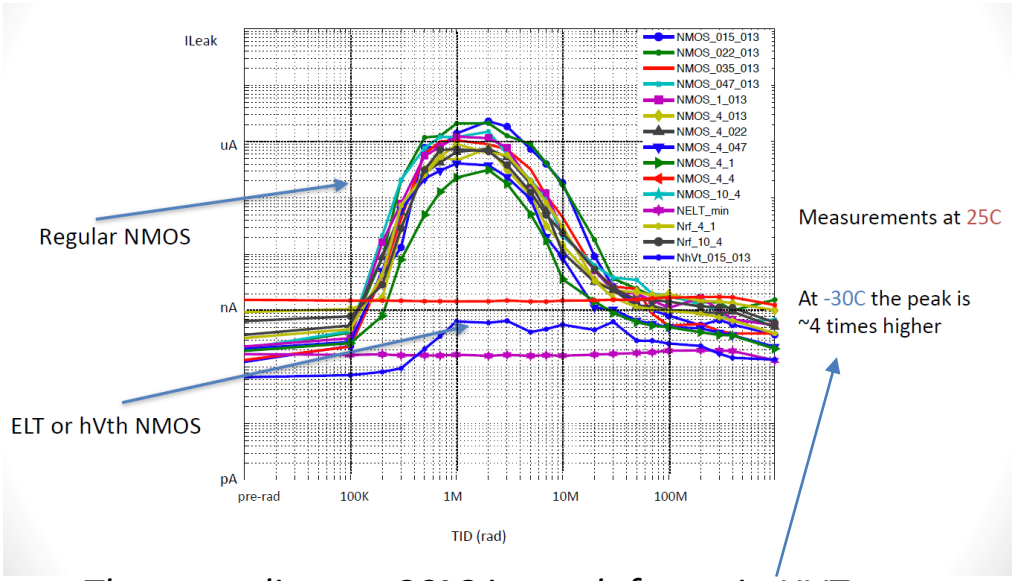
Specifications

Parameter	Value
Technology	TSMC 130nm CMOS
Number of pixels	256 x 256 @ 55 μm pitch
Analog front-end size	55 x 14.5 μm
Analog supply voltage	1.2 V
Detector capacitance	50 fF
Detector polarity	Optimized for electron collection
Maximum of charge distribution	16ke^- (200μm Si @ 80e^-h^+ pairs per μm)
Leakage current	Up to 12nA/pixel (non-uniform)
Minimum threshold	~500e^-
Pile-up	Discharge of 16ke^- charge in 300ns
Time of arrival resolution	25ns
Operating temperature (in experiment)	-30°C<T<0°C
Analog power consumption	~6.1μW/pixel 200mW/cm^2 (250mW/cm^2) (constant)

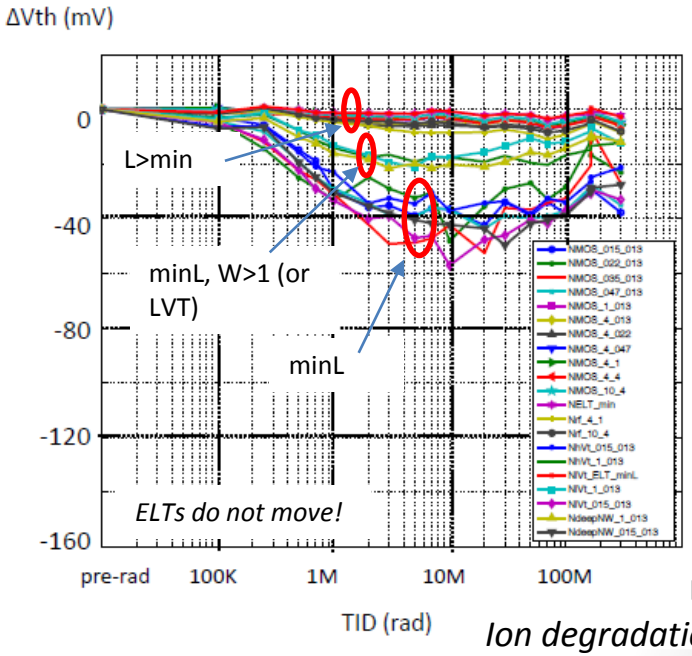
FAB 6 (NMOS)



FAB 14 (NMOS)



The annealing at -30°C is much faster in HVT transistors wrt regular transistors



Ion degradation<5%

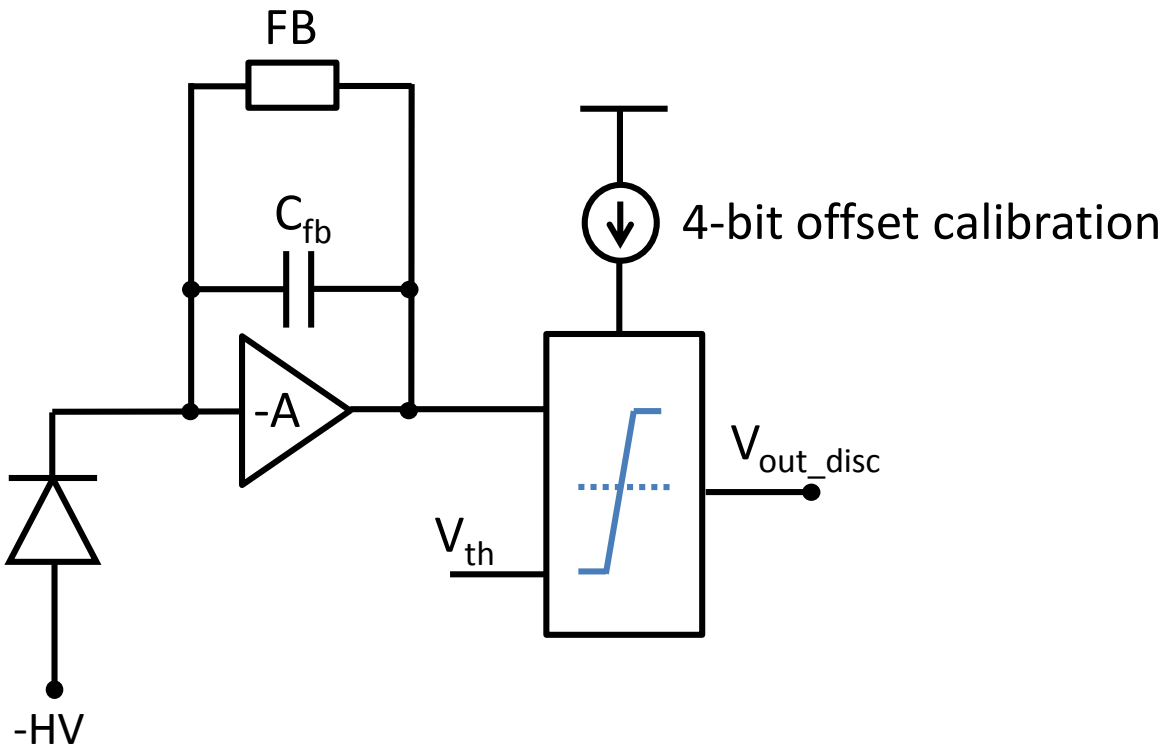
2 Fabs showed different results in terms of leakage for the NMOS transistors

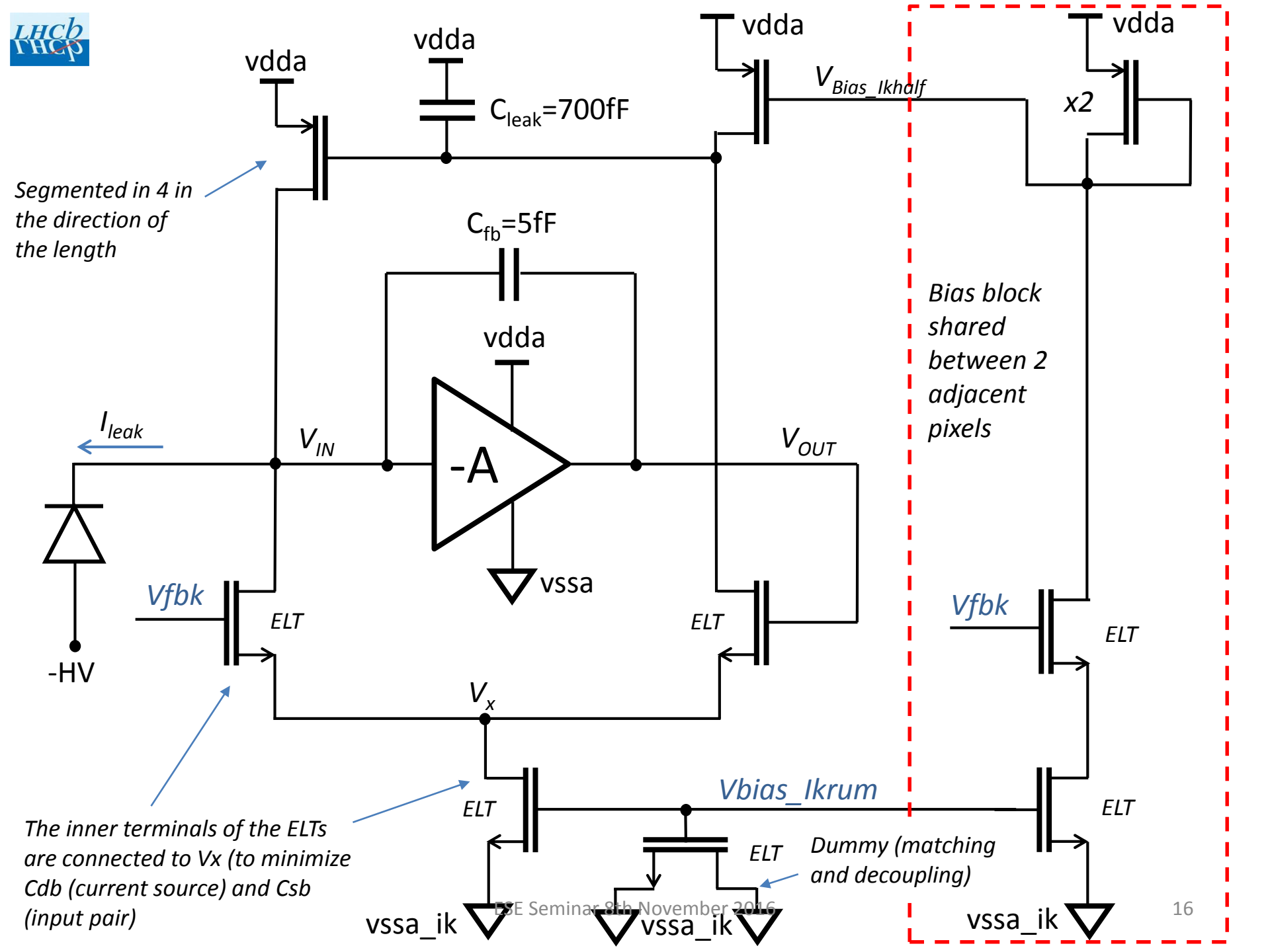
We decided to design for the worst case i.e.:

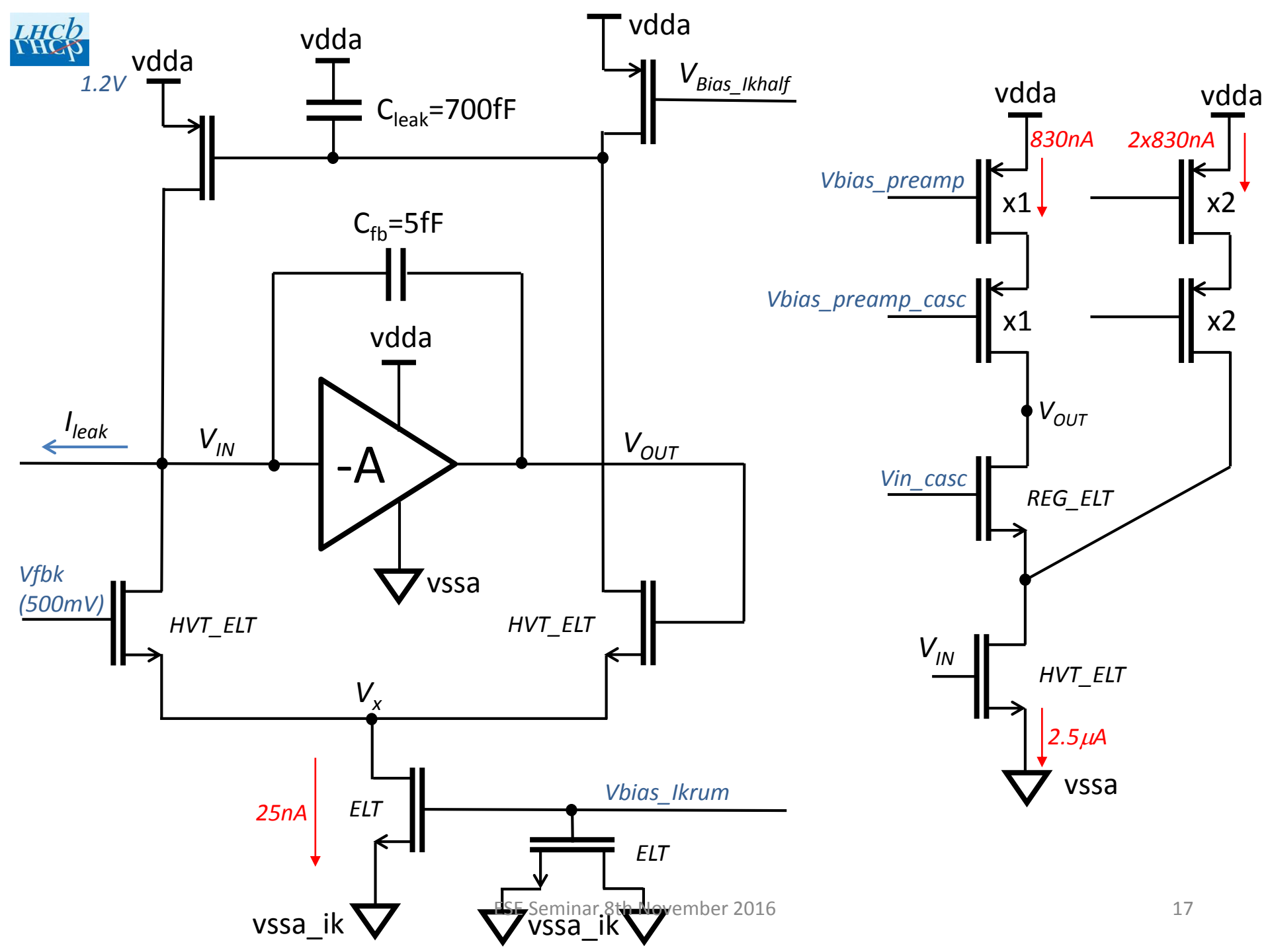
NMOS transistors either ELT or HVT

Radiation measurements: S. Michelis, F. Faccio

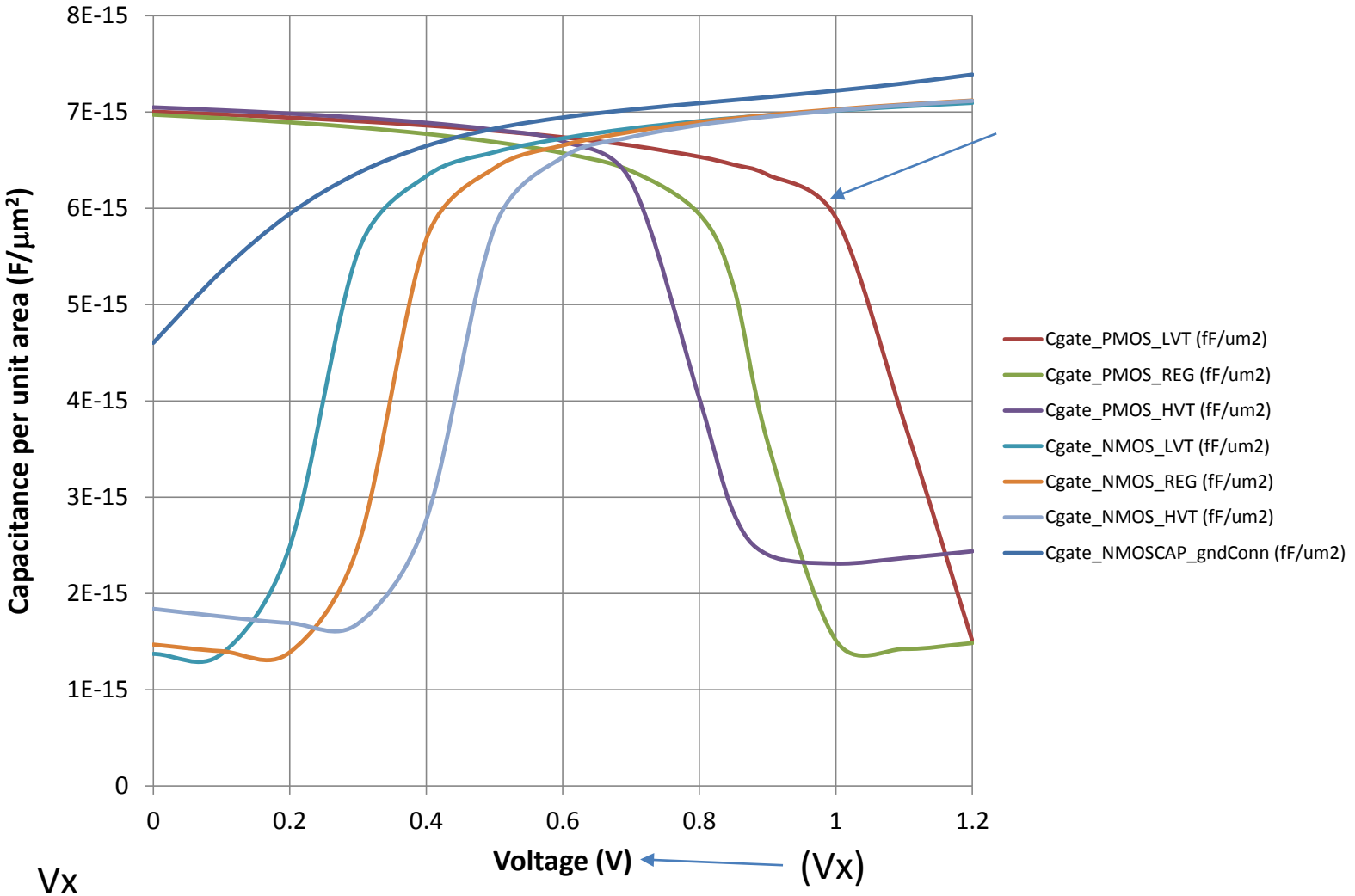
The front-end circuit

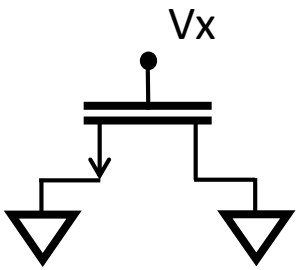


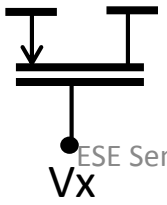

vdda
vdda
vdda
vdda
C_{leak}=700fF
V_{Bias_Ikhalf}
x2
Segmented in 4 in the direction of the length
C_{fb}=5fF
vdda
Bias block shared between 2 adjacent pixels
I_{leak}
V_{IN}
-A
V_{OUT}
vssa
Vfbk
ELT
ELT
Vfbk
ELT
-HV
V_x
Vbias_Ikrum
ELT
ELT
ELT
Dummy (matching and decoupling)
The inner terminals of the ELTs are connected to Vx (to minimize Cdb (current source) and Csb (input pair)
vssa_ik
vssa_ik
vssa_ik


vdda
1.2V
vdda
C_leak=700fF
vdda
V_Bias_Ikhalf
C_fb=5fF
vdda
-A
I_leak
V_IN
V_OUT
vssa
Vfbk
(500mV)
HVT_ELT
HVT_ELT
V_x
25nA
ELT
Vbias_Ikrum
ELT
vssa_ik
vssa_ik
vdda
vdda
830nA
2x830nA
Vbias_preamp
x1
x2
Vbias_preamp_casc
x1
x2
V_OUT
Vin_casc
REG_ELT
V_IN
HVT_ELT
2.5μA
vssa

The choice on the capacitance for C_{LEAK}





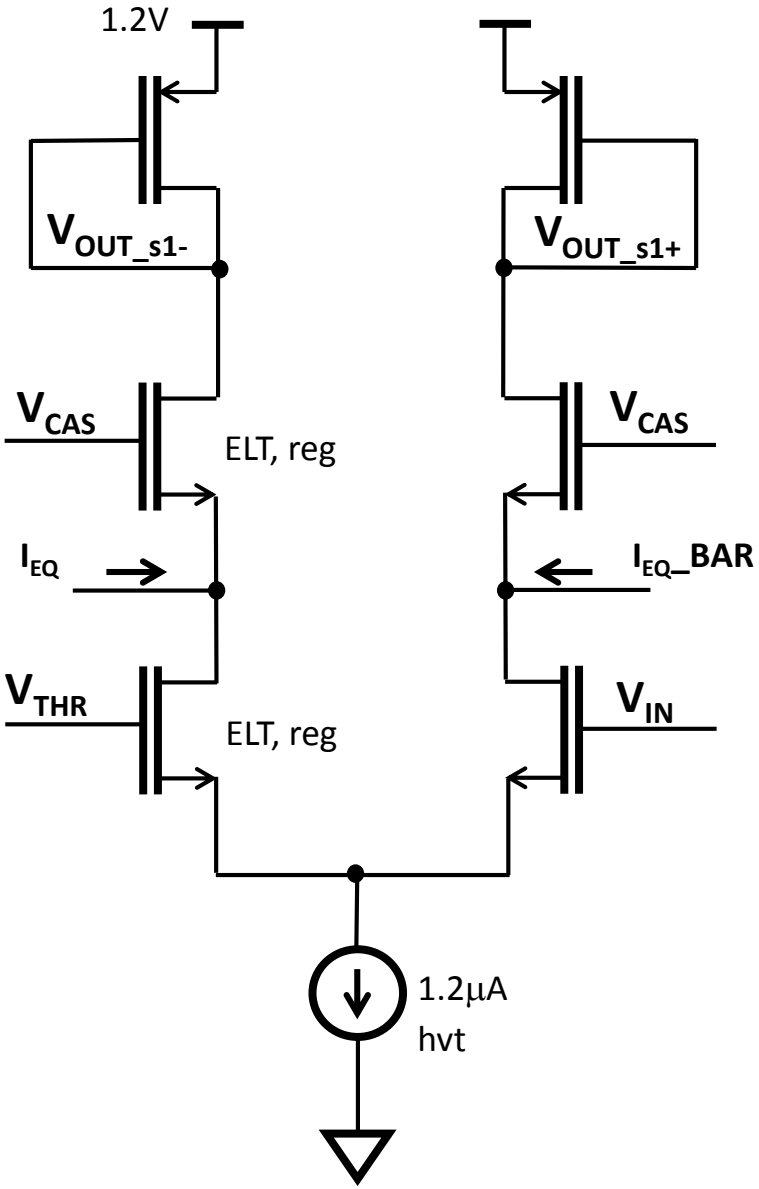


C_{LEAK} implemented as a PMOS LVT
For Power Supply Rejection Ratio
For minimization of its gate leakage current!

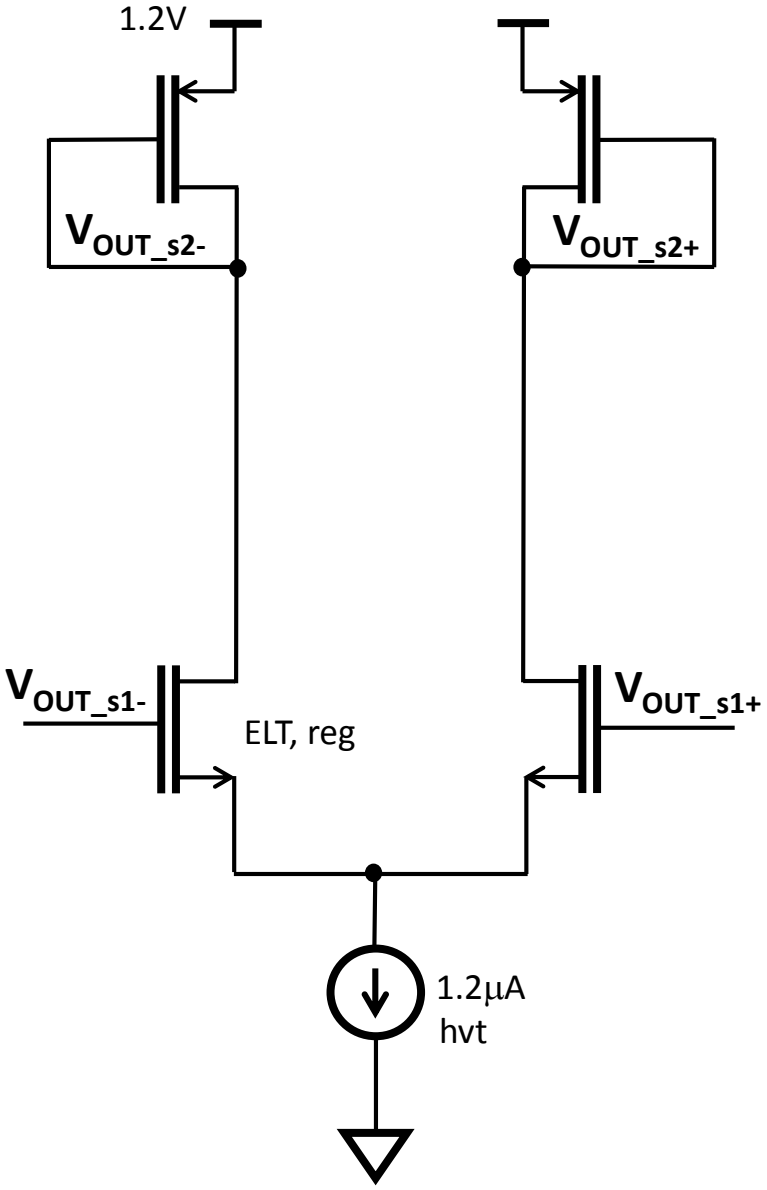
The comparator

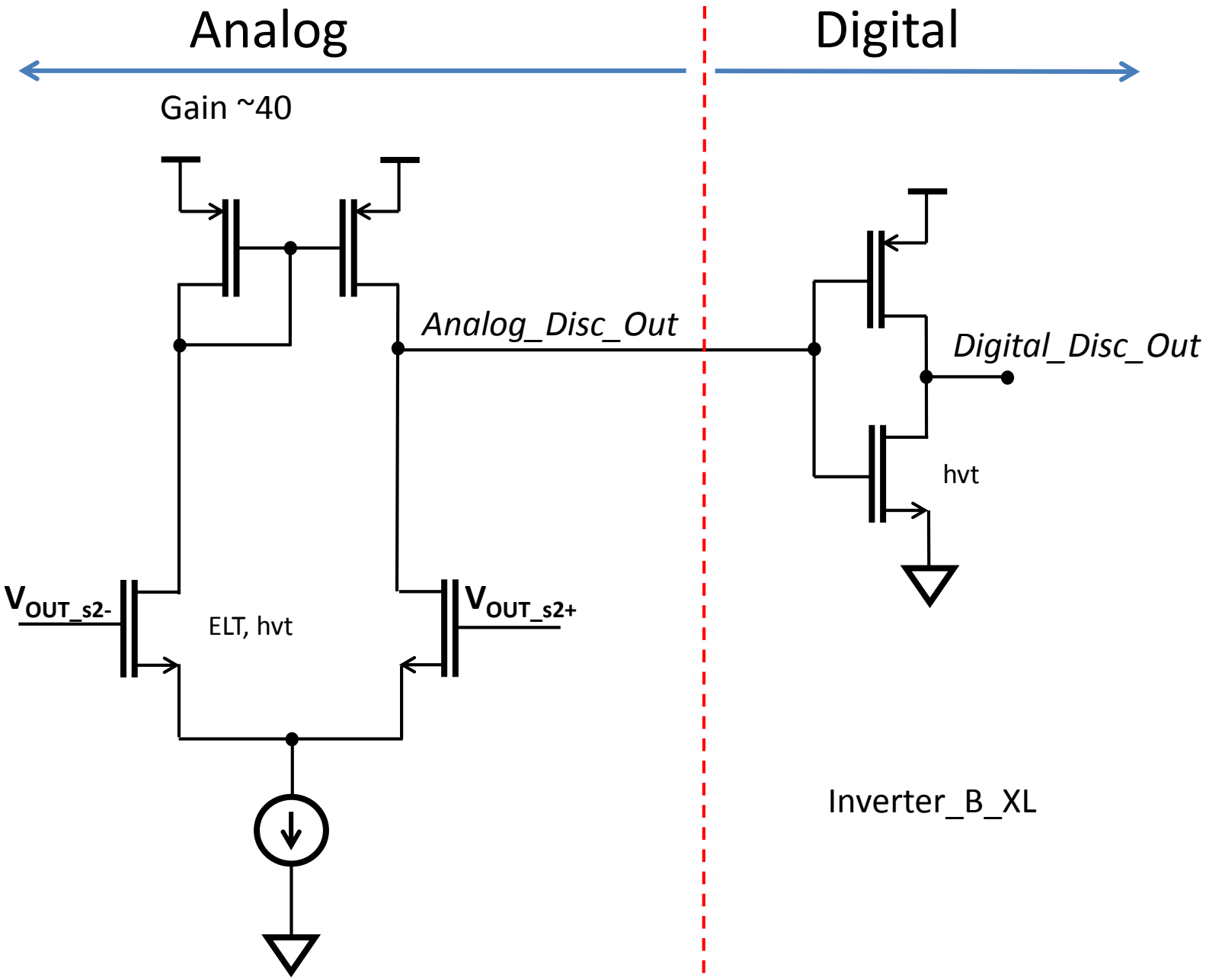
- Designed for minimizing time-walk of the system (target below 25ns)
- Designed based on cascading low gain stages was selected
- Constant current consumption in analog part

Gain ~4, BW ~40MHz

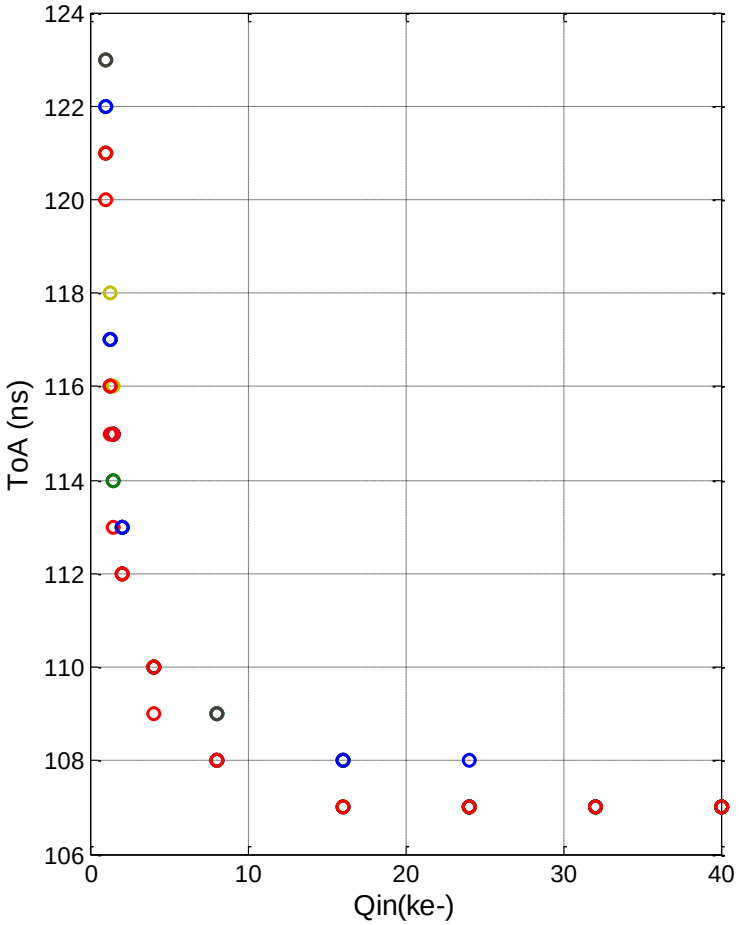


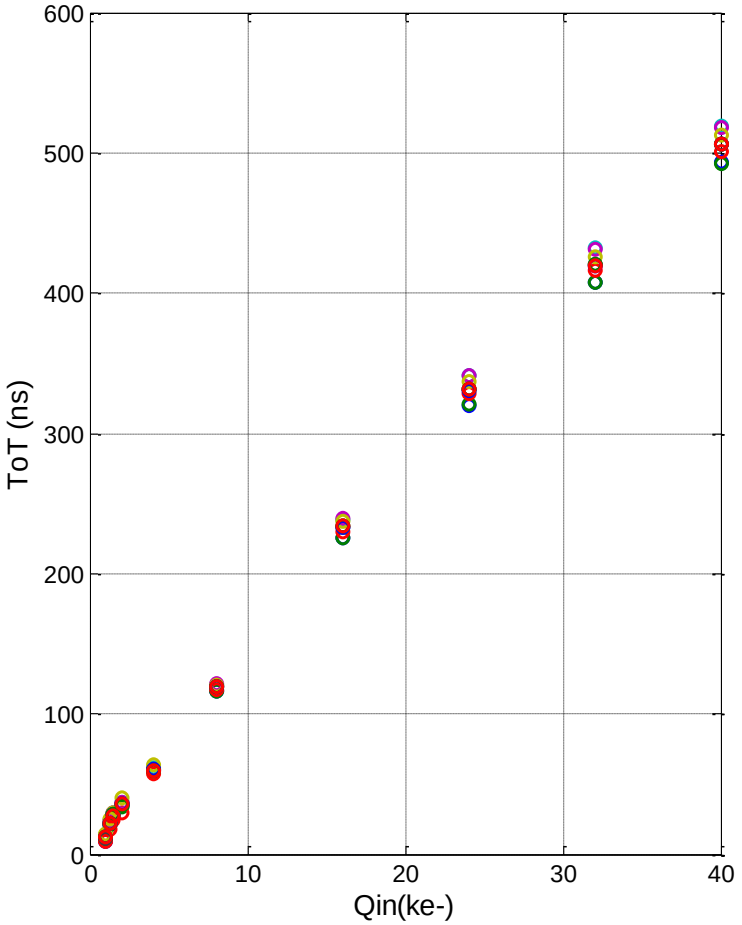
Gain ~3.2, BW ~40MHz




Analog
Digital
Gain ~40
Analog_Disc_Out
Digital_Disc_Out
hvt
V_{OUT_s2-}
ELT, hvt
V_{OUT_s2+}
Inverter_B_XL

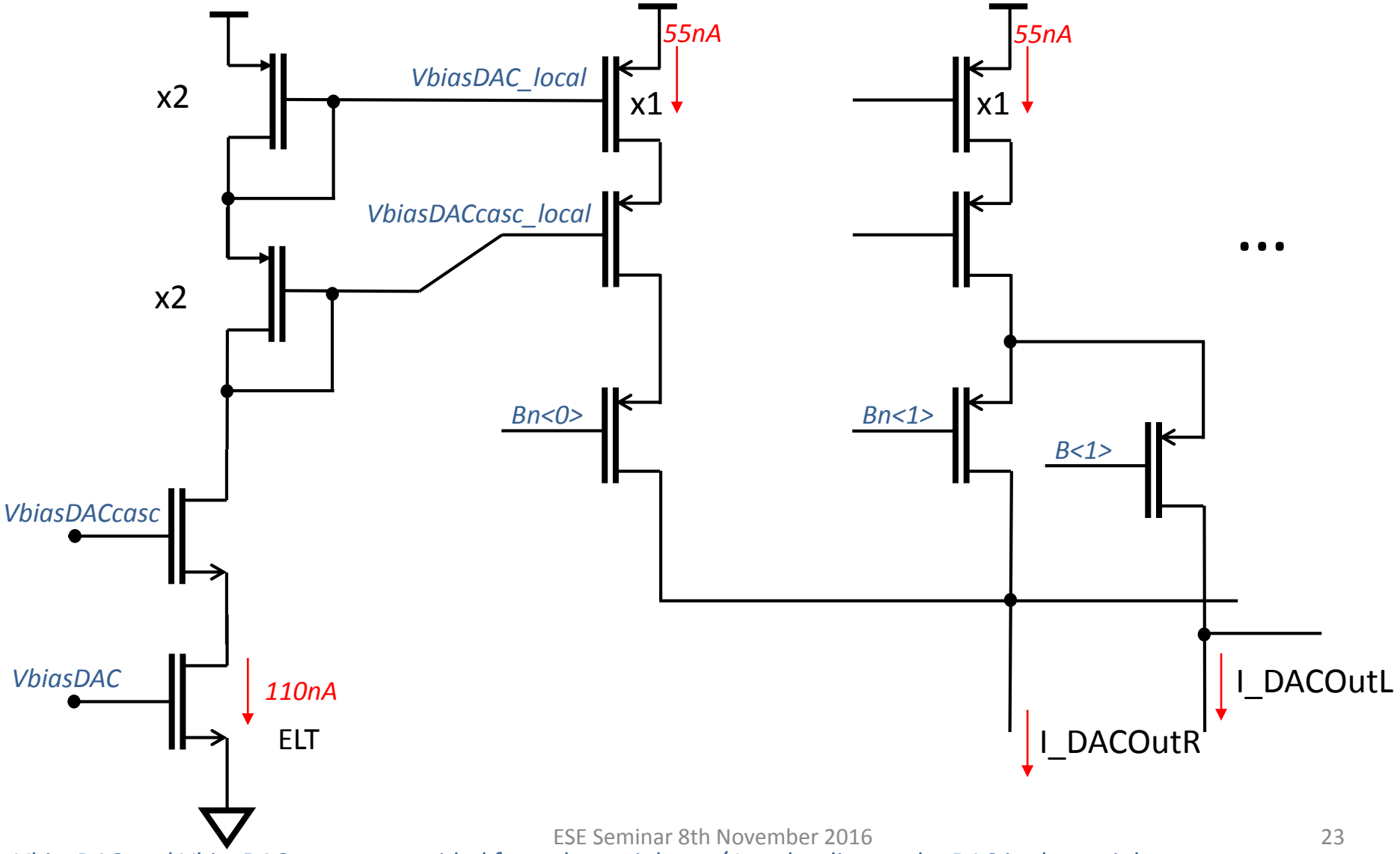
Simulation ToA, ToT



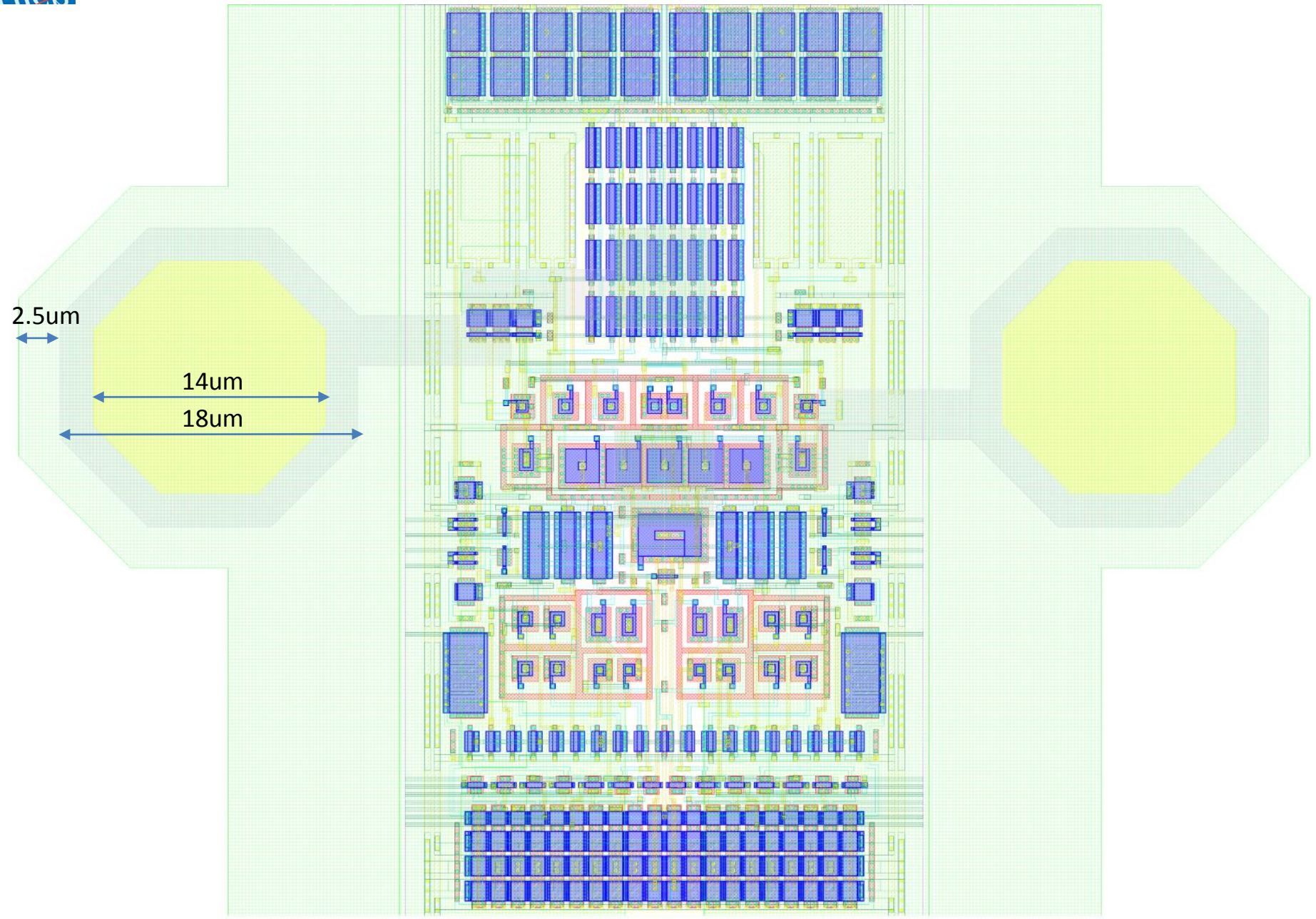


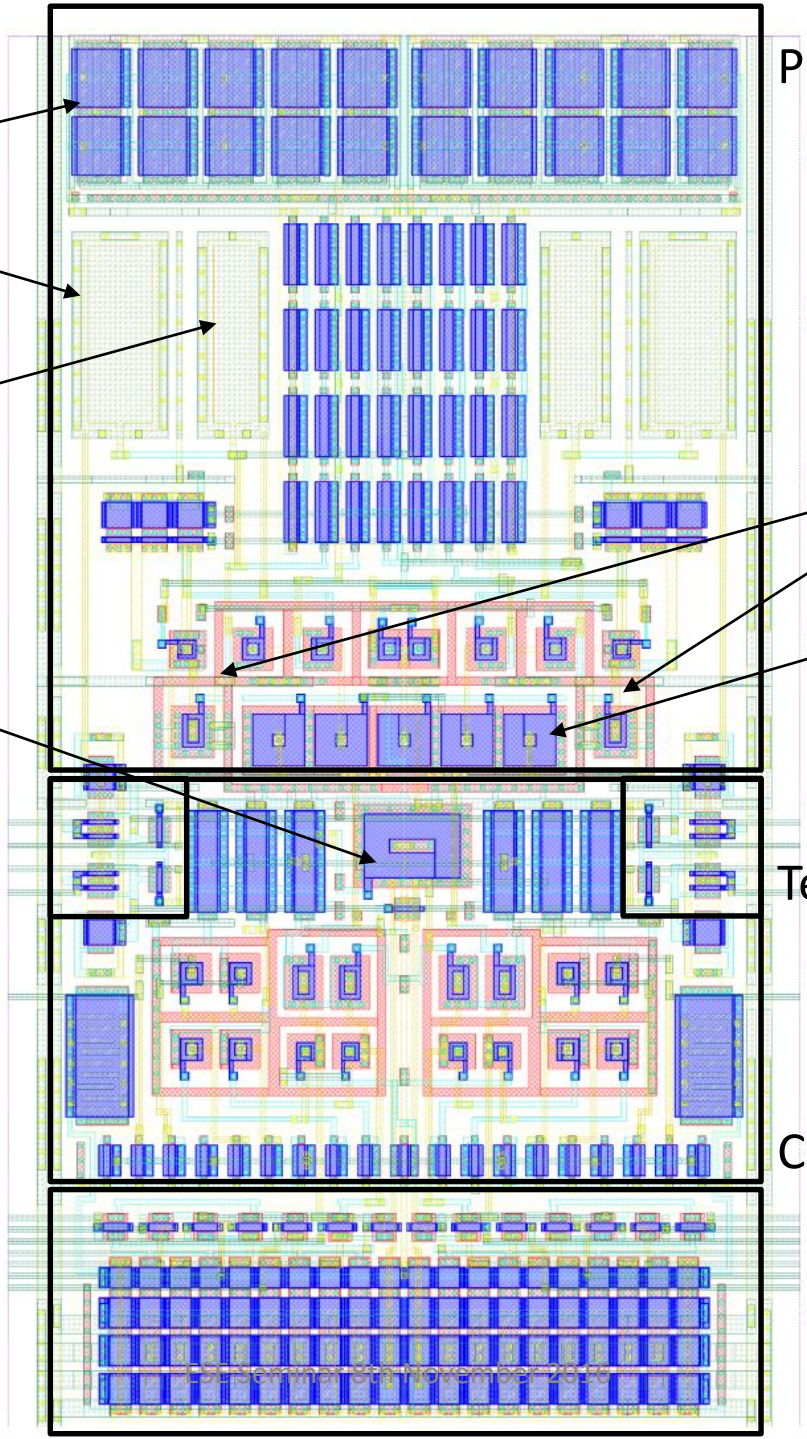
Threshold at 750e-, reference pixel (bottom column).
Corners: typ,ff,ss, radiation corners (at 100Mrad and 400Mrad)

Implementation of the DAC



VbiasDAC and VbiasDACcasc are provided from the periphery. / Less loading to the DAC in the periphery.


2.5um
14um
18um



Blocks "double pixel"

NMOS transistors on DNW

Ikrum current sources

Shielding

Most contacts are double

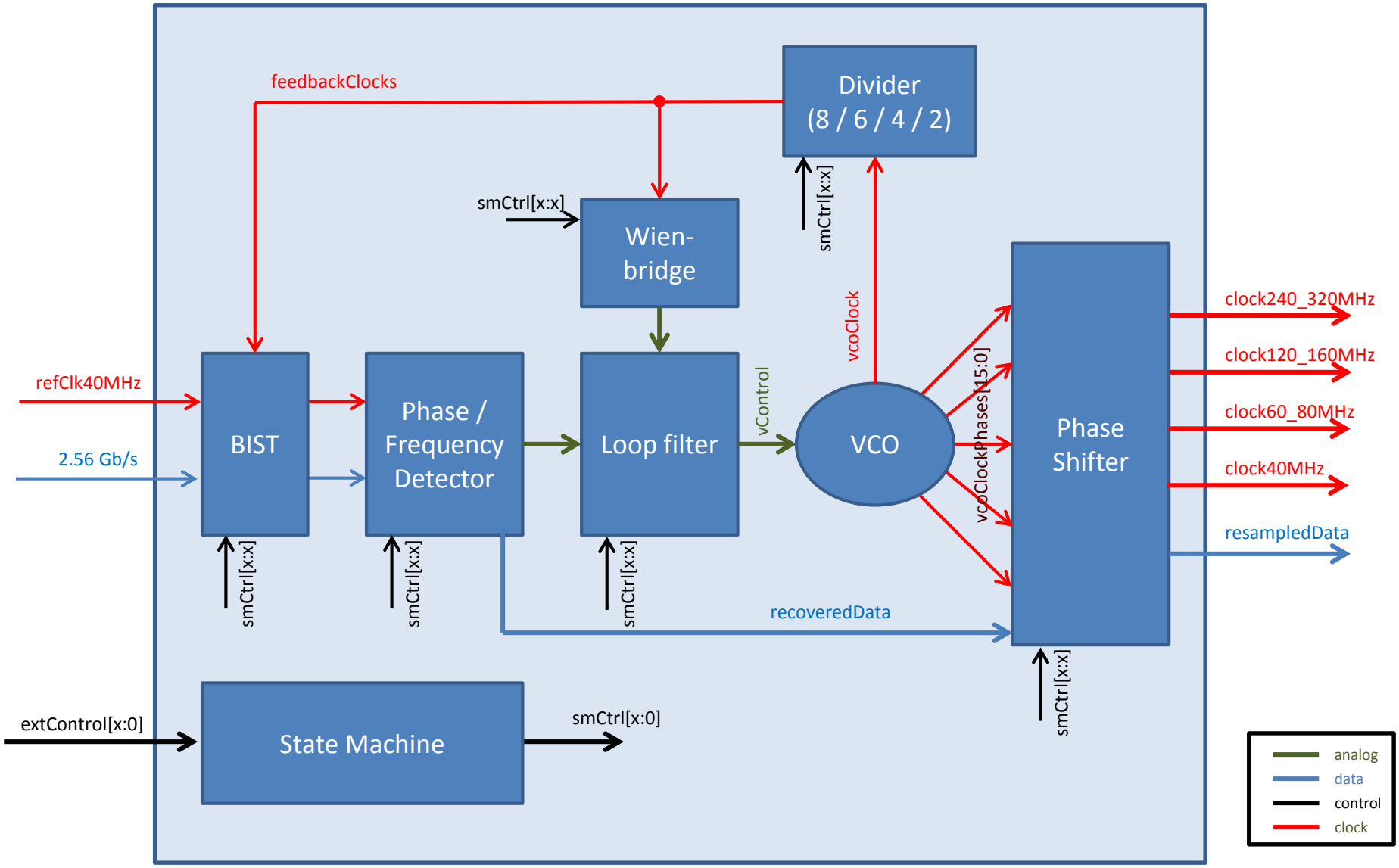
Left/right most columns different schematic and layout

Dimensions 29um x 55um

X. LLOPART

P. Leitao

eCDRPLL (simplified) Block Diagram



P. Leitao

ePLLCDR Description

- Radiation-hard and phase deterministic PLL & CDR
  - TSMC 130nm, 960 x 420 µm
- Two Frequency Multiplier modes
  - VCO@240MHz - 40, 60, 120 and 240 MHz simultaneous output clocks
    - 260-ps phase shift resolution
    - Targets GBT-FPGA/backend applications
  - VCO@320 MHz – 40, 80, 160 and 320 MHz simultaneous output clocks
    - 195-ps phase shift resolution
    - Targets typical TTC/e-link applications
  - BIST for jitter characterization (to be run at production time)
- Clock and Data Recovery
  - VCO@320 MHz only
    - 40, 80, 160 and 320 MHz simultaneous output clocks
    - 40, 80, 160 and 320 Mbps selectable output recovered data
    - Uses reference-less wien-bridge VCO calibration (no external clock required)
    - 195-ps phase shift resolution (data pushed-out on clock's falling edge)

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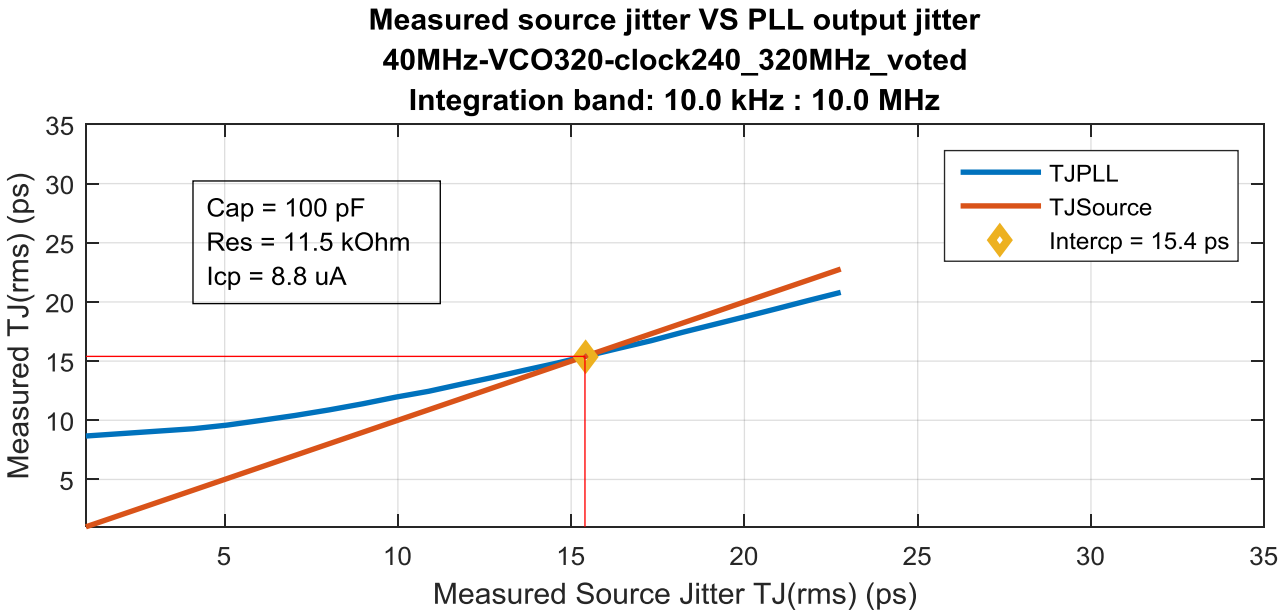
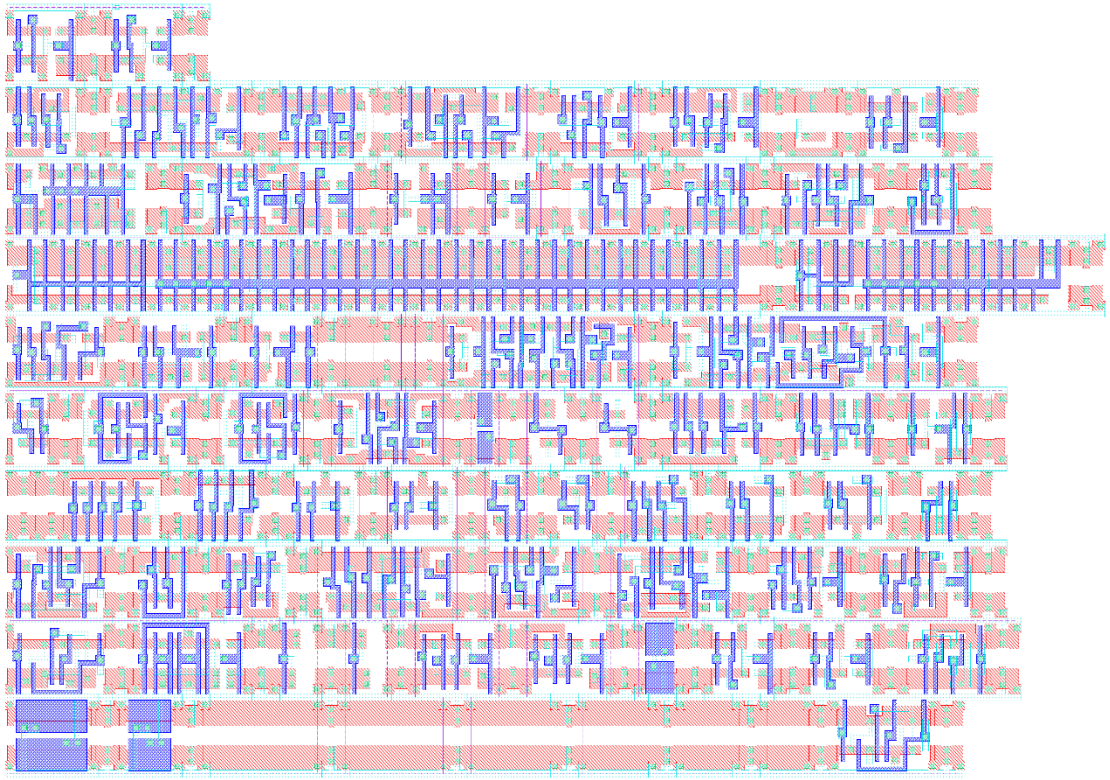
ePLLCDR preliminary experimental data



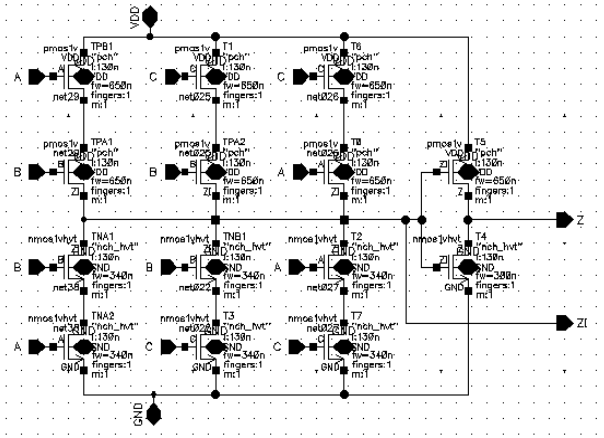
- Jitter measured using the phase noise (Agilent E5052B)
  - Input Clock:
    - 40 MHz (Agilent 81133A)
  - Output Clock:
    - 320 MHz
    - PLL w/ Default parameters
- Phase Shifter
  - INL and DNL < 0.5 LSB
- PLL full characterization on going
- CDR and BIST are still being characterized

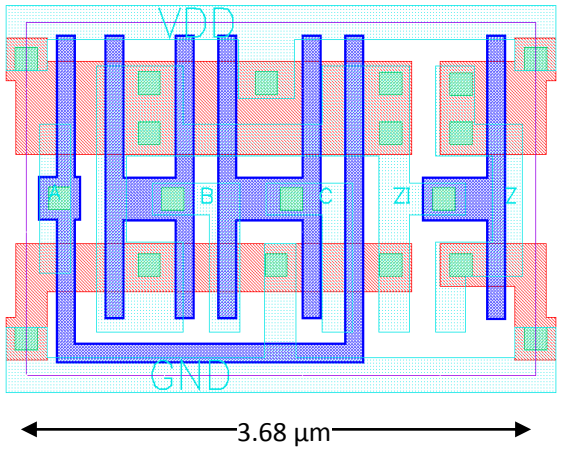
CERN TSMC 130nm HD Library

Library type	Tap-less CMOS standard cell library
Transistors	Pmos+NmosHVT
Antenna cell	1
WellSubTap cell	1
Filler cells	8
DeCap cells	5 (thin gate) 4 (thin gate + diode) 4 (thick gate)
Sequential cells	2
ClockGate cells	1
ClockBuffer cells	3
Combinatorial cells	54
Total cells	83
Technology	TSMC 130nm 1p7m4x1z1u
Metals used	M1 to M2
Corners [prerad, 100M and 400MRad]	1.2 25C TT 1.1 80C SS 1.3 -20C FF



VOTERI_B_XL_TSMC_HVTN





VOTERI3_B_XL_TSMC_HVTN

test Cell Library: Process , Voltage 1.20, Temp 25.00

Truth Table

INPUT			OUTPUT	
A	B	C	Z	ZI
0	0	x	0	1
0	1	0	0	1
x	1	1	1	0
1	0	0	0	1
1	x	1	1	0
1	1	x	1	0

Pin Capacitance Information

Cell Name	Pin Cap(pf)			Max Cap(pf)	
	A	B	C	Z	ZI
VOTERI3_B_XL_TSMC_HVTN	0.00442	0.00413	0.00402	0.10100	0.10100

Leakage Information

Cell Name	Leakage(nW)		
	Min.	Avg	Max.
VOTERI3_B_XL_TSMC_HVTN	0.00000	0.12682	0.32031

Delay Information

Delay(ns) to Z rising :

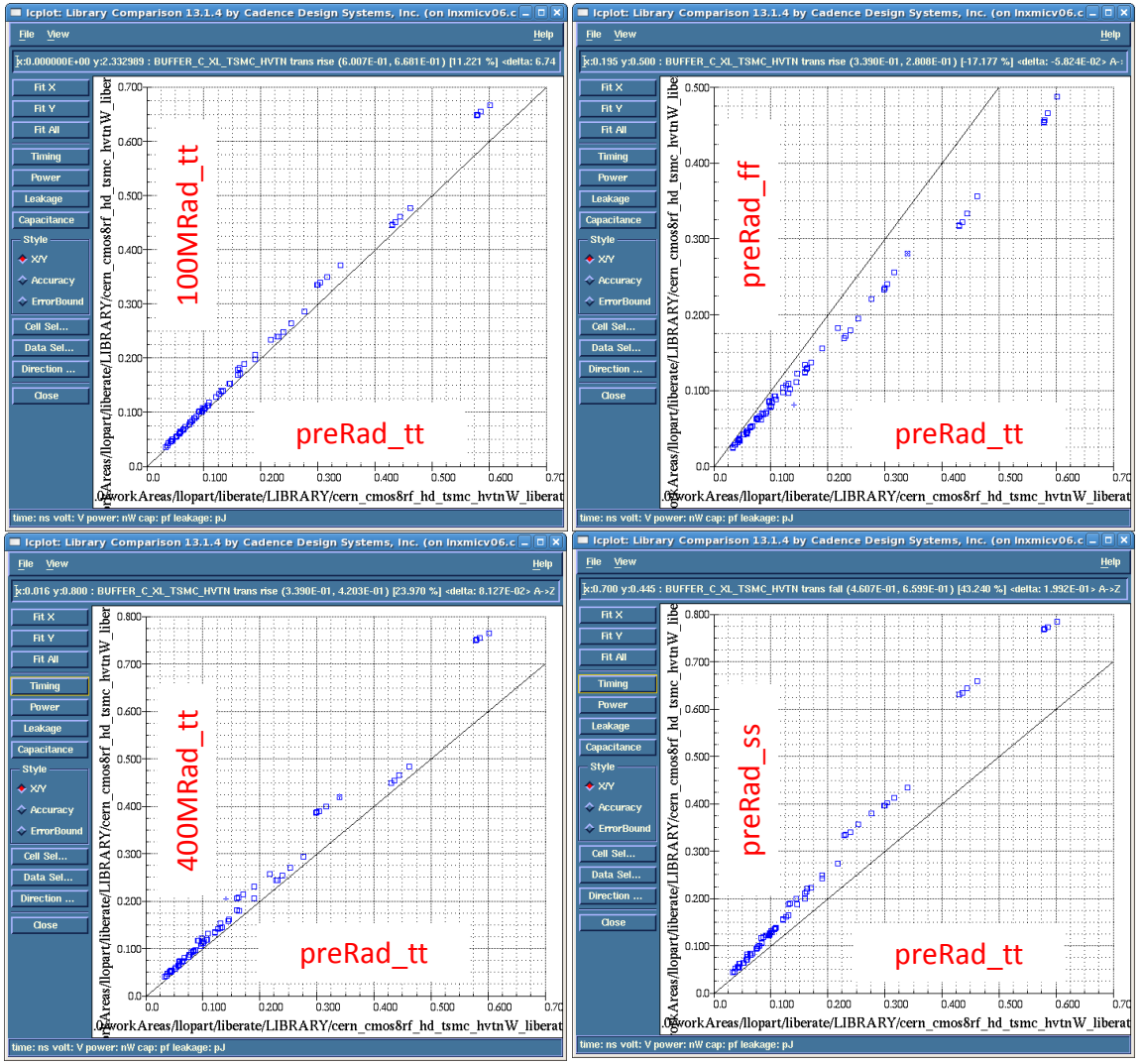
Cell Name	Timing Arc(Dir)	Delay(ns)		
		Min	Mid	Max
VOTERI3_B_XL_TSMC_HVTN	ZI->Z (FR)	0.02528	0.16214	1.29370
	A->Z (RR)	0.13665	0.38323	2.39742
	B->Z (RR)	0.11776	0.36529	2.37046
	C->Z (RR)	0.13377	0.36643	2.24325

Delay(ns) to Z falling :

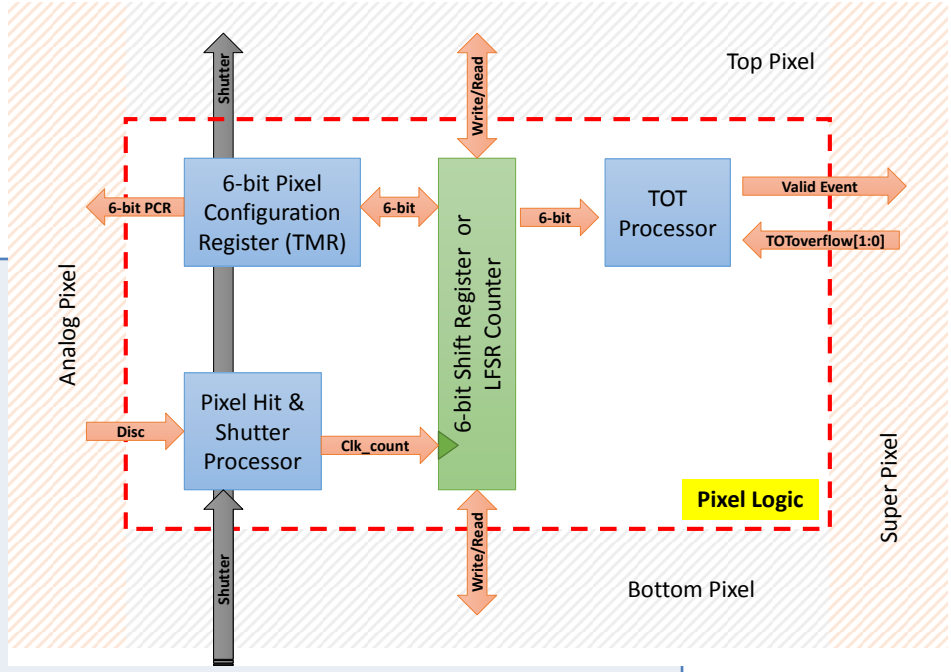
Cell Name	Timing Arc(Dir)	Delay(ns)		
		Min	Mid	Max
	ZI->Z (FF)	0.02384	0.14605	1.14841

HD Library Characterization

- Use Liberate
- 9 different corners:
  - TT 25C 1.2
    - preRad
    - 100MRad
    - 400MRad
  - SS 80C 1.1
    - preRad
    - 100MRad
    - 400MRad
  - FF -20C 1.3
    - preRad
    - 100MRad
    - 400MRad
- Observation:
  - 400MRad_TT → preRad_SS
- **Corners used:**
  - **SLOW: SS 80C 1.1 400MRad**
  - **TYP: TT 25C 1.2 PreRad**
  - **FAST: FF -20C 1.3 PreRad**



Velopix Pixel

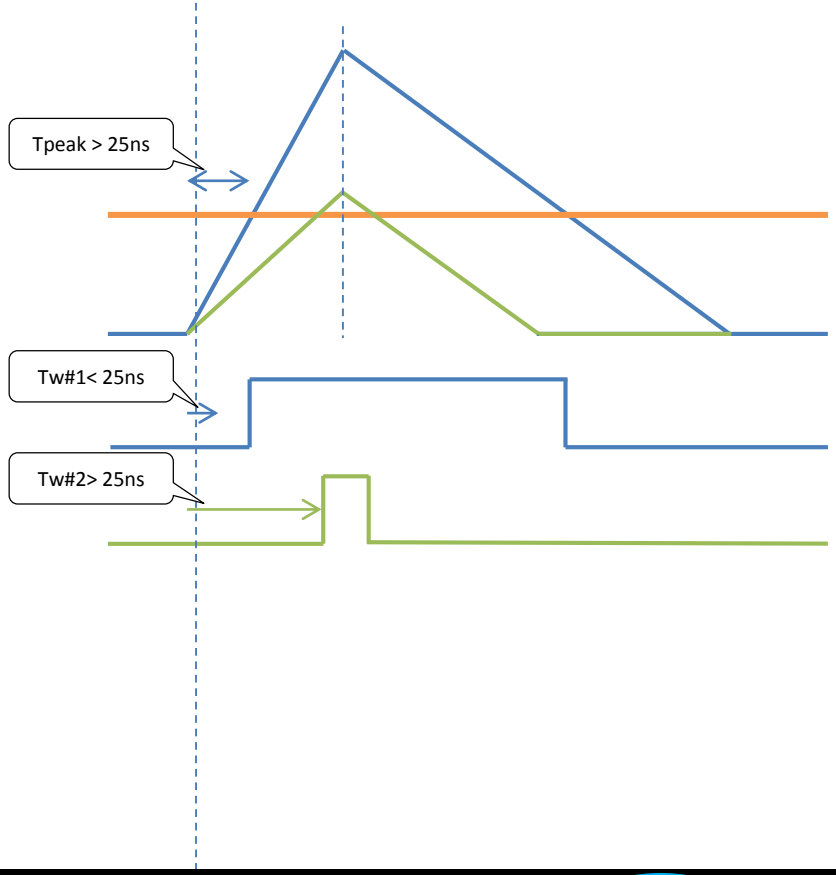


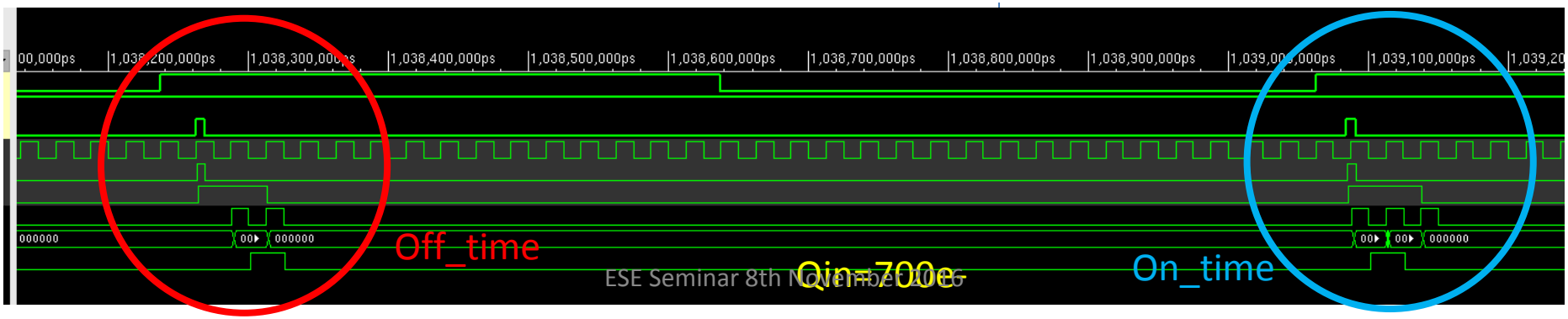
@Shutter	SelectOverflow_FullRange_TOToverflow	TOToverflow [1:0]	Select_1hitTOT_iTOT	Select_PC_TOT	@SelectDirection_Write_Read	read_seu	@Parallel Load		
0	X	XX	X	X	0	0	0	Read	Reads the 6-bit Shift Register
							1		Reads back the 6-bit PCR
						1	1		Reads the 6-bit SEU status from the PCR
					1	X	X	Write	Writes the 6-bit PCR
1	0	00	0	0	X	X	X	Data acquisition	Valid event generated if $TOT_{measured} \geq 0$
		01							Valid event generated if $TOT_{measured} \geq 1$
		10							Valid event generated if $TOT_{measured} \geq 2$
		11							Valid event generated if $TOT_{measured} \geq 3$
	1	XX	0	0				Data debug acquisition	Integrating TOT up to 63 counts
				1					Integrating PC up to 63 counts
			1	0					1-hit integrating TOT up to 63 counts
				1					1-hit integrating PC up to 63 counts

TOT Processor

- Event-by-event processor
- Very useful to correctly set a hit in BxID
- Events below TOT threshold are ignored
- Most noise events can also be filtered

TOT threshold	TOT clocks	Fix delay to valid event
00	0	50ns
01	1	75ns
10	2	100ns
11	3	125ns

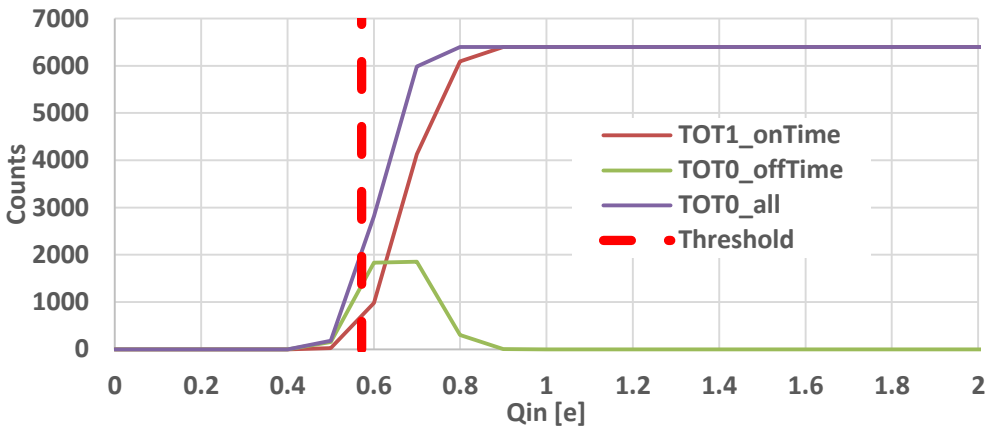


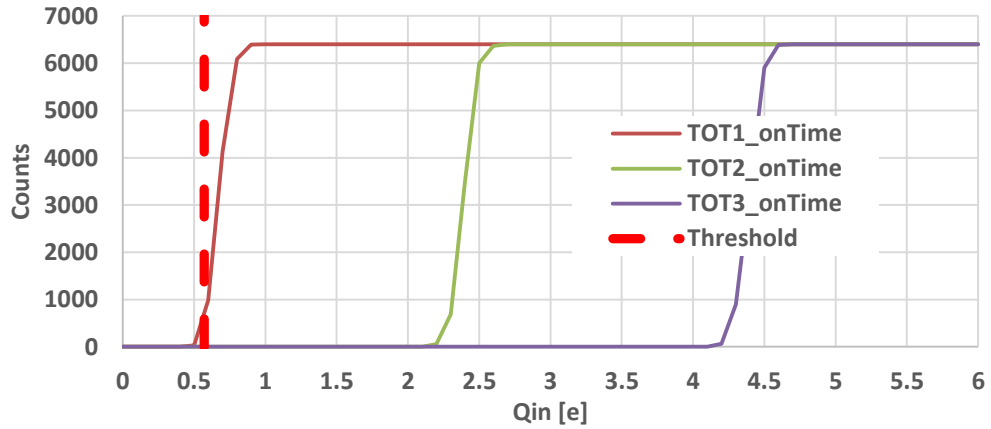


Simulation of TOT processor

Peak Time	25ns
Return to zero	12.5ns/Ke$^-$
ENC	60e$^-_{rms}$
Threshold mismatch	30e$^-_{rms}$
Gain	35e$^-$/mV
Analog Threshold	~570e$^-$
Pixels tested	64
TestPulses per Qin/pixel	100

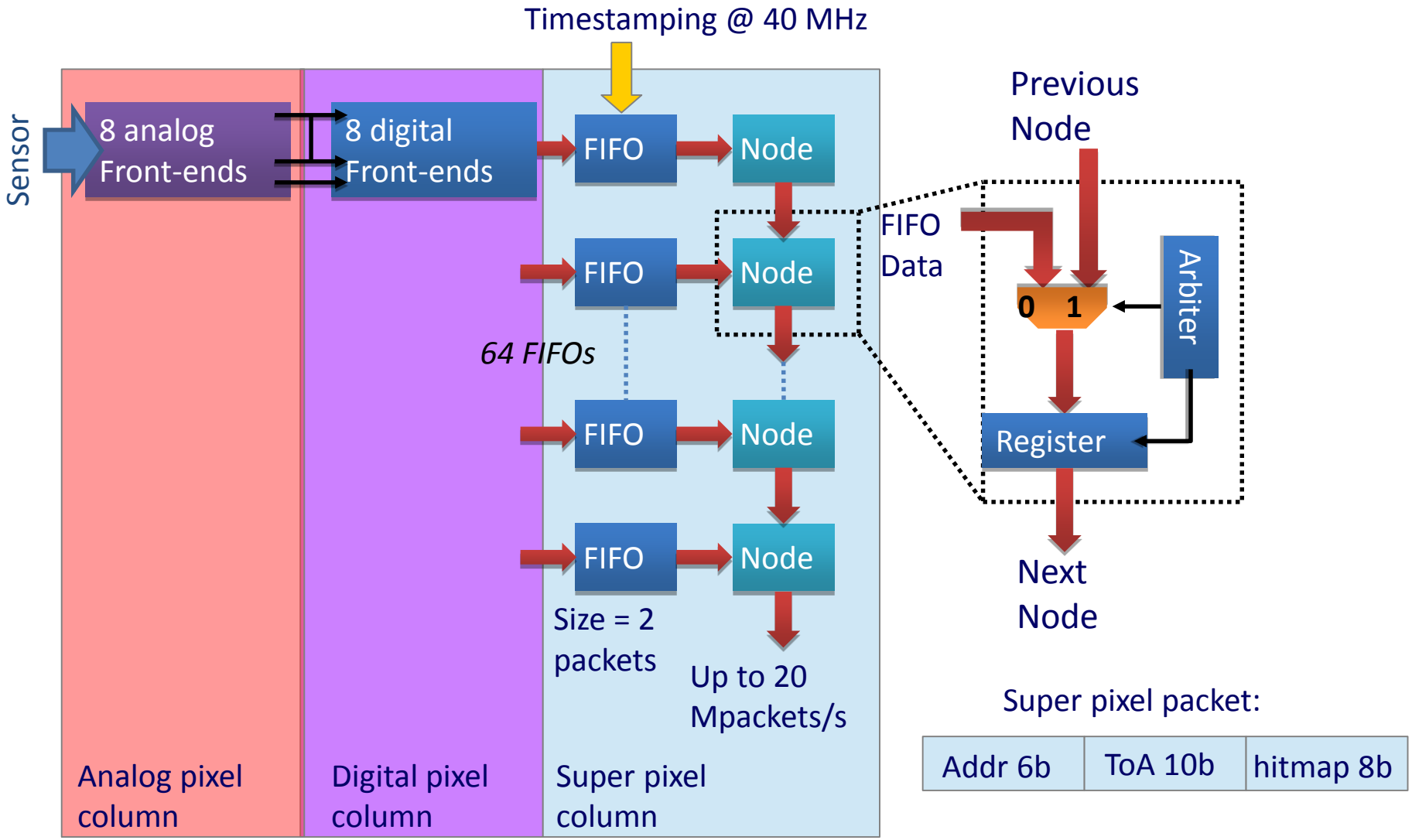
Best setting: TOT=01 → 100% Qindetected ≥ 1.0 Ke$^-$



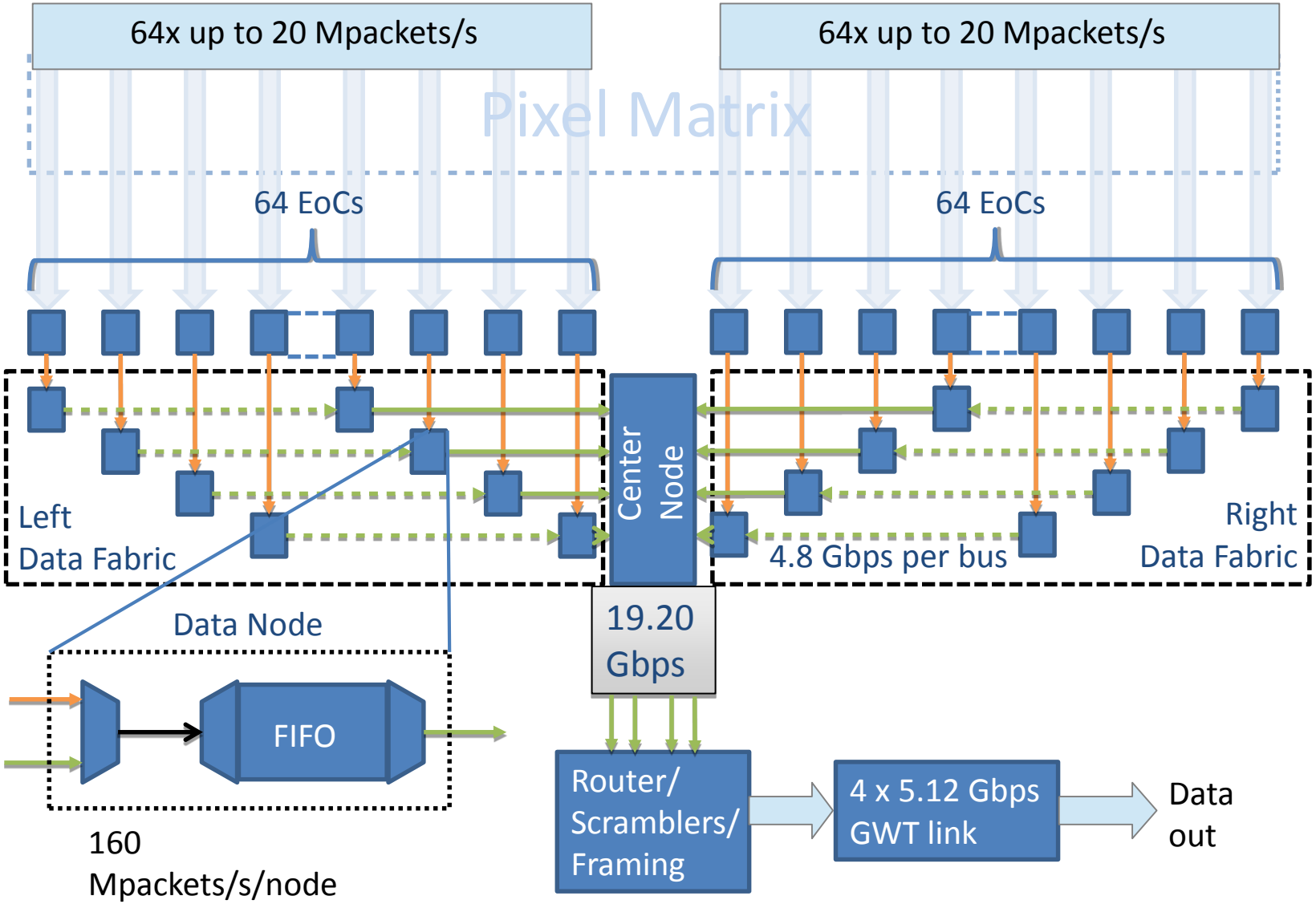


T. POIKELA

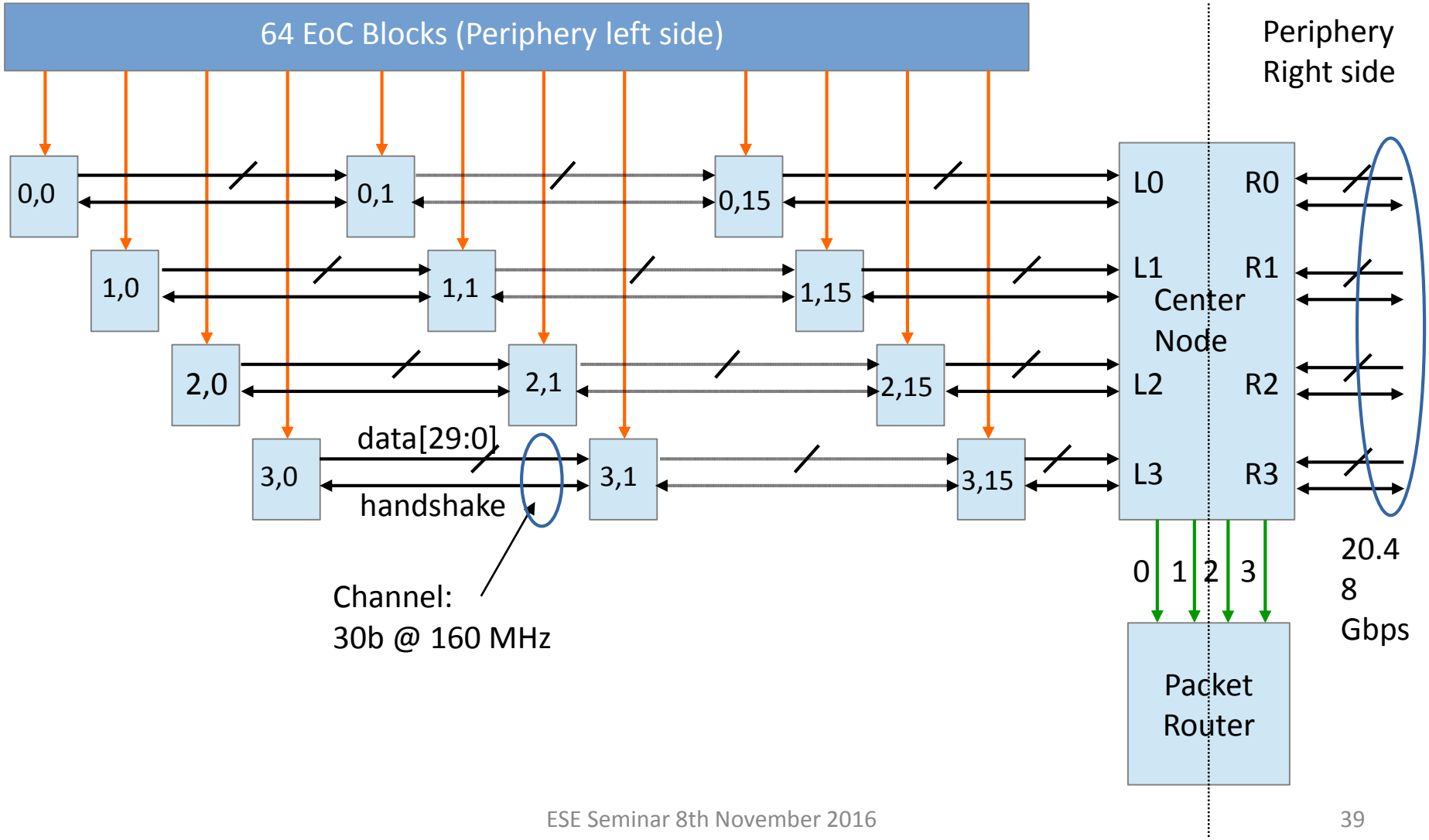
Double column datapath



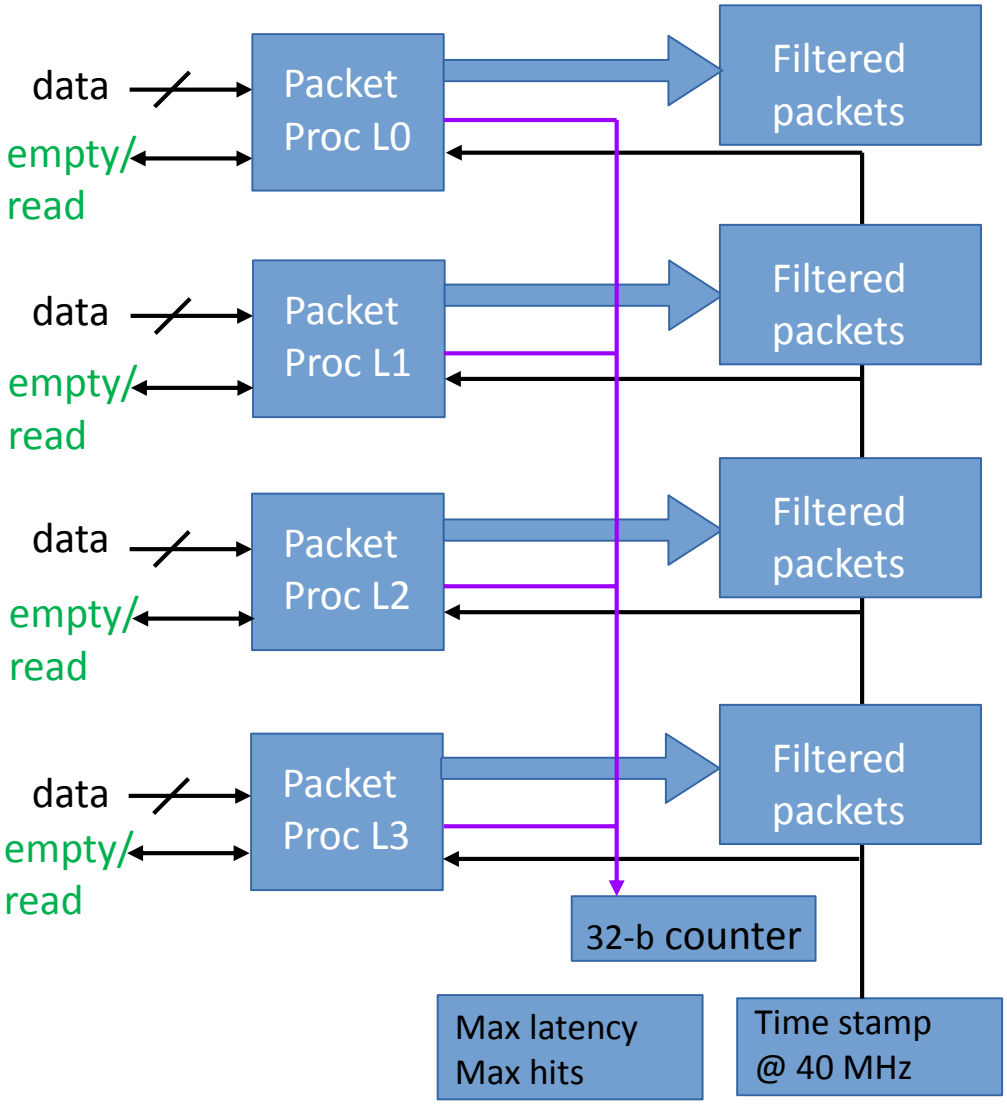
Periphery datapath



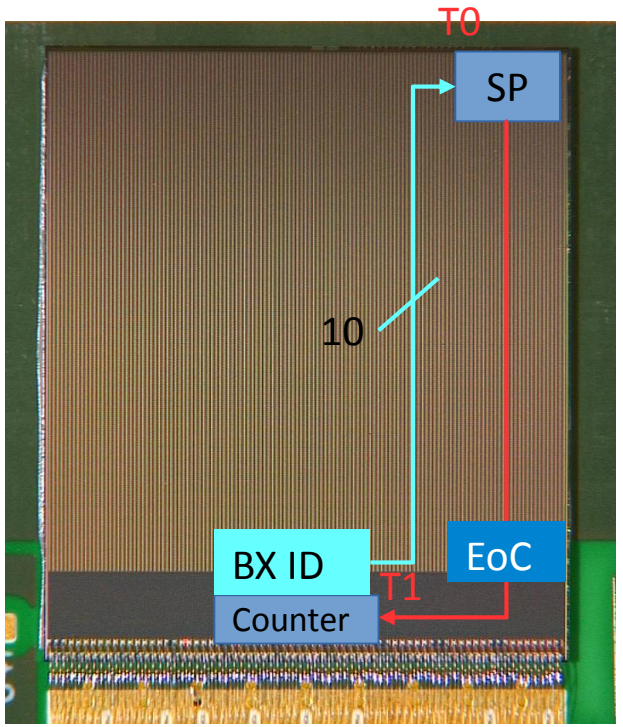
EoC Data Fabric



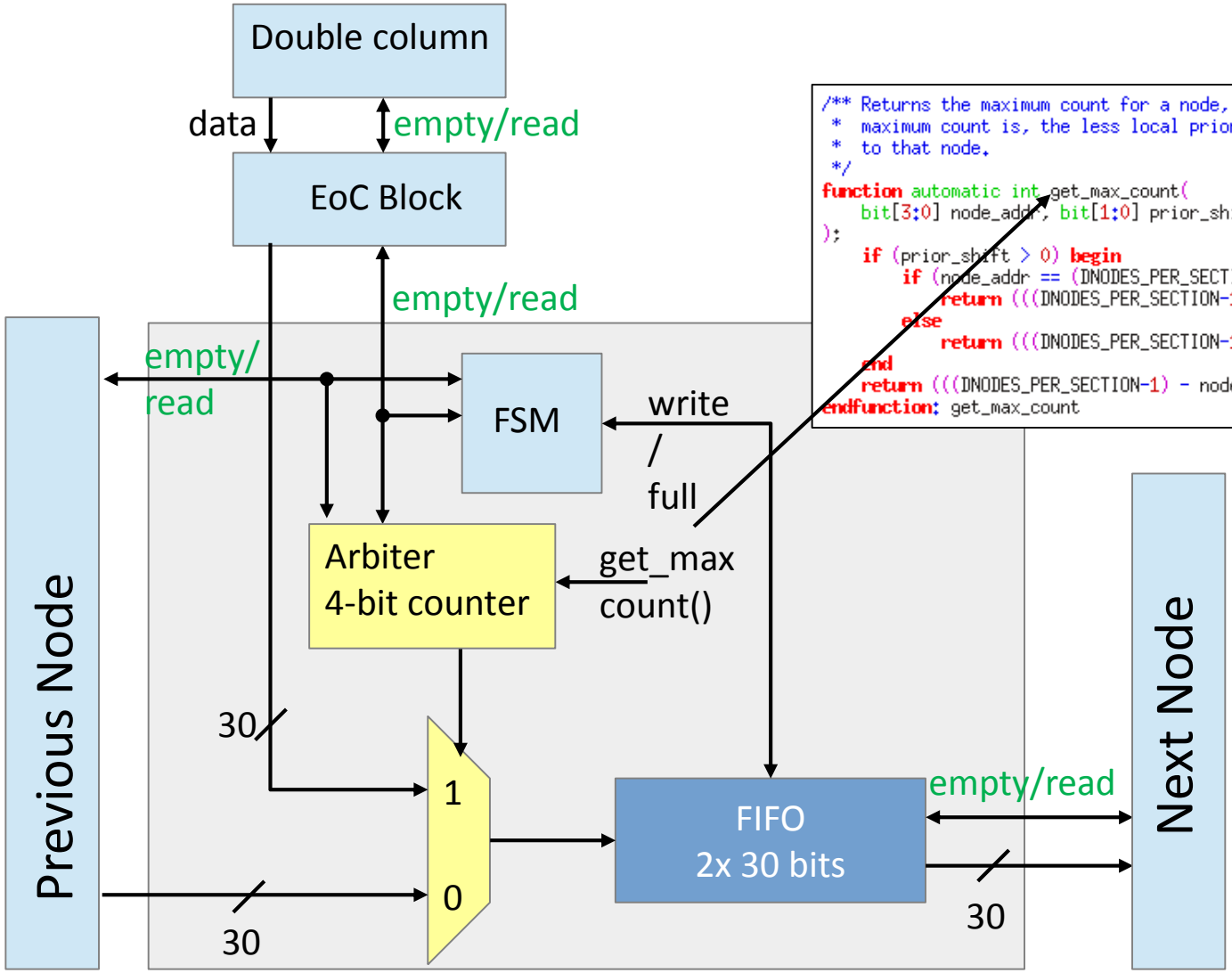
Packet processors (Center node)



Latency: T1 - T0

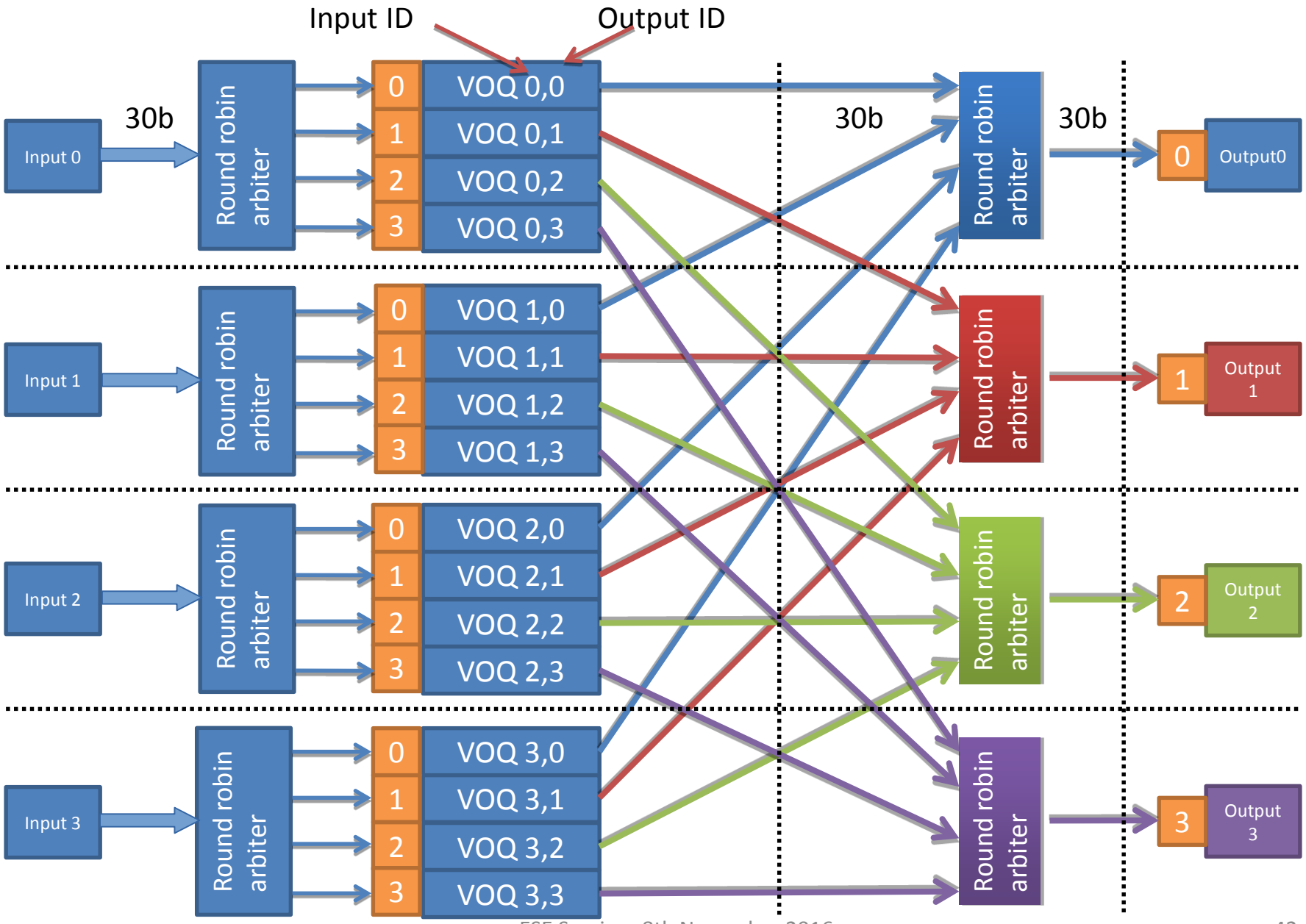


EoC Data Fabric Node

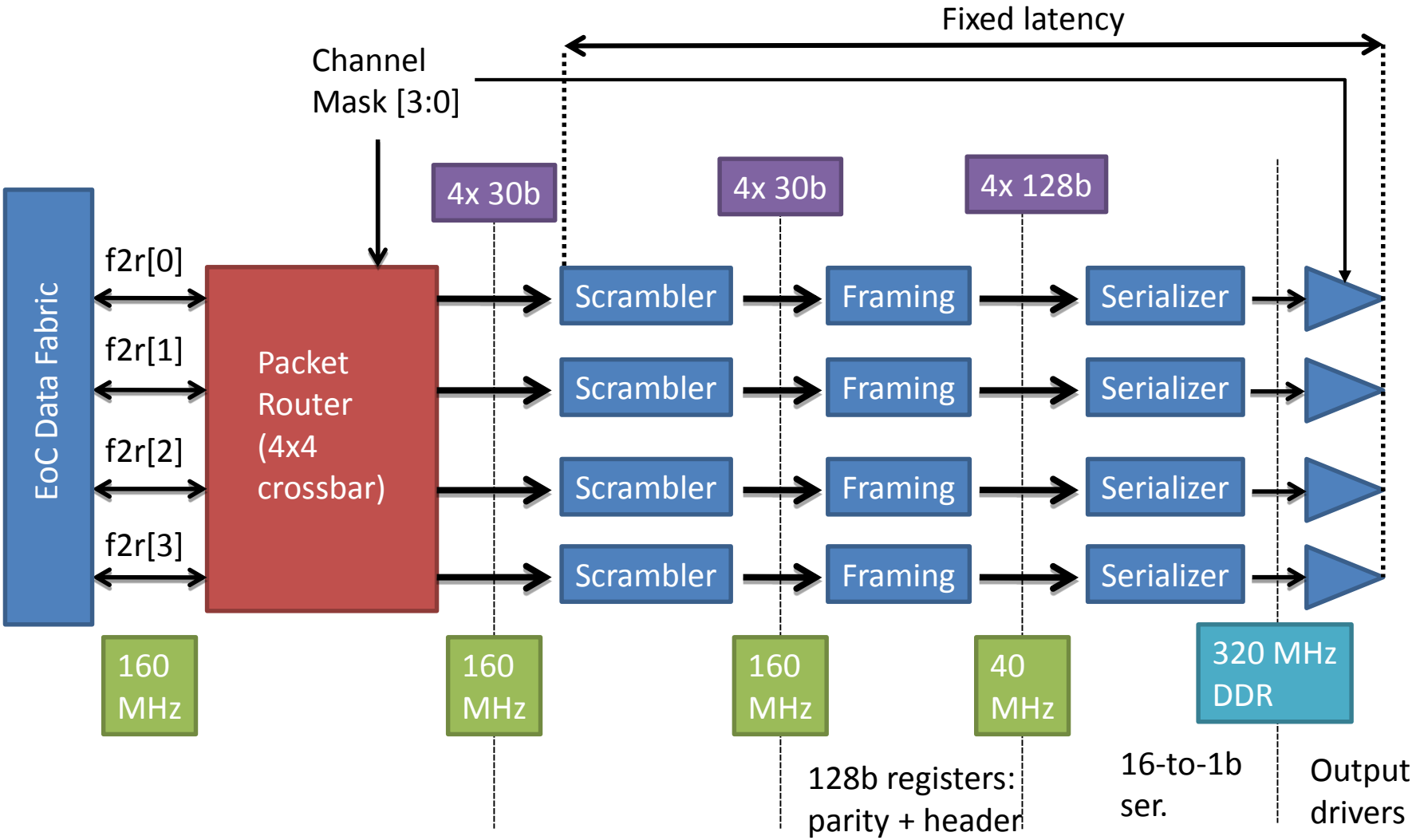



```
/** Returns the maximum count for a node, based on its address. The higher the
 *  maximum count is, the less local priority is assigned to EoC block connected
 *  to that node.
 */
function automatic int get_max_count(
    bit[3:0] node_addr, bit[1:0] prior_shift
);
    if (prior_shift > 0) begin
        if (node_addr == (DNODES_PER_SECTION-2))
            return (((DNODES_PER_SECTION-1) - node_addr) >> prior_shift) + 1;
        else
            return (((DNODES_PER_SECTION-1) - node_addr) >> prior_shift);
    end
    return (((DNODES_PER_SECTION-1) - node_addr) >> prior_shift);
endfunction: get_max_count
```

Packet Router

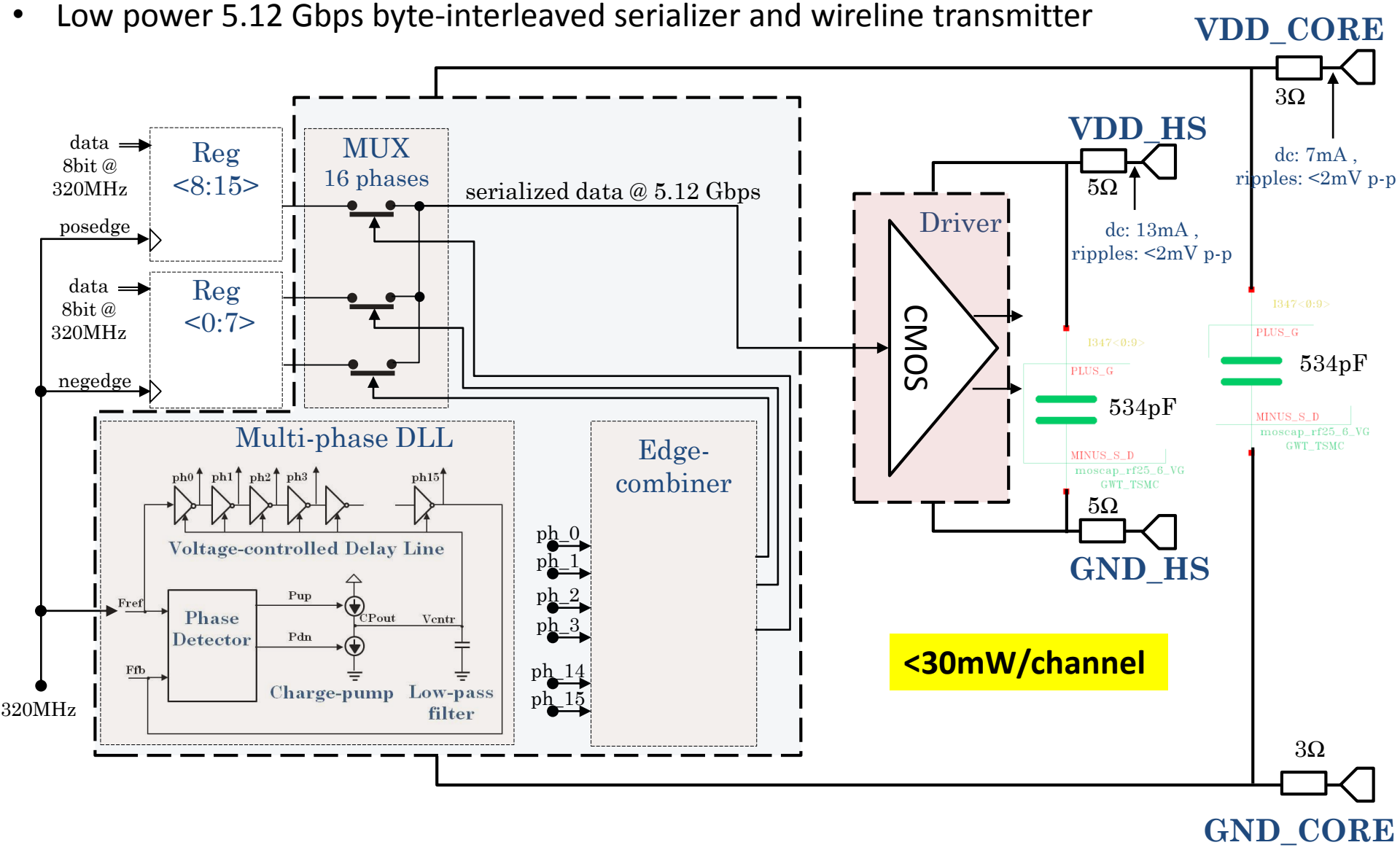


Router and output block

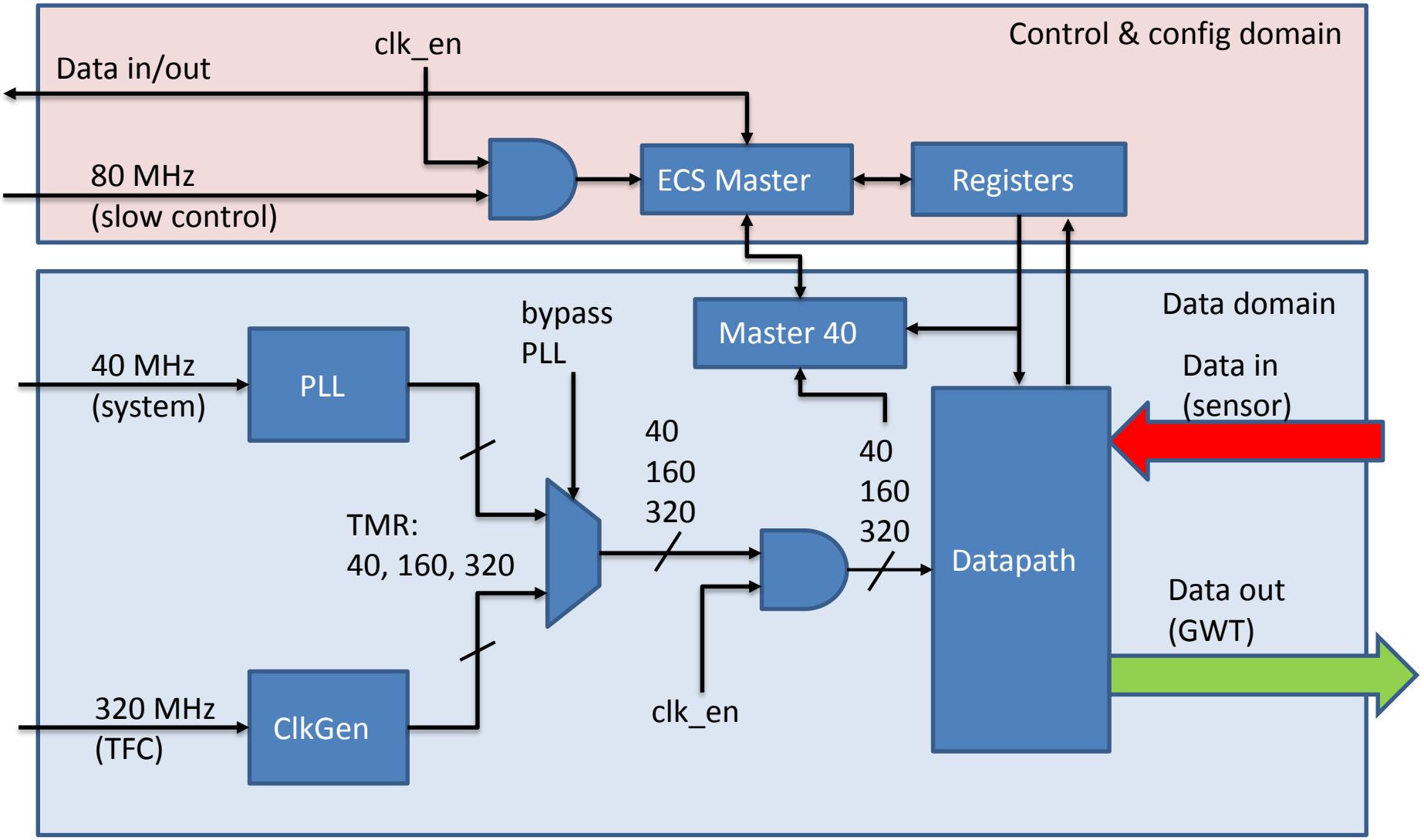


GWT (NIKHEF)

- Low power 5.12 Gbps byte-interleaved serializer and wireline transmitter



Clock distribution



Velopix: TMR/RadHard design

- Pixel Matrix (<400Mrad):
  - Only NMOS ELT transistors used in analog front-end
  - Full TMR in FSM & configuration FFs:
    - Pixel configuration → Asynchronous self correcting TMR latch
  - Pixel data flip-flops (FF) unprotected
  - Custom made HD Standard cell library (74 cells) with HVT NMOS HVT and regular PMOS:
    - Standard cell library characterized at 400 Mrad, High-Vt NMOS + Std PMOS

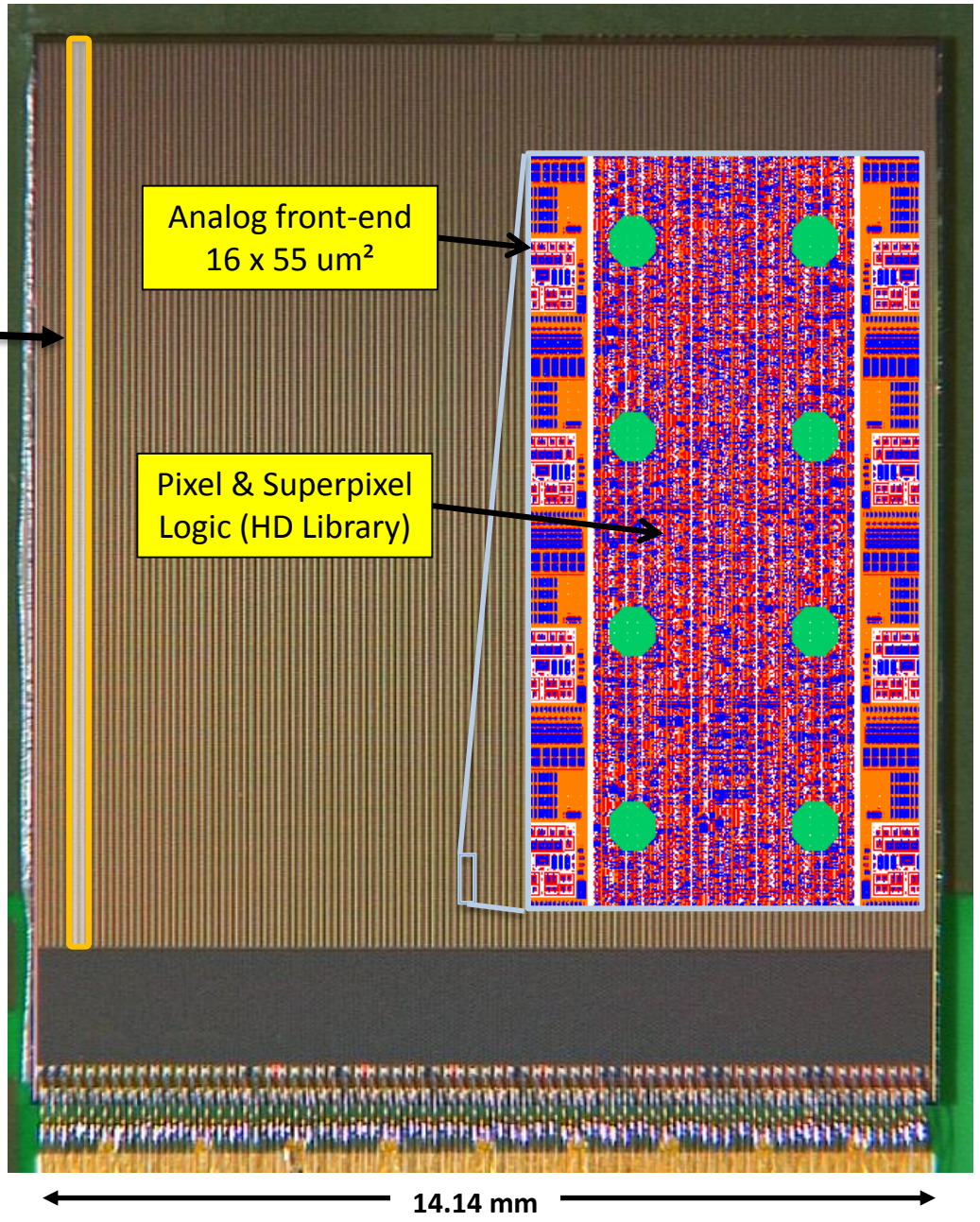
- Periphery (<50Mrad):
  - Full TMR in FSM & configuration FFs
  - Data path unprotected

VeloPix

Double column:
- 512 pixels
- 64 super pixels

Full matrix:
- 128 Double columns
- ~190 Mtransistors
- 14.8nF digital decoupling (thick gate)

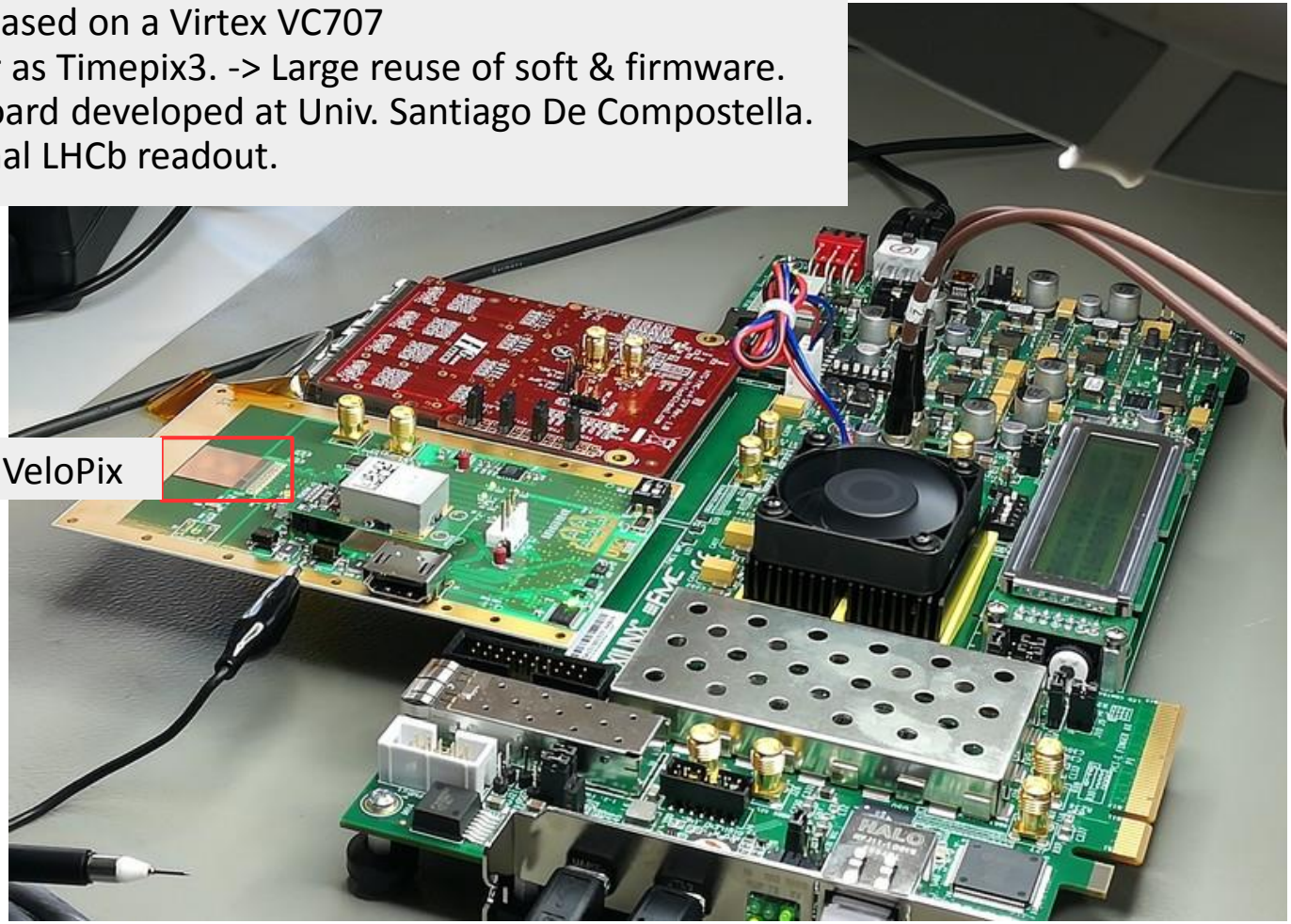
Active Periphery:
- 40, 80, 160 and 320 TMR clocks
- HVT TSMC (tcb013ghphvt library)
- 4nF digital decoupling (thin gate)



J. BUYTAERT

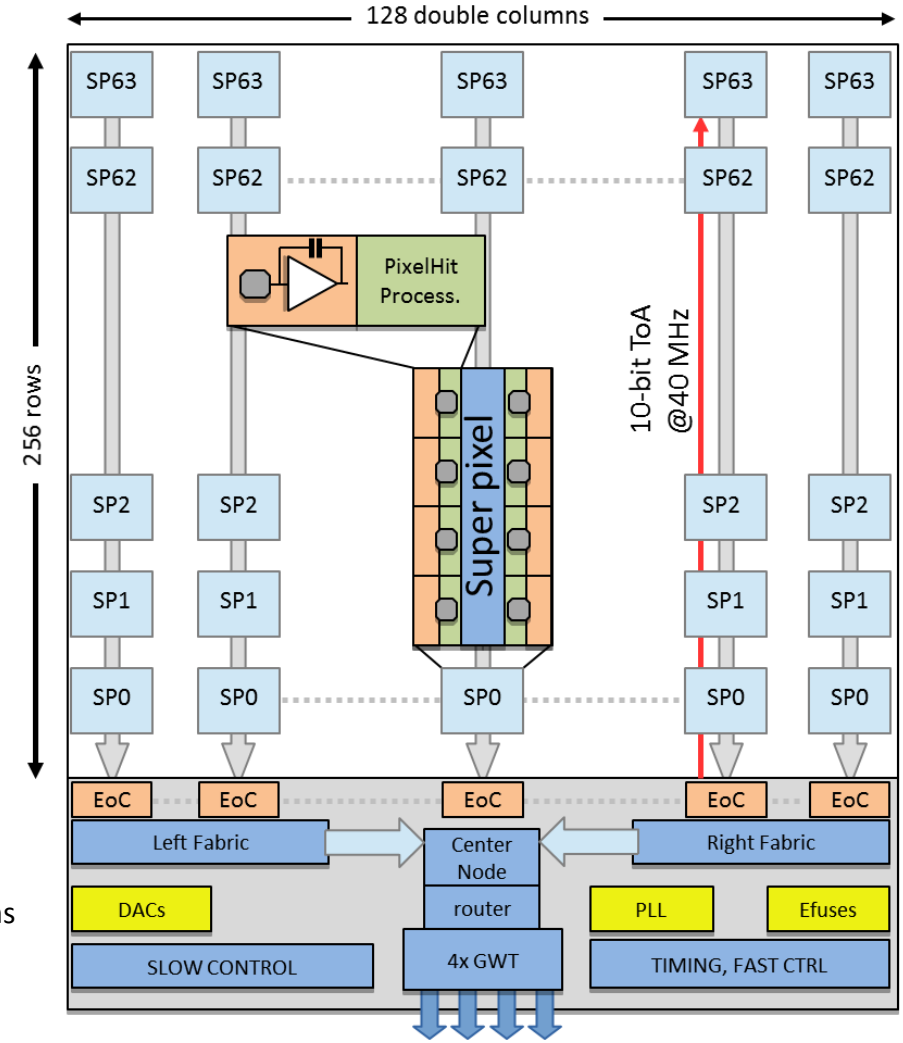
VeloPix test readout system

- SPIDR-readout system developed at NIKHEF (NL)
  - Based on a Virtex VC707
- Similar as Timepix3. -> Large reuse of soft & firmware.
- Chipboard developed at Univ. Santiago De Compostella.
- Not final LHCb readout.

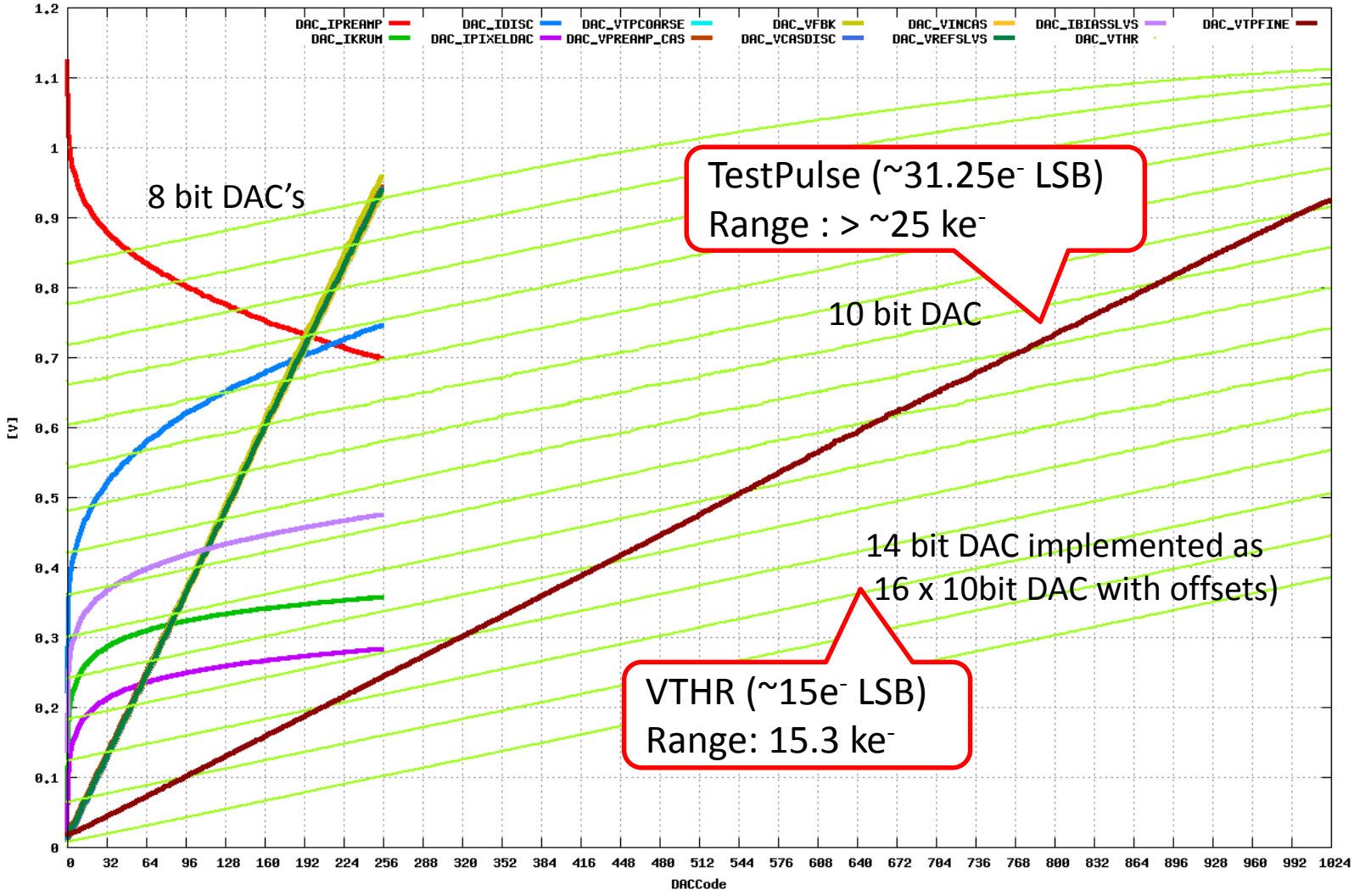


VeloPix: General Measurements

- ✓ Measured power consumption (@nominal settings):
  - ✓ Analog suuply < 480 mW
  - ✓ Digital:
    - ✓ Periphery < 380mW
    - ✓ Pixel Matrix <350mW (idle, i.e. clock distribution only)
    - ✓ @High rate ~+300mW (simulated)
  - ✓ Total= ~1.5W @High rate
- ✓ Slow and Fast control fully functional.
- ✓ Pixel matrix Configuration and readout
- ✓ On-chip biasing DACs (next slide)
- ✓ Internally measured packet latency (@low rate)
- ✓ eCDRPLL (CERN) total jitter @320MHz <6ps$_{rms}$



VeloPix on-chip biasing DACs



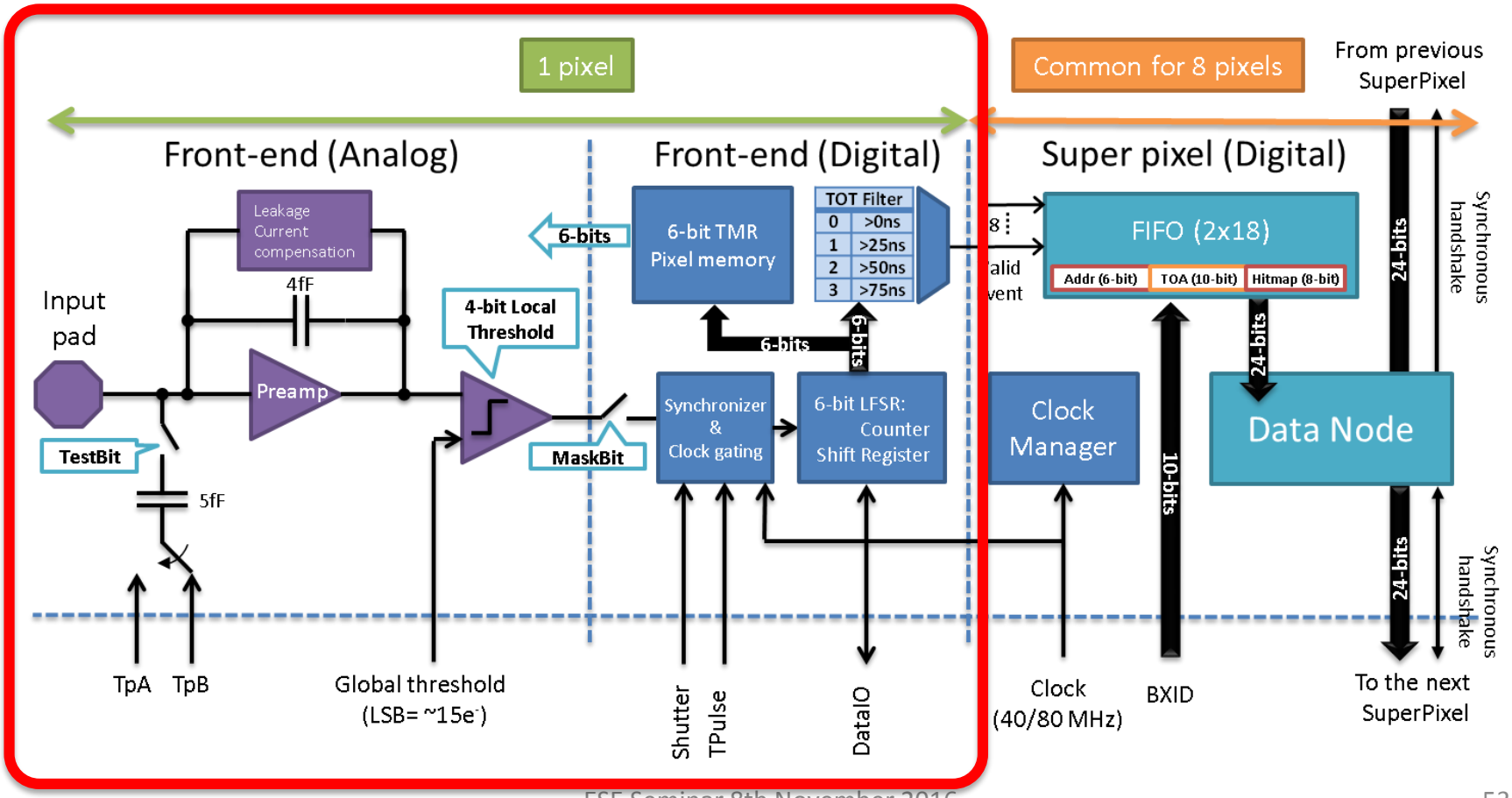
VeloPix Serializers (GWT)

- A low power (~20mW) 5.12 Gbps byte-interleaved serializer and wireline transmitter (NIKHEF).
- Voltage driver, large swing (1.6 V diff)
- Measure internally generated PRBS15 signal with scope → Measured BER<10^{-12}

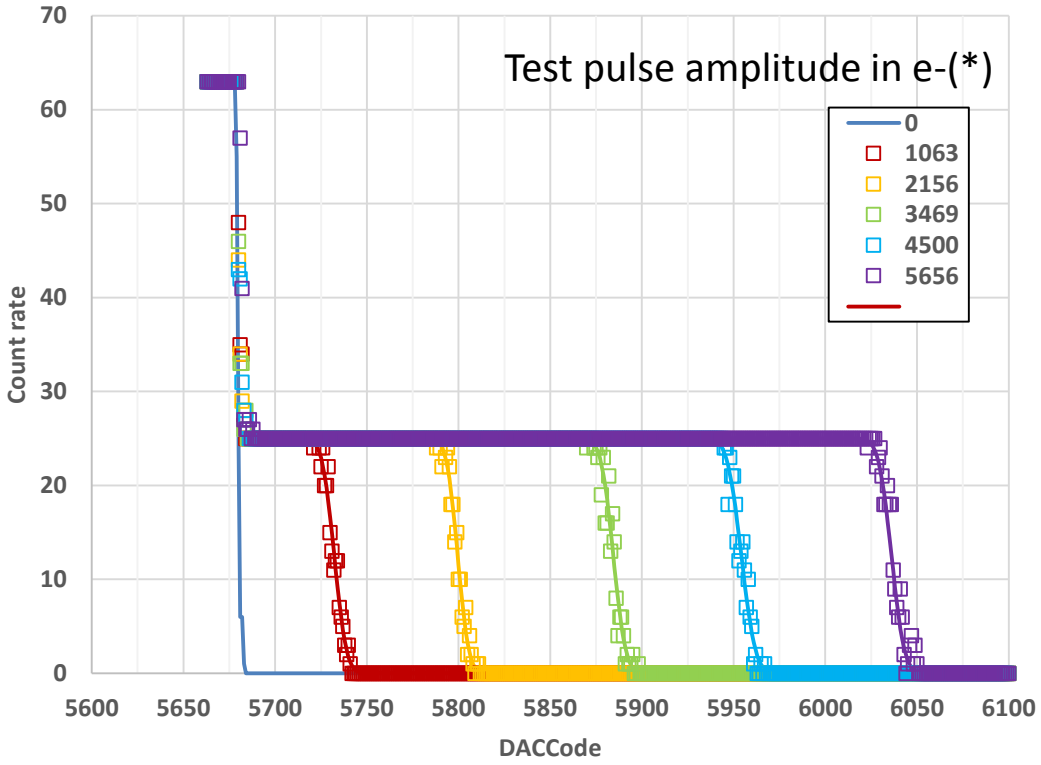
Eye of VeloPix PRBS15 stream

FE Measurements

- Front end characterization measurements done through the slow control readout.

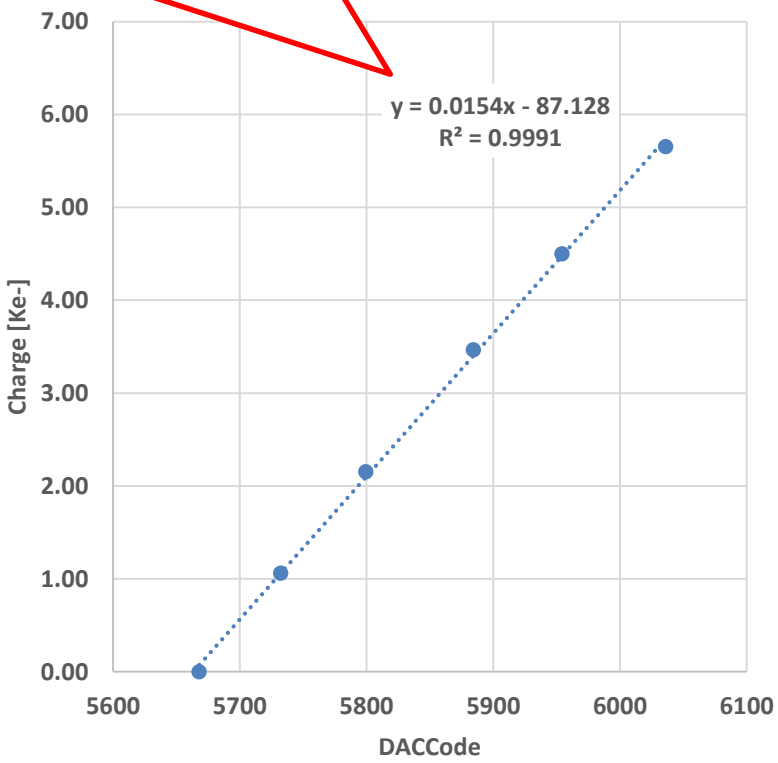


Front-end gain: (test pulses in one pixel)



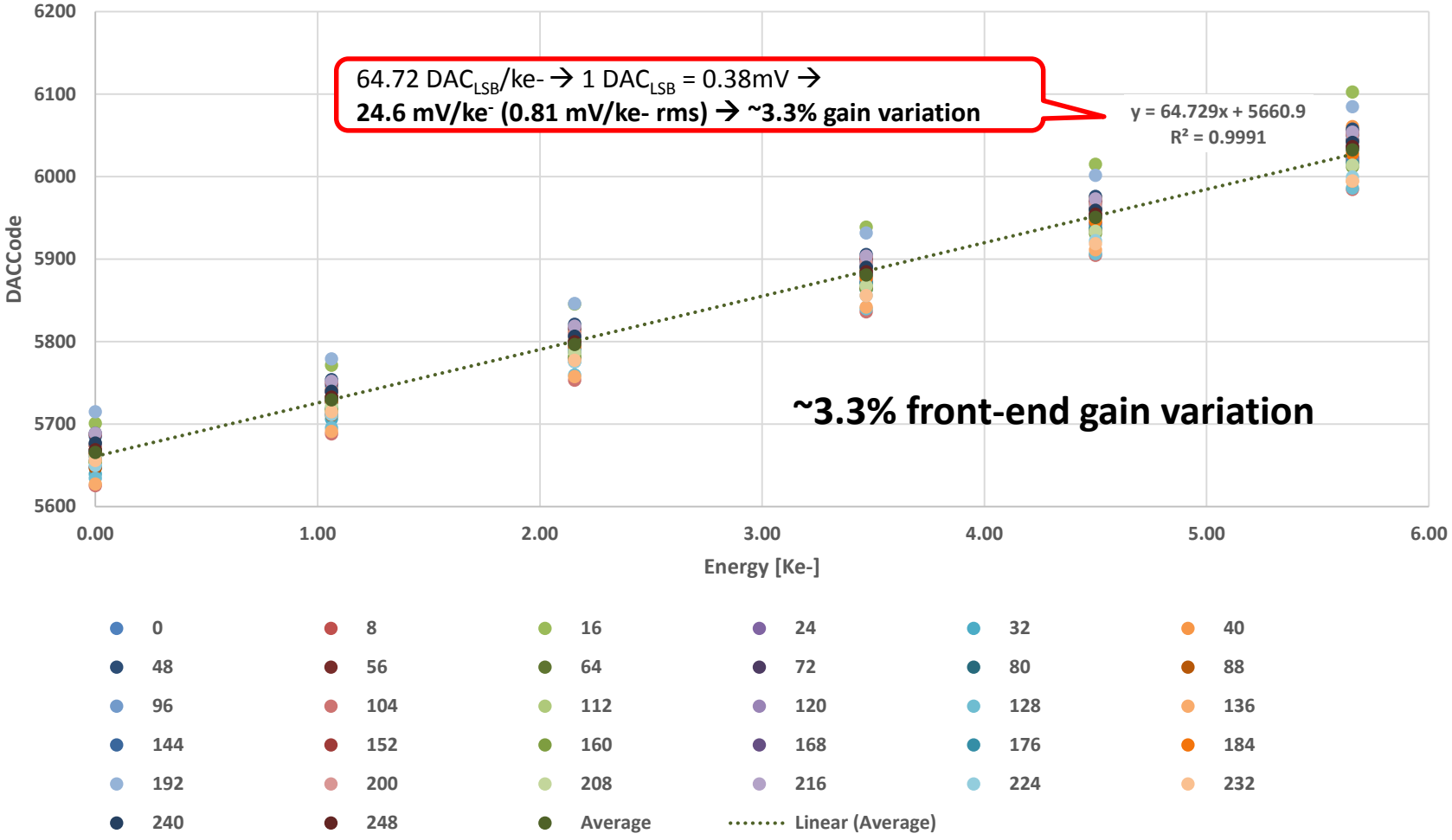
Global threshold level

0.0154 e^-/DAC_{LSB}* → 1 DAC_{LSB} = 0.38mV → **24.6 mV/ke^-**



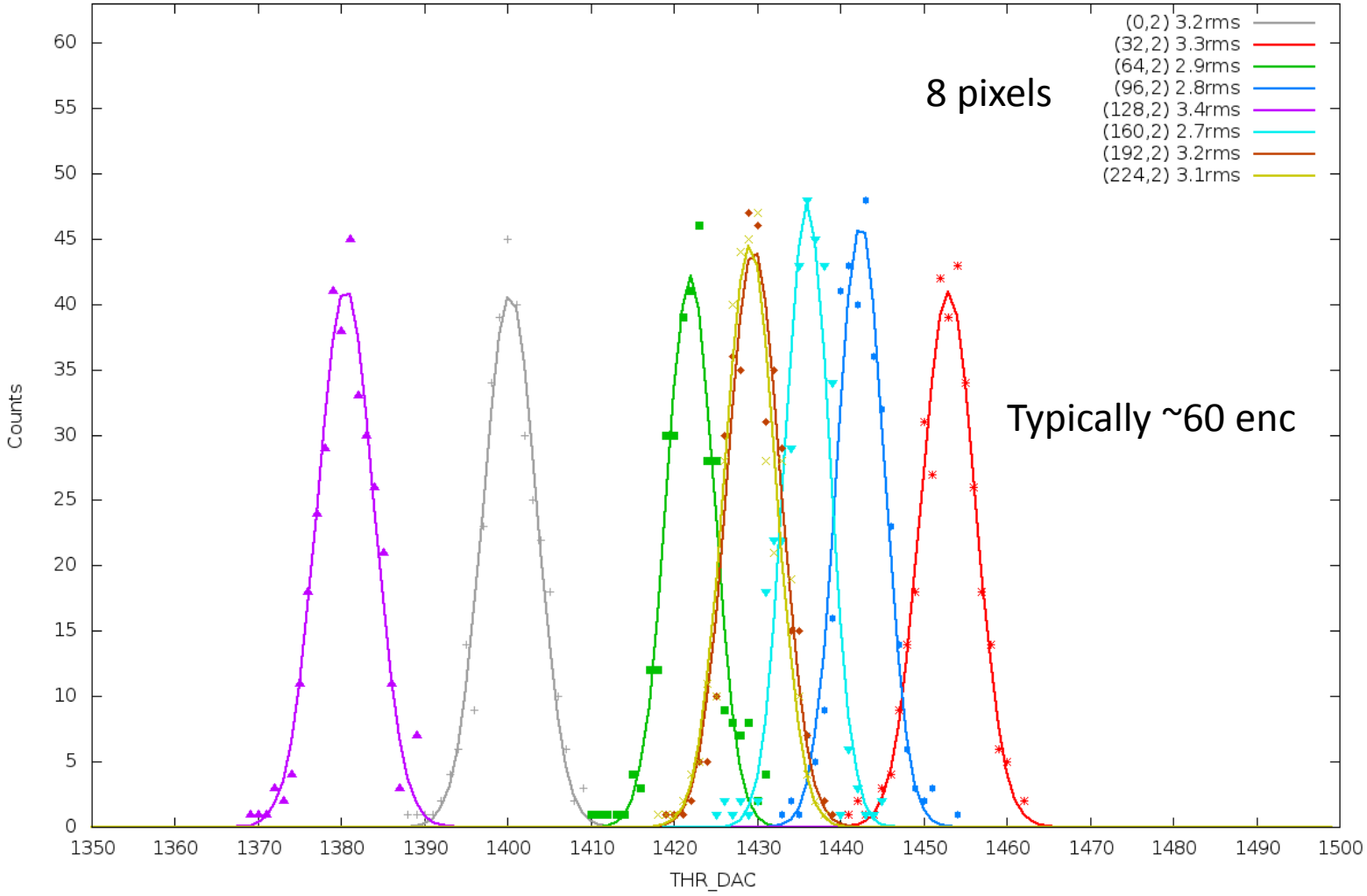
*Assuming Ctest=5fF

Front-end gain uniformity (test pulses in 32 pixels)

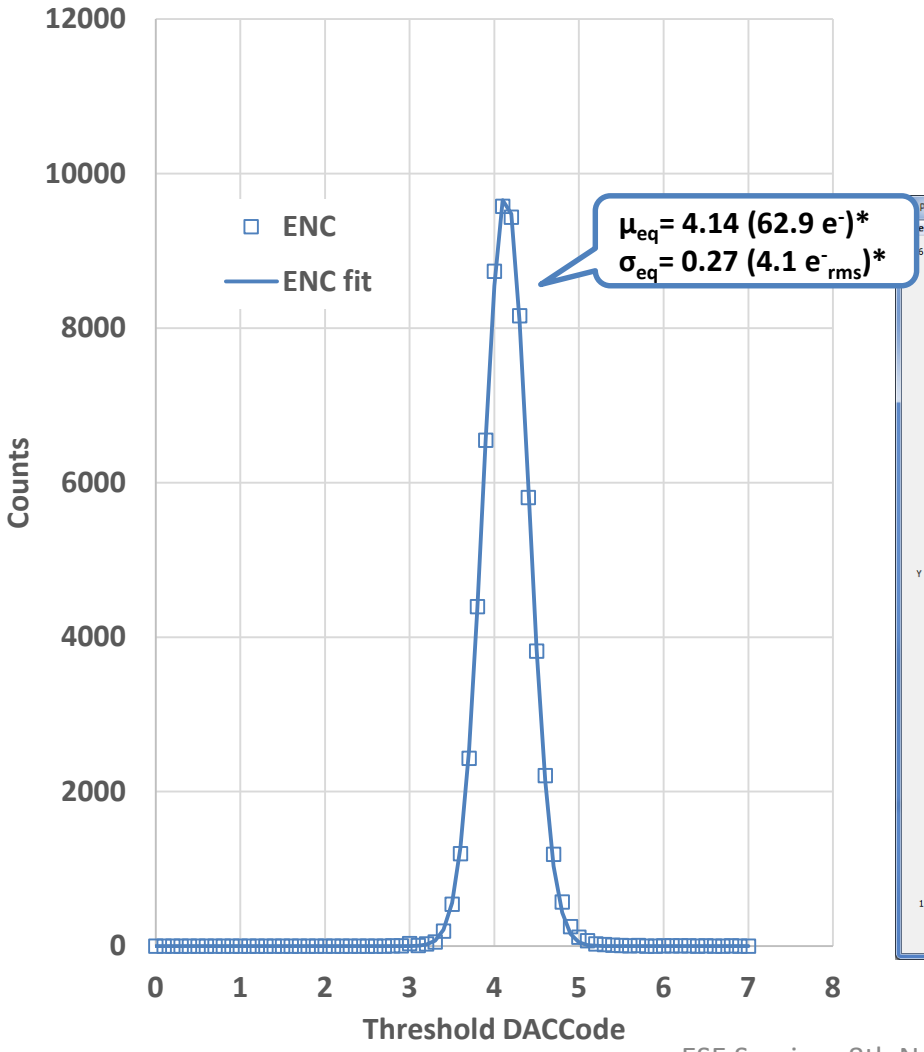


Pixel ENC.

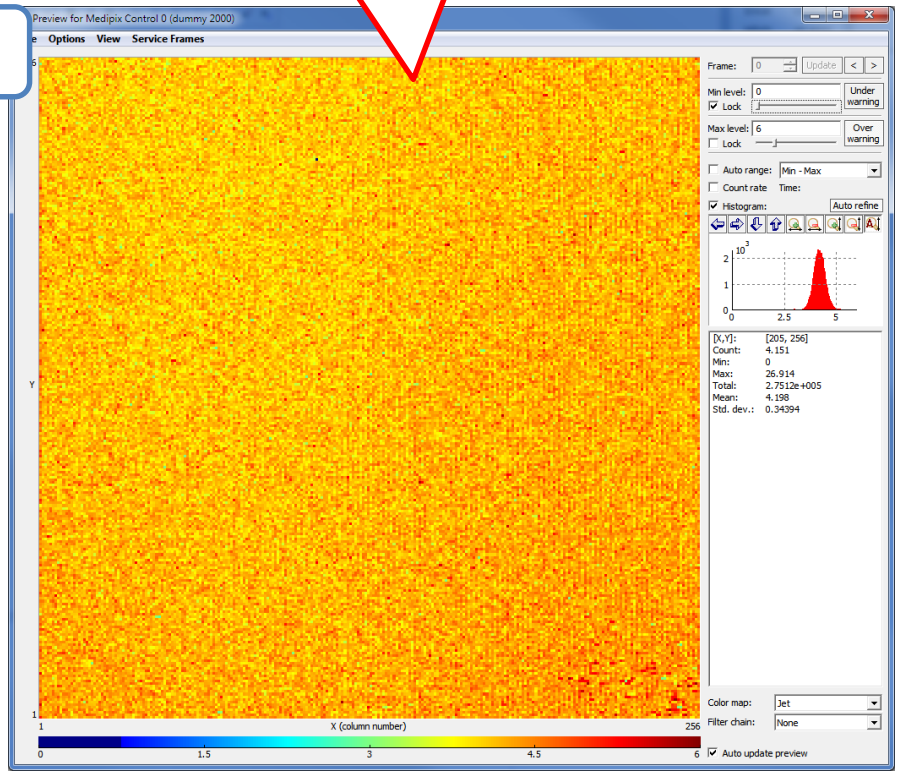
[Threshold scan over noise floor in PC mode]



ENC of full matrix.

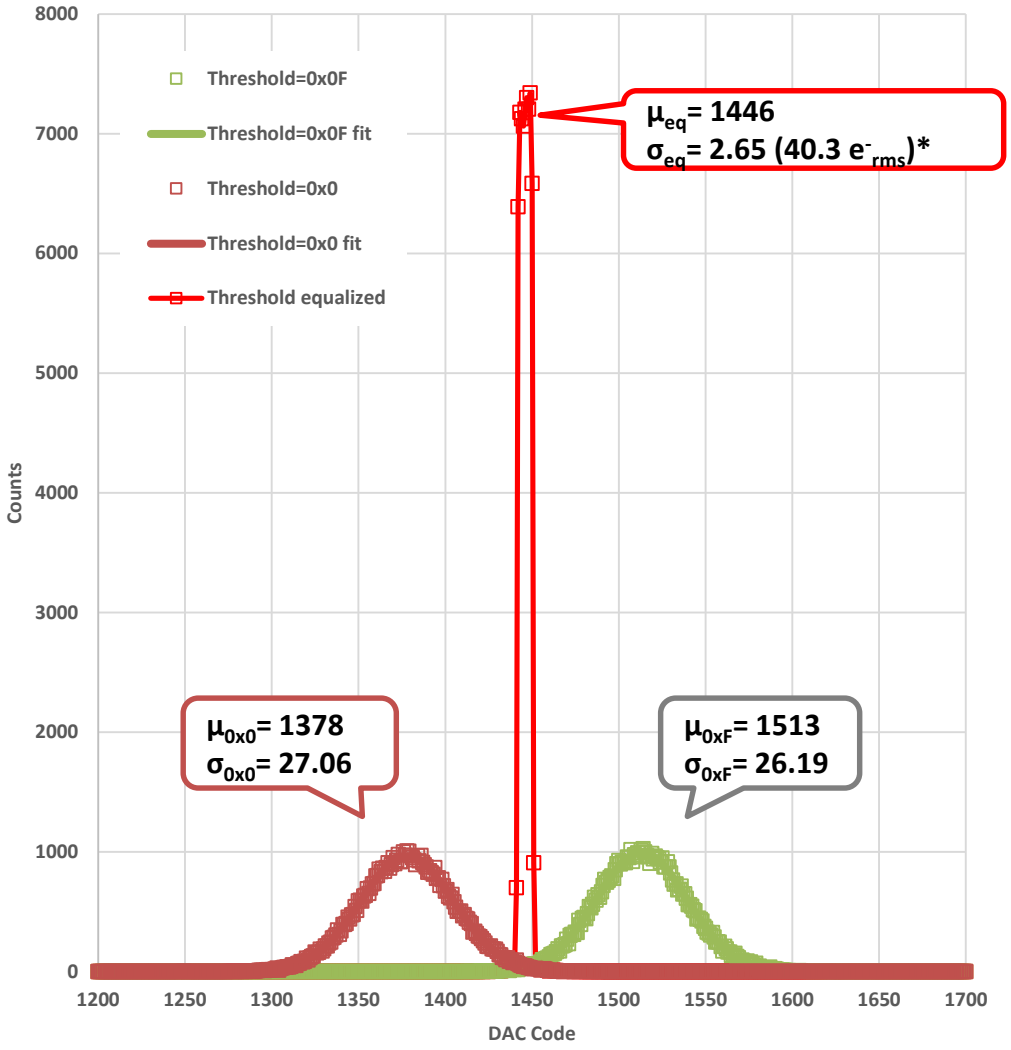


Measured ENC of all pixels
- **Threshold scan over noise floor**
- **All pixels at code 0xF**
- **No trend visible**

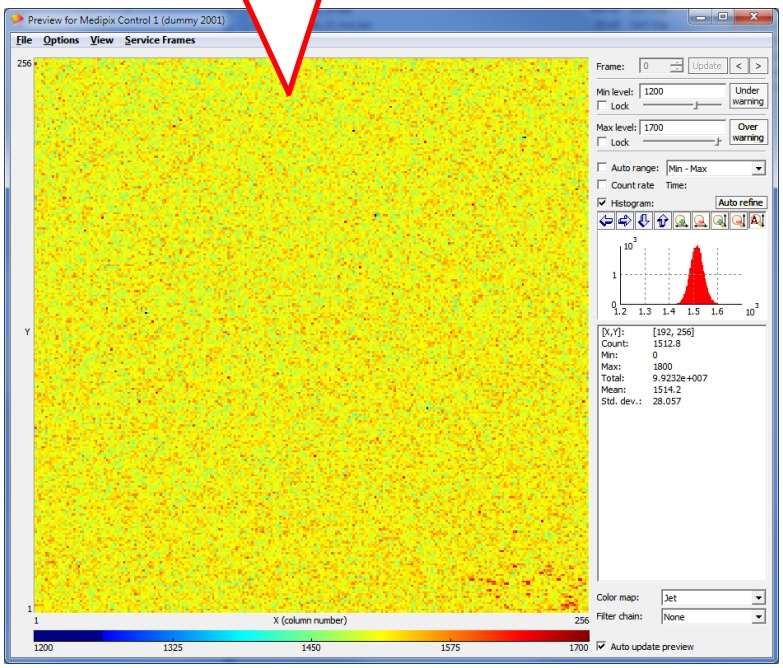


*@gain of 25mV/ke$^-$

Threshold Equalization.



Unequalised Threshold distribution:
- **All pixels at code 0x0**
- **No trend visible.**



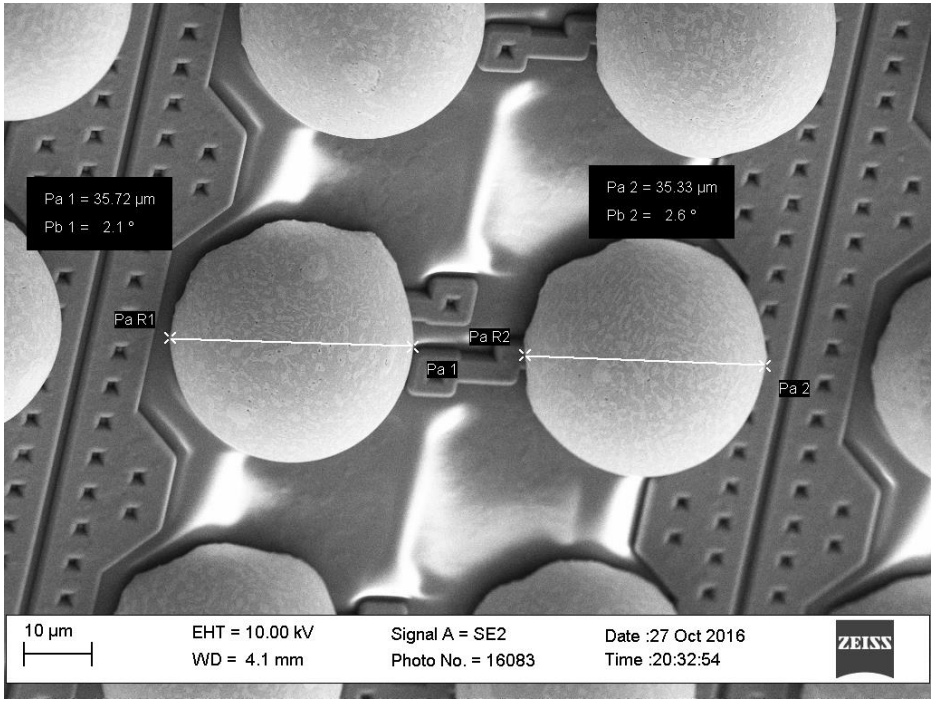
*@gain of 25mV/ke^-

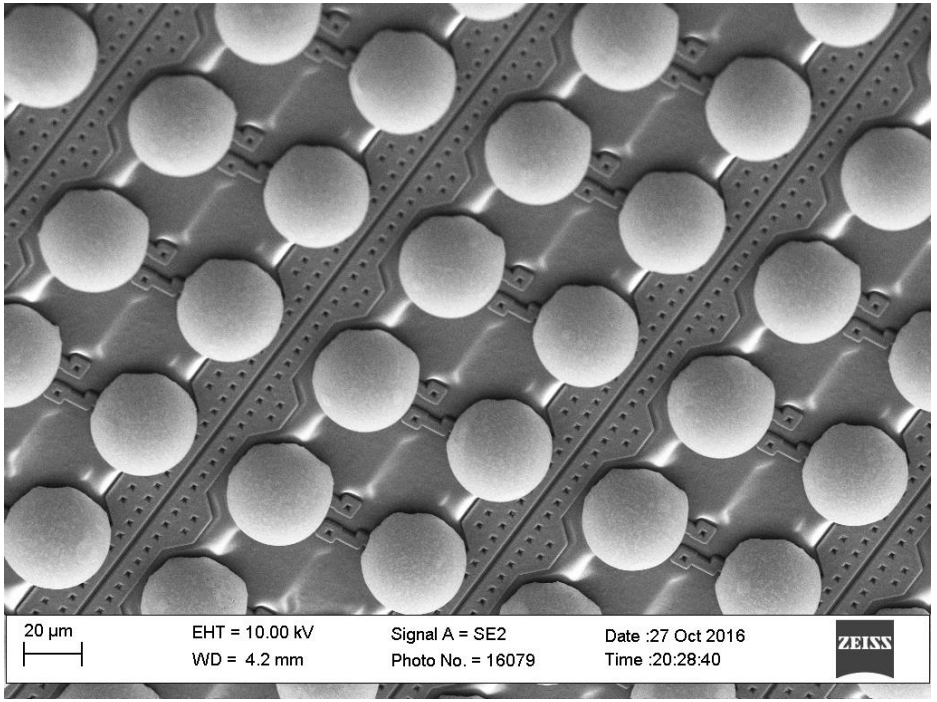
Summary of pixel measurements

Pixel gain	~24.6 mV/Ke$^-$
Pixel to pixel gain variation	~3.3%
Pixel ENC	62.9 e$^-$
Pixel to pixel threshold mismatch	410 e$^-$rms
Pixel to pixel threshold mismatch calibrated (Threq)	40.3 e$^-$rms
Expected minimum threshold	> 450 e-

Threshold equalization only calculated not measured on chip
All measurements assuming Ctest=5fF

Bumps on a Velopix chip

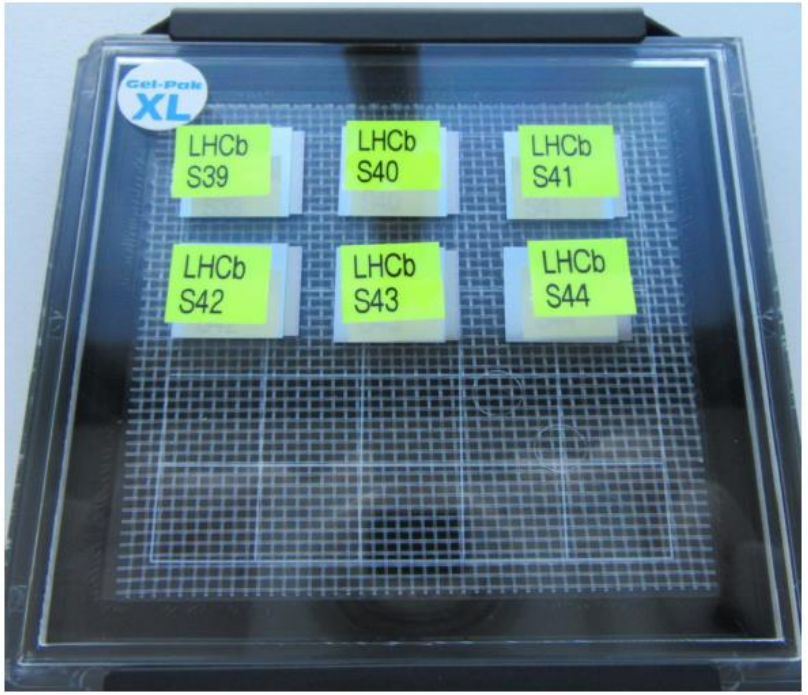




SEM images done by S. Vähänen (Advacam)

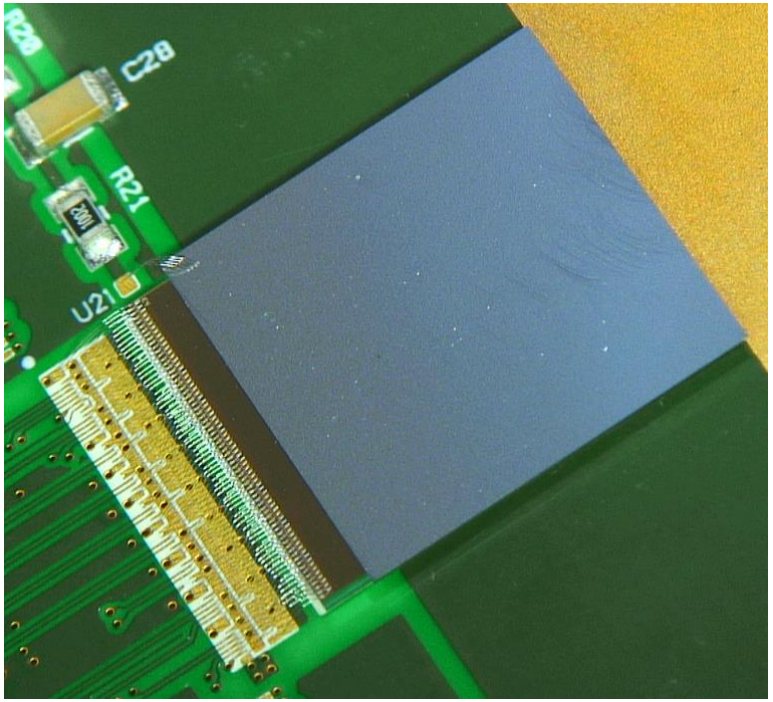
Velopix Modules

- Bumping to the 200 µm n-p Hamamatsu Si sensor
- 8 3x1 modules and 6 single sensors available
- Not thinned → Experiment requires thinning to ~200 µm

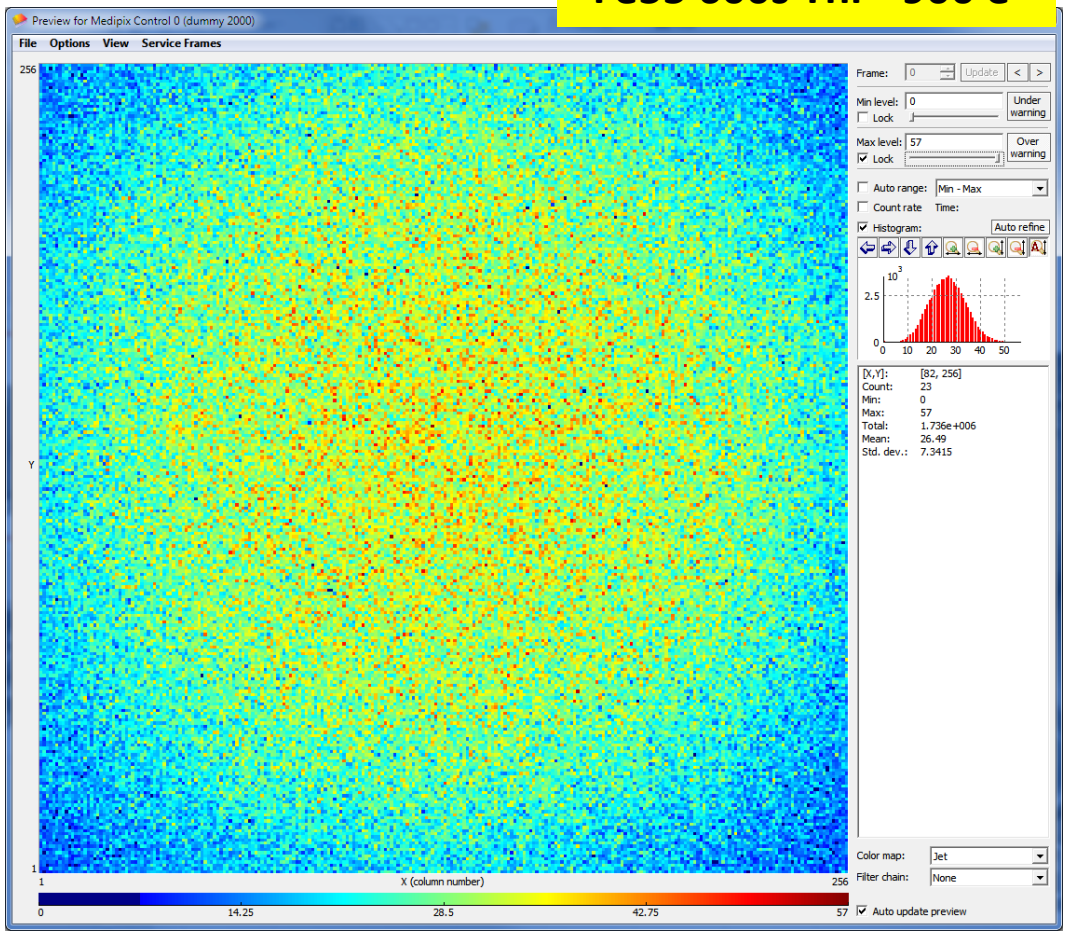


First source measurements [S40 single sensor]

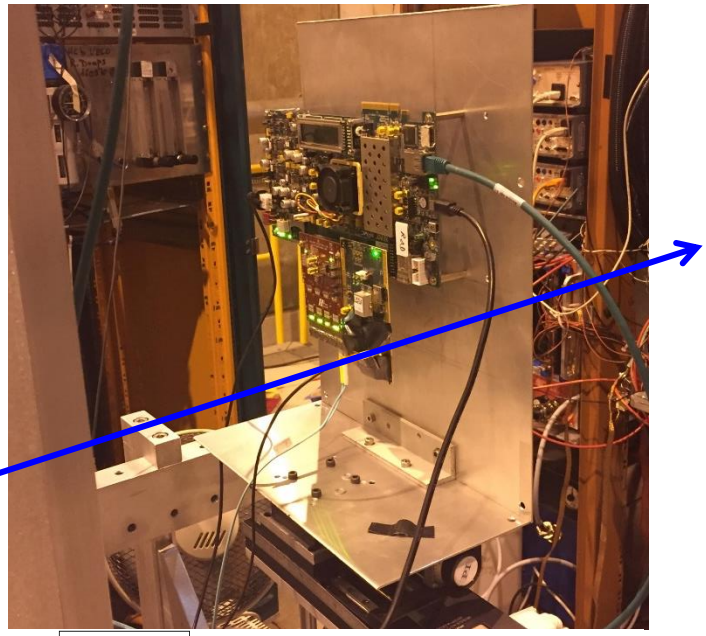
- Image taken through the ECS (Slow Control) in photon counting mode



Fe55 600s Thr ~900 e-



Beamtest



- First VeloPix in testbeam last Sunday
- Image taken through 1 GWT link
- Hitmap from 1 SPS spill (~5 sec)
- Received 2.6 Million Superpixel packets with 3.42 Million pixel hits:
  - Numbers consistent with #tracks recorded by the Timepix3 telescope (upstream of VeloPix)
  - Linking of VeloPix hits to telescope tracks to be done
- **Note that this is only 0.1% of the rate capability of VeloPix !**

Still to do…

- Obtain calibration with X-ray sources:
  - Extract correct FE characterization (ENC, gain…)
- Read the chip at full bandwidth with all GWT (20 Gbps):
  - where to find such beam?
- Whole setup test using: GBT as clock reference, optical drivers, 200m of fibers and miniDaq
- TID and SEU irradiation campaigns
- Production testing later this year at CERN

Conclusions

- VeloPix ASIC designed in 130nm CMOS for the LS2 VELO upgrade
- First results show the chip is alive and eyes open:
  - Power < 2 W/ASIC, DACs working, pixels functional
  - Pixel: Gain ~25 mV/Ke- and ENC 63 e- (no sensor)
  - GWT serializer working
- All measurements, so far, indicate that the Velopix chip is fully functional as designed:
  - First source images taken in photon counting mode : Slow Control
  - First beam test through the binary readout chain @ low rate
  - Scheduled TID and SEU campaigns to validate design robustness

VeloPix Contributors

- ASIC designers:
  - R.Ballabriga, V.Gromov, X.Llopart, S.Miryala, T.Poikela, J.D.Schipper and W.Wong
- IP Blocks:
  - eCDRPLL: R. de Oliveira and P. Leitao
  - Band-Gap: S. Michelis
- Support, readout and Testing:
  - J. Alozy, M.van Beuzekom, H.Boterenbrood, B. van der Heijden, J. Buytaert, M.Daldoss and E.Lemos