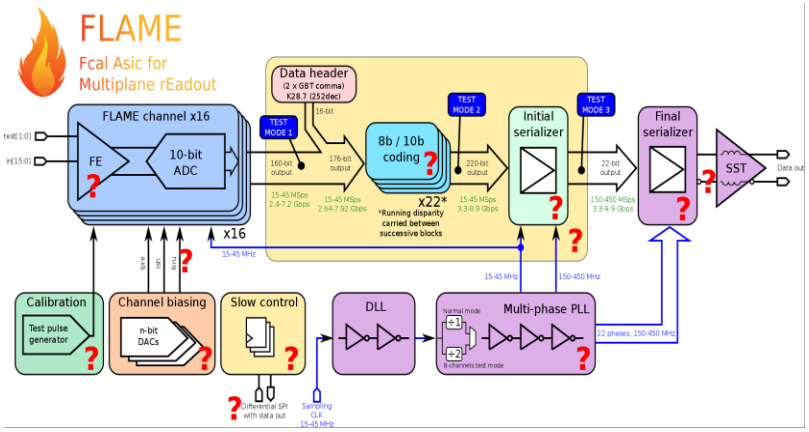
FPGA module prototype for ADC comunication
Status work

Bartosz Dziedzic, Witold Daniluk, Tomasz Wojtoń, Leszek Zawiejski

IFJ PAN, Cracow

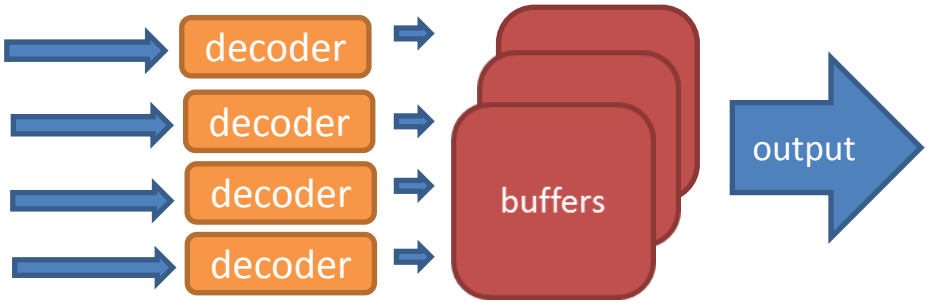
Si sensors: the new design of the readout electronics

Dedicated the FLAME system

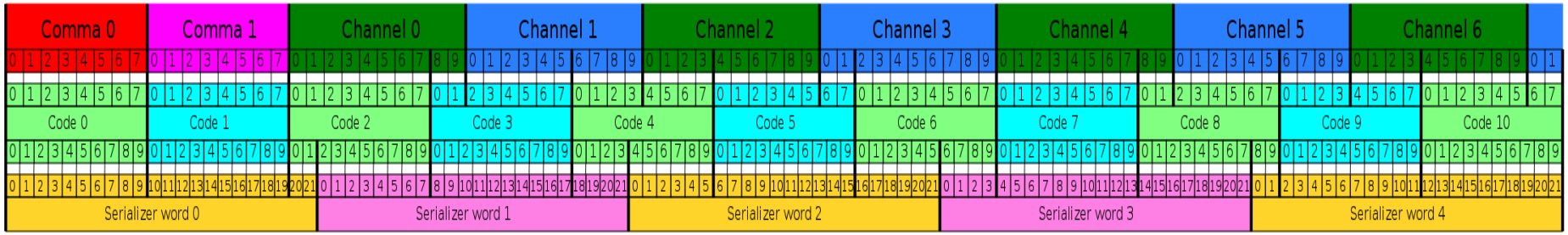


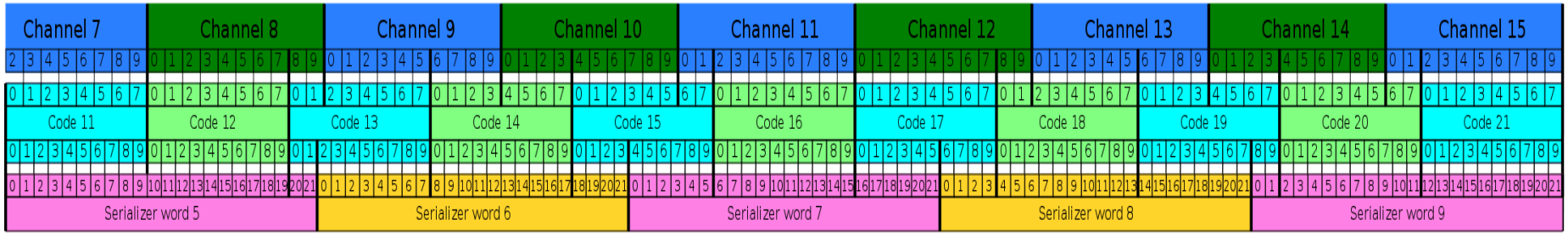
Data received from ASIC's of the FLAME readout sytem

FPGA module for ADC communication



ASIC output: 220 bits in 22 words (16 channels x 10b + 2 x 8b (commas) + coding (8b/10b)



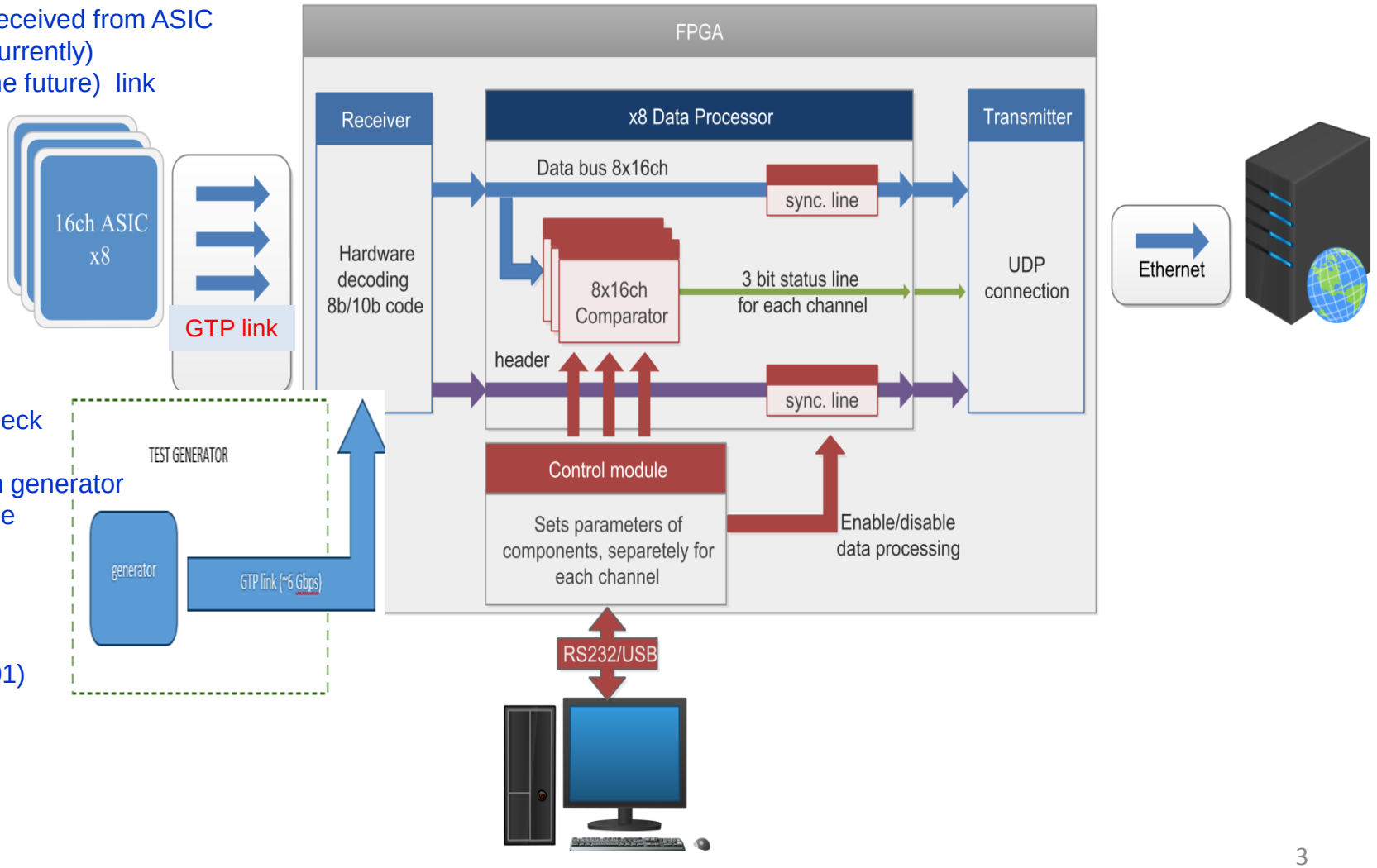


FPGA - Data flow scheme

Schematic view of the data flow within the FPGA,
with some active modules between which the data flow take place

Real data : received from ASIC
using GTP (currently)
or GTX (in the future) link

Test data: check
transmission
using pattern generator
created inside
the FPGA
structure
which sends
string of bits
(like 01010101)



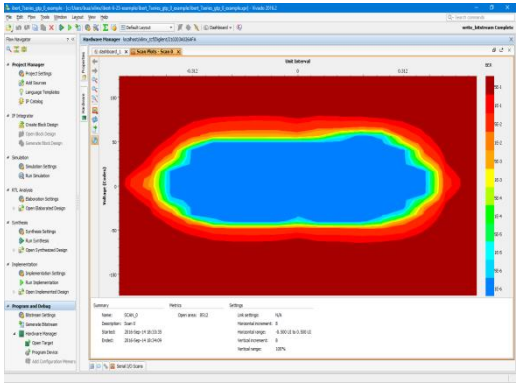
Stages of work on a final version of the prototype

- Test of the hardware link and its quality: transmitter – receiver (GTP)
- Checking the quality of the transferred data:
  from pattern generator to frame check
- Processing of the received data from ASIC and send them to storage

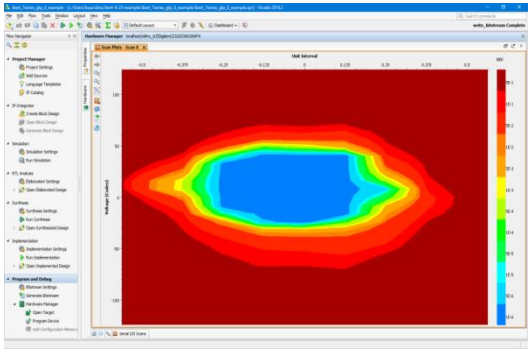
Hardware test: transceiver (T+R)

The blue color represents area with a small number of errors
and red one where attempt to read signals gives the only errors

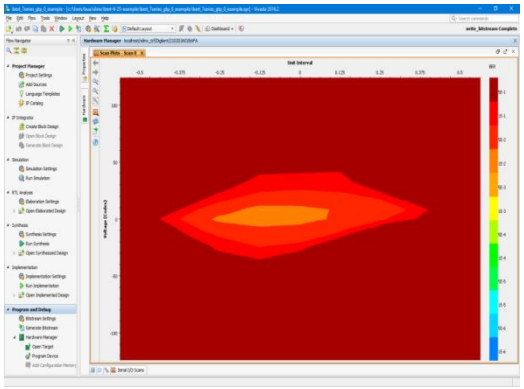
3.125 Gb/s rate



6.25 Gb/s rate



Satisfactory quality of the signal transmission at the different thicknesses and lengths of the cables (up to several meters in length)

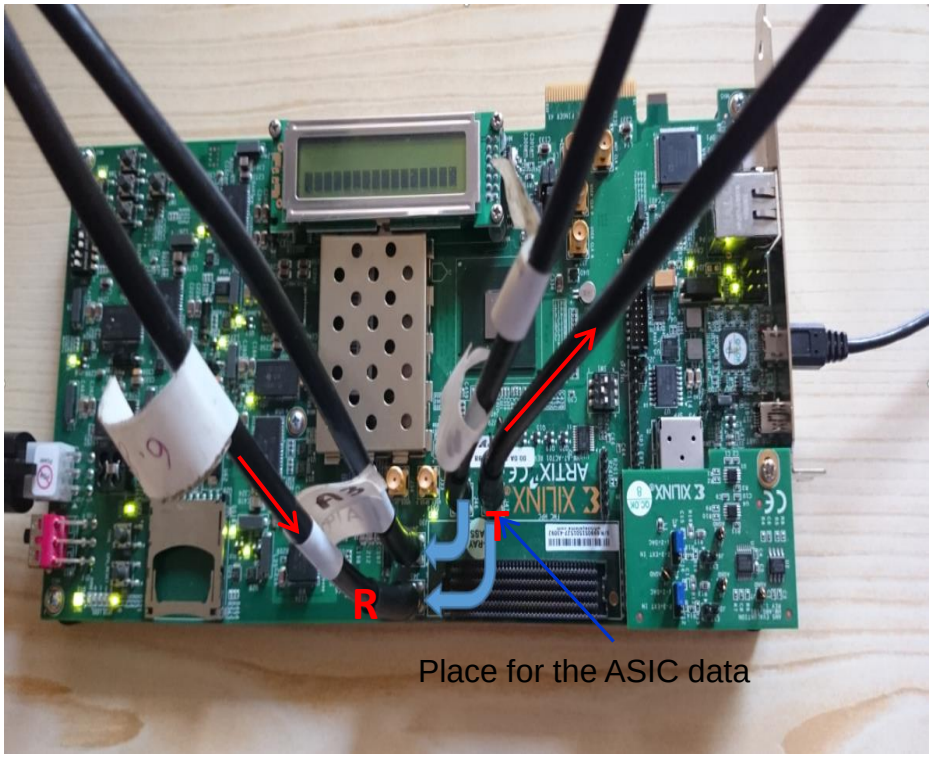


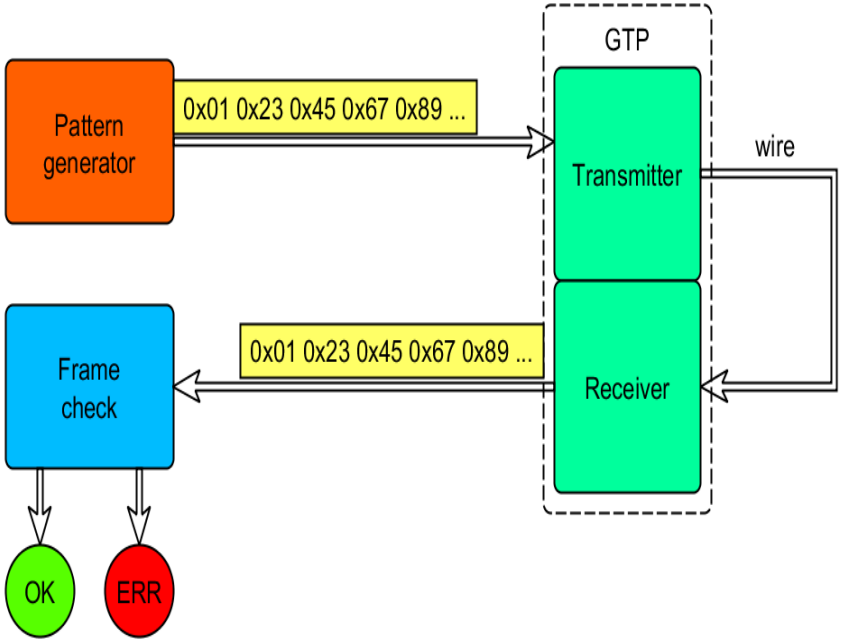
But big distortion of the signal shape when cables had different length

Evaluation board contains FPGA-Artix 7 XC7A200T (XILINX) with GTP transceivers with the maximum bandwidth 6.6 Gb/s.
For 1 ASIC working with 20 MHz sampling, the expected rate is 4.4 Gb/s and GTP link is enought for tests it and for SMA connectors only one transceiver can be set.
Ethernet - 1 Gbps

5

Hardware link: test of the transmission

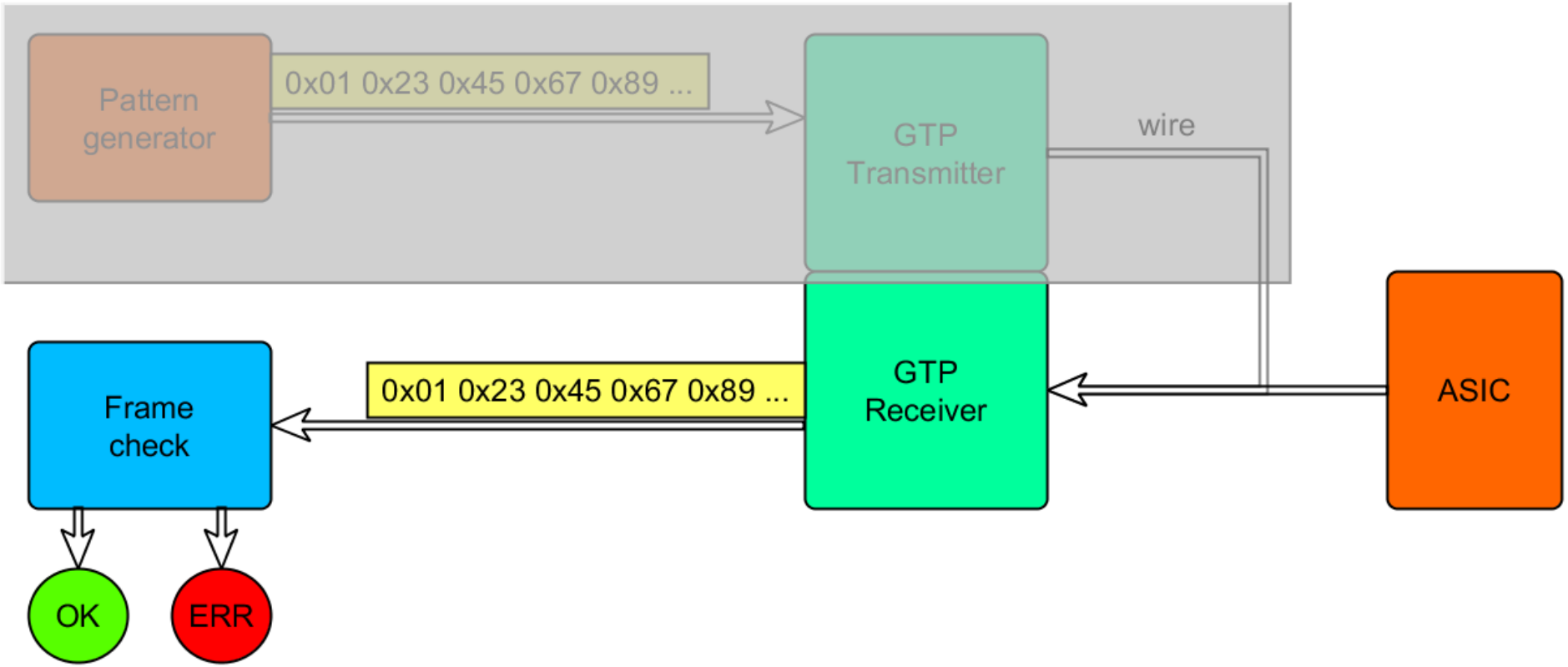




- Used a transceiver on the board with the transmitter connected to the receiver by cables
  Tests of receiver are started after the implementation the transmitter

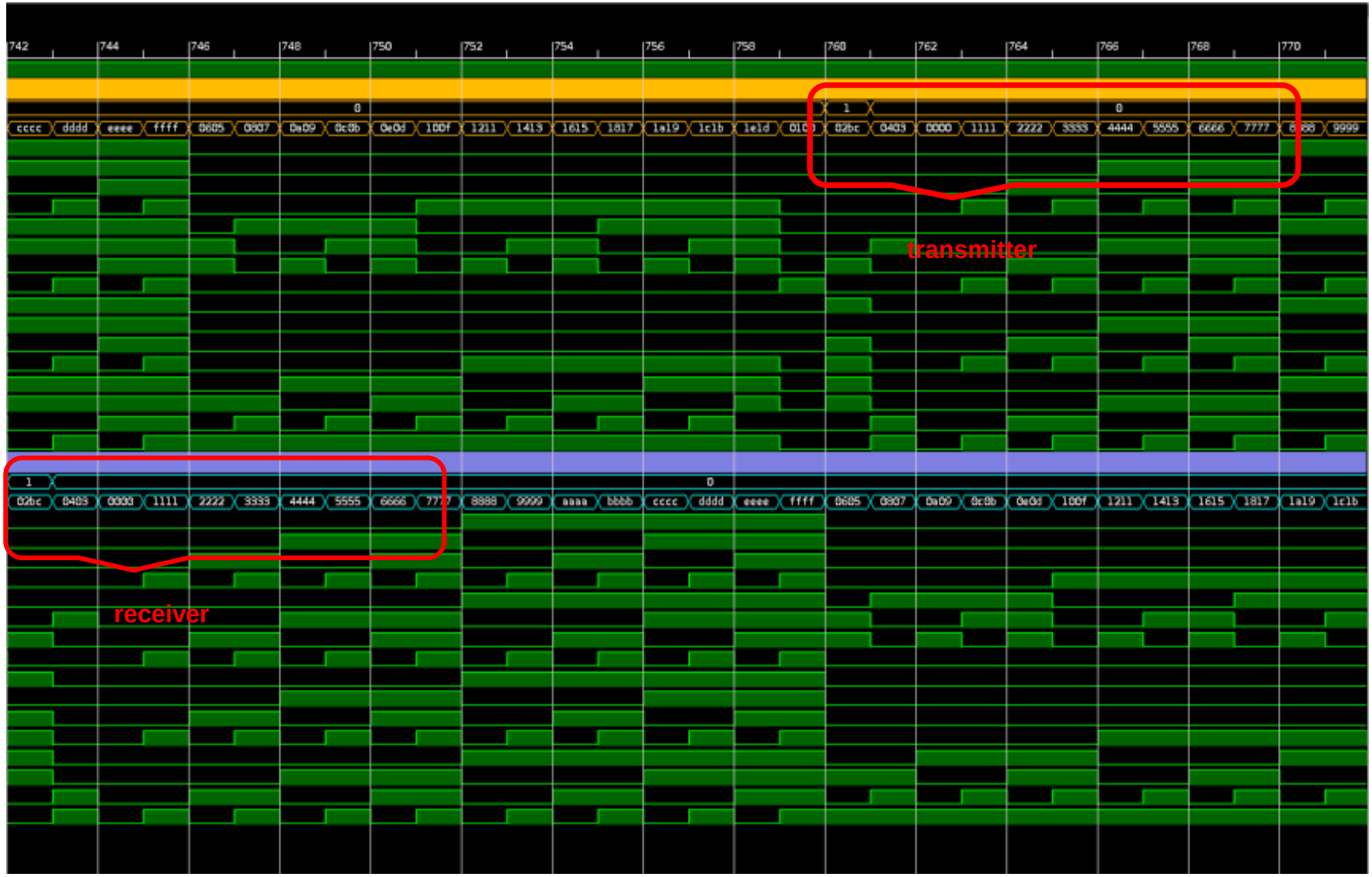
- At this stage we have defined a sequence of bits that are send and verify at receiver.

Next step: data processing

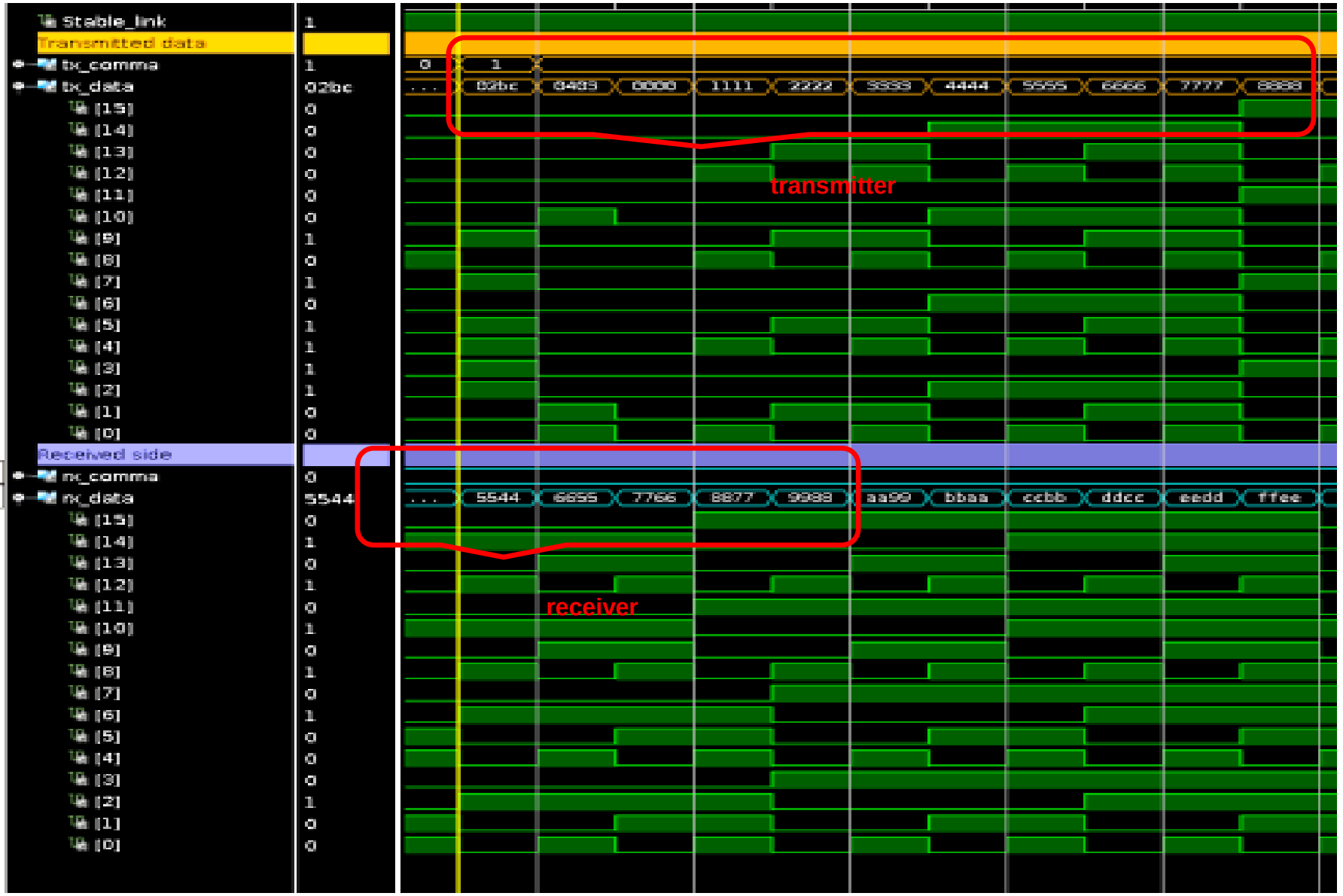


Exchange the pattern generator with pattern generator in ASIC and test transmission between ASIC and frame check module in FPGA

Optimisation of the processing



Optimisation of the processing: the sequence of bits was changed



SUMMARY

- Noticeable progress has been achieved in the work on the final prototype FPGA module for ADC communication with server data

- Work is ongoing to optimise processing, build trigger and prepare data to be send by Ethernet

- In the final step the ASIC data (from FLAME readout system) will be used