



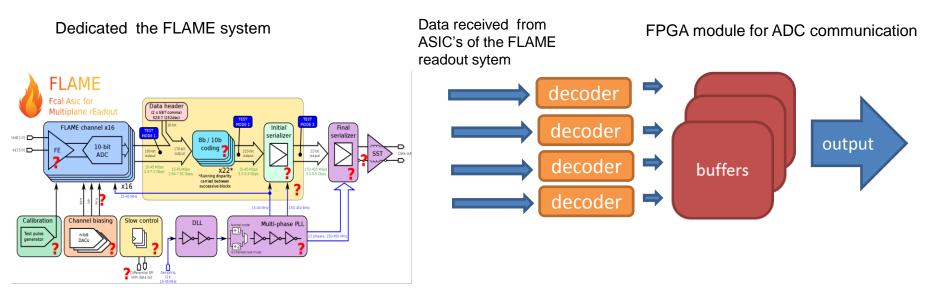
# FPGA module prototype for ADC comunication Status work



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### Si sensors: the new design of the readout electronics



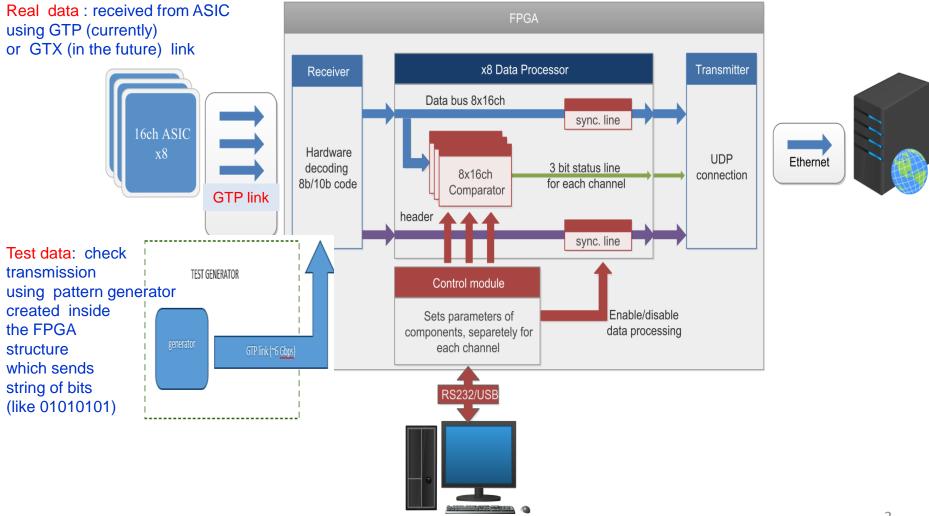
#### ASIC output: 220 bits in 22 words (16 channels x 10b + 2 x 8b (commas) + coding (8b/10b)

Comma 0	ma 0 Comma 1 Channel 0		Channel 1	Channel 2	Channel 3		Channel 4	Chan	nel 5 C	Channel 6
0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7 8	9 0 1 2 3 4 5 6 7 8	9 0 1 2 3 4 5 6 7 8 9	0 1 2 3 4 5 6	7890	) 1 2 3 4 5 6 7 8	9 0 1 2 3 4 5	6 7 8 9 0 1 2 3	8 4 5 6 7 8 9 0 1
0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7 0	1 2 3 4 5 6 7 0 1 2	3 4 5 6 7 0 1 2 3 4 5	6 7 0 1 2 3 4	5670	1 2 3 4 5 6 7 0	1 2 3 4 5 6 7	0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7
Code 0	Code 1	Code 2	Code 3 Co	de 4 Code 5	Code 6		Code 7	Code 8	Code 9	Code 10
0 1 2 3 4 5 6 7 8 9	0 1 2 3 4 5 6 7 8 9	0 1 2 3 4 5 6 7 8 9 0	1 2 3 4 5 6 7 8 9 0 1 2 3	4 5 6 7 8 9 0 1 2 3 4 5 6	789012345	6 7 8 9 <mark>0</mark>	1234567890	1 2 3 4 5 6 7 8	9012345678	9 0 1 2 3 4 5 6 7 8 9
0 1 2 3 4 5 6 7 8 9	10111213141516171819	2021 0 1 2 3 4 5 6 7 8	9 101112131415161718192021	0 1 2 3 4 5 6 7 8 9 101112	131415161718192021	0 1 2 3 4	5 6 7 8 9 10 11 12 13 14 1	51617181920210	1 2 3 4 5 6 7 8 9 10	112131415161718192021
Serialize	er word 0	Seria	lizer word 1	Serializer word	Serializer word 3			Serializer word 4		

(	Channel 7	Channel 8 Chann		Channel 9 Channel :		Channel 11	Channel 12	Channel 1	(	Channel 14	Channel 15	
2	3 4 5 6 7 8 9	0 1 2 3 4 5 6 7	9 0 1 2 3 4 5	6 7 8 9 0 1 2	3 4 5 6 7 8 9 0	1 2 3 4 5 6 7 8 9	0 1 2 3 4 5 6 7	8 9 0 1 2 3 4 5 6 7	8 9 0 1 2 3	3 4 5 6 7 8 9 0	1 2 3 4 5 6 7 8 9	
0	1 2 3 4 5 6 7	0 1 2 3 4 5 6 7	1234567	0 1 2 3 4 5 6	7 0 1 2 3 4 5 6	7 0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7 0 1	2 3 4 5 6 5	7 0 1 2 3 4 5 6	7 0 1 2 3 4 5 6 7	
	Code 11	Code 12	Code 13	Code 14	Code 15	Code 16	Code 17	Code 18	Code 19	Code 20	Code 21	
0 1	2 3 4 5 6 7 8 9	0 1 2 3 4 5 6 7 8 9	12345678	9012345678	901234567	<mark>8 9</mark> 0 1 2 3 4 5 6 7 8 9	0 1 2 3 4 5 6 7 8 9	0 1 2 3 4 5 6 7 8 9 0 1	2 3 4 5 6 7 8	901234567	8 9 0 1 2 3 4 5 6 7 8 9	
0 1	2 3 4 5 6 7 8 9 1	10111213141516171819	0210123456	7 8 9 10111213141516	17 <mark>18192021</mark> 0123	4 5 6 7 8 9 101112131415	161718192021 <mark>0123</mark>	4 5 6 7 8 9 101112131415	61718192021 0	1 2 3 4 5 6 7 8 9	101112131415161718192021	
	Serializer word 5		9	Serializer word 6		Serializer word 7		Serializer word 8		Serializer word 9		

### FPGA - Data flow scheme

Schematic view of the data flow within the FPGA, with some active modules between which the data flow take place



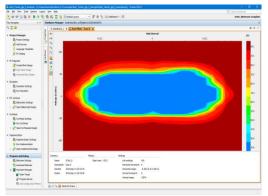
## Stages of work on a final version of the prototype

- Test of the hardware link and its quality: transmitter receiver (GTP)
- Checking the quality of the transferred data: from pattern generator to frame check
- Processing of the received data from ASIC and send them to storage

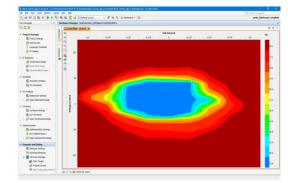
### Hardware test: transceiver (T+R)

The blue color represents area with a small number of errors and red one where attempt to read signals gives the only errors

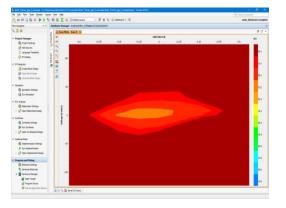
#### 3.125 Gb/s rate



6.25 Gb/s rate



Satisfactory quality of the signal transmission at the different thicknesses and lengths of the cables (up to several meters in length)

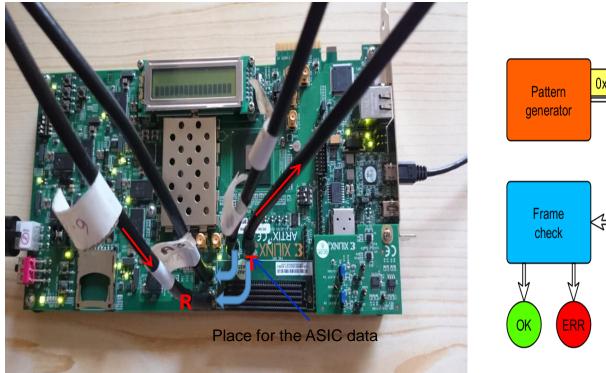


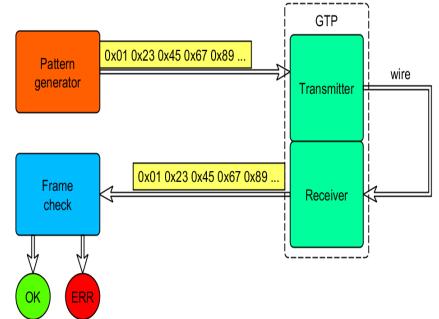
But big distortion of the signal shape when cables had different length

Evaluation board contains FPGA-Artix 7 XC7A200T (XILINX) with GTP transceivers with the maximum bandwidth 6.6 Gb/s. For 1 ASIC working with 20 MHz sampling, the expected rate is 4.4 Gb/s and GTP link is enought for tests it and for SMA connectors only one transceiver can be set. Ethernet - 1 Gbps

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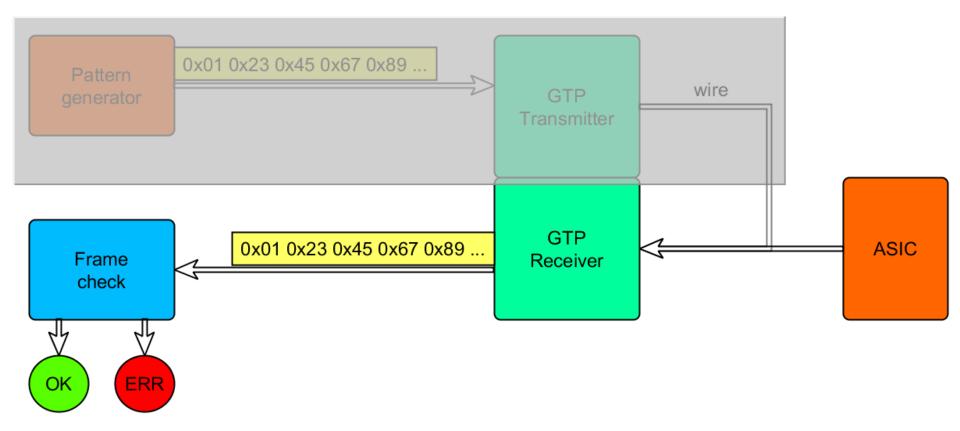
### Hardware link: test of the transmission





- Used a transceiver on the board with the transmitter connected to the receiver by cables Tests of receiver are started after the implementation the transmitter
- At this stage we have defined a sequence of bits that are send and verify at receiver.

# Next step: data processing



Exchange the pattern generator with pattern generator in ASIC and test transmission between ASIC and frame check module in FPGA

# Optimisation of the processing

742	744	746	748	750 7	52	754	756	758	760	762	764	766	768	770
eece V ddde		0605 ( 0907 )	_		1211 / 1418				1 X			0 4444 ¥ 5555	6666 × 7777	( 8 88 V 9999
<u>( ecce                                 </u>						1017								
										ransmit	tor			
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02bc 8485	3999 1111	2222 3333	4444 5555	(6666) 777 7)	8888 99999	aaaa boob	ecce dddd		8685 0907	0+09 8:85	0e0d 100f	1211 1413	1615 1817	lal9 leib
	receiv													

## Optimisation of the processing: the sequence of bits was changed

Dashboard Op 🍓 Stable link 1 ک nansmitted data Þ 📲 tx\_comma **(8)** 20 🕈 📲 tx\_data 1111 🗶 2222 🗶 3333 🗶 4444 🌋 5555 🗶 6666 🕽 02bc . . . 025c 📜 0403 🗶 0000 ) 7777 🗙 8888 • B (15) 0 **lê (14)** 20 Ť 10 🖣 [13] 0.5 **le (12)** 80 e, transn 0 18 (1.1.) ۹., **Ve (10)** 1 ile [9] Q 181 4 п **le [7]** M 0 1 **6 [5]** [編][4] 1 16 [3] -1 E. Ø Ve (1) 10 **i a** [0] Received side 0 👷 📲 nc\_data 5544 6655 💥 7766 aa99 🔀 bbaa cebb 🐰 ddee eedd 💥 ffee 8877 🔀 9988 100 5544 V& [15] 51 囁 [14] 8 🍓 (13) а. հի (12) 0 receiver հելույ 1 <sup>1</sup>8 (10) 0 11 8 Q [編][7] 1 O 6 [5] 0 [編] [4] **0**0 **18** [3] 1 **12** Ma (1) 0 le [0]

## SUMMARY

- Noticeable progress has been achieved in the work on the final prototype FPGA module for ADC communication with server data
- Work is ongoing to optimise processing, build trigger and prepare data to be send by Ethernet
- In the final step the ASIC data (from FLAME readout system) will be used