RD50 Collaboration
HV-CMOS submission

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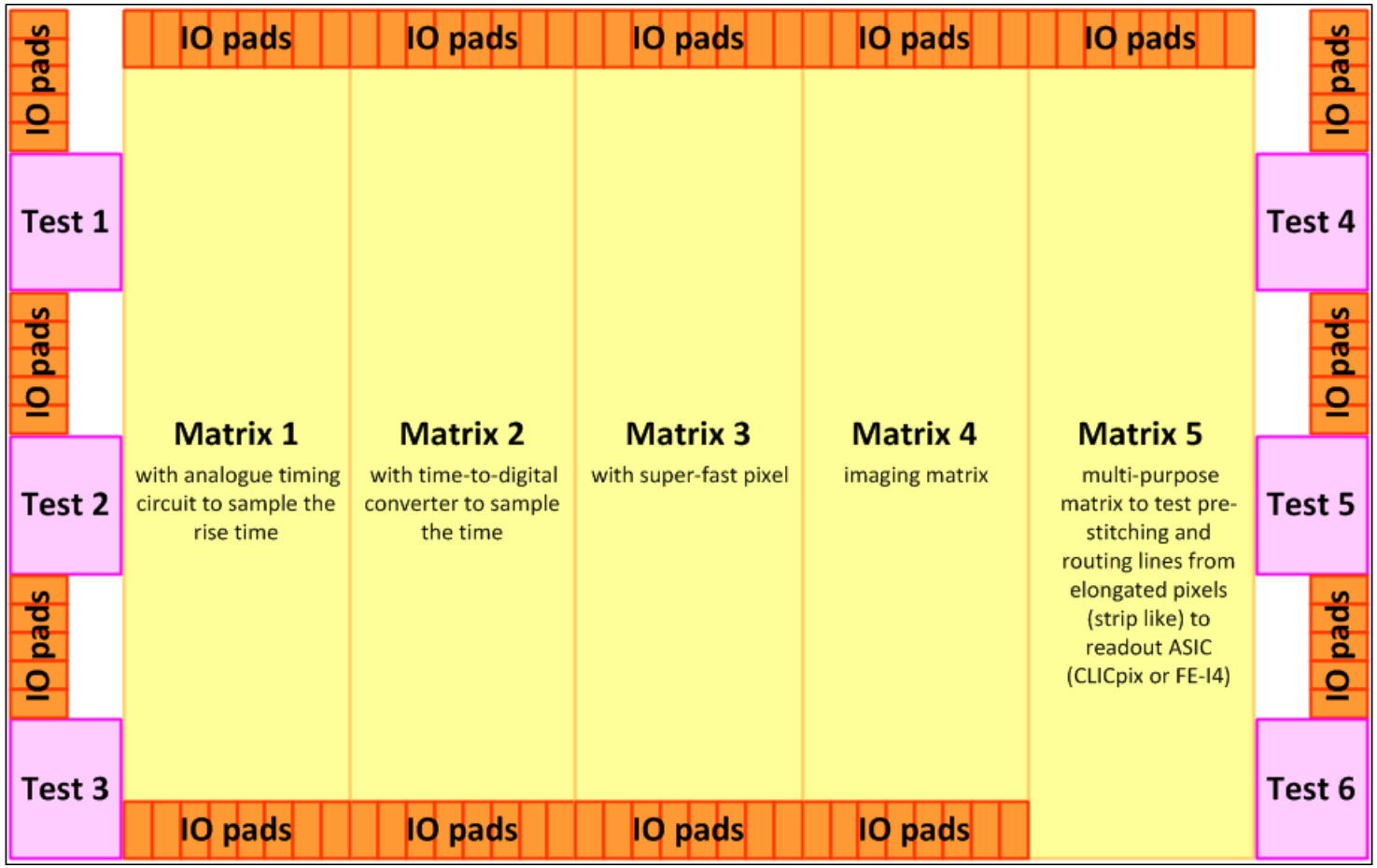
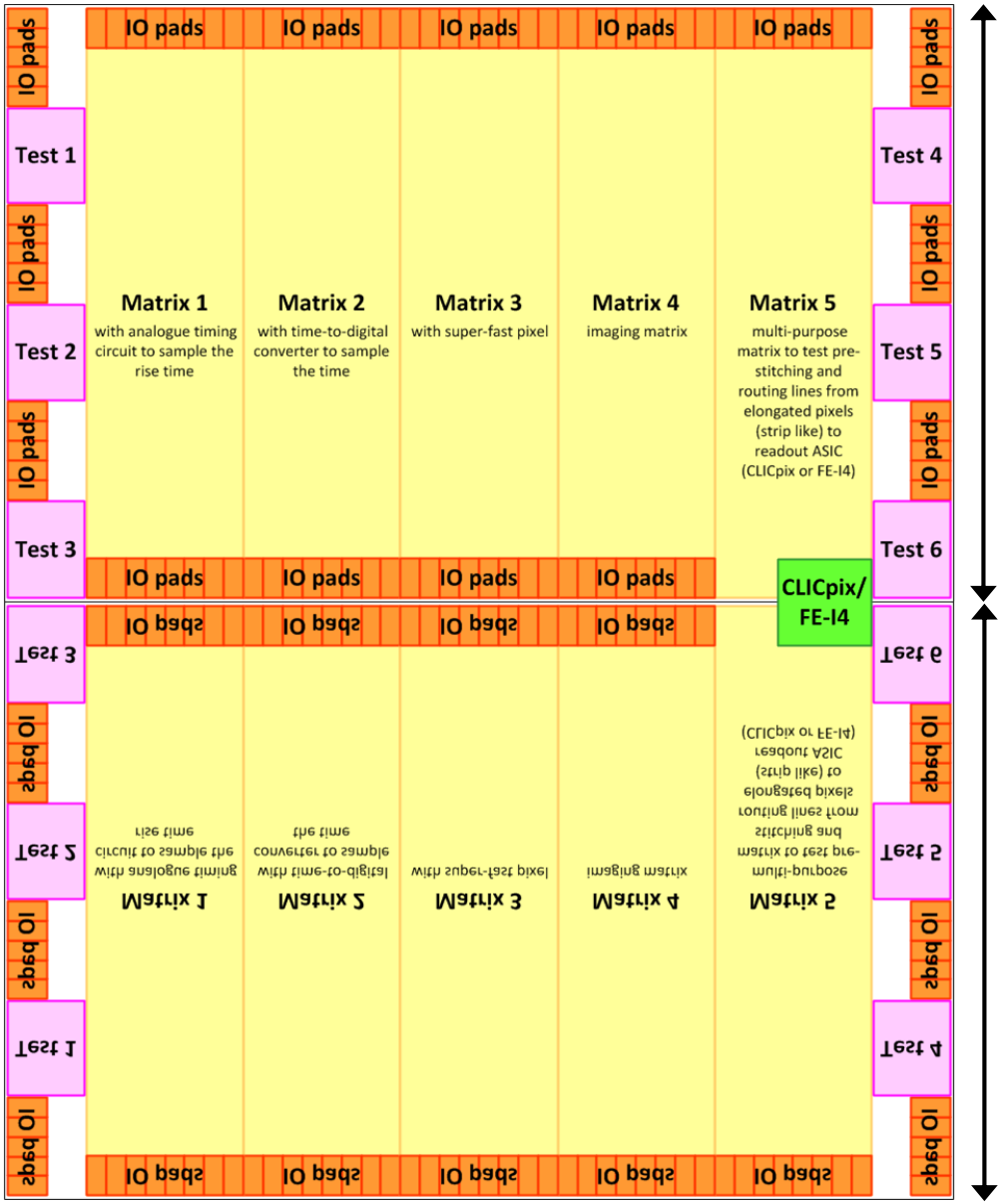
Reticle floorplan



Matrix 5



Reticle type A

Reticle type B
(mirrored design)

Placement accuracy between neighbouring chips? Seal ring?

Comments and topics that we need to discuss

1. There are no dimensions in the floorplan (on purpose)
2. **Pixel size** in each matrix? → This will help us to define the area of each matrix and the area of the chip(*)
3. **Matrix 1.** Timing circuit to sample the rise time:
   - Sampling **frequency**?
   - Sampling of **rise time** only? Sampling of **amplitude**, as well?
4. **Matrix 3.** With super-fast pixel:
   - Shorter rise time is achieved with more power consumption. Power consumption needs to be low.
   - Type of pixel? Binary, TOA measurement, TOT measurement, energy measurement…?
5. **Matrix 4.** Imaging matrix:
   1. Type of readout circuit?
   2. Circuits with converter and Correlated Double Sampling (CDS)?
6. Readout electronics **inside or outside** the pixel area? (especially in matrices 1 and 2)

(*) Maximum design box dimensions are **25,840 mm x 32,480 mm (with full mask set submission)** or **25,840 mm x 9,505 mm (with 1 x 3 MLM submission)**. Requirement to leave space for a PCM structure (1,826 mm x 1,826 mm) inside the design box for foundry tests, and need to confirm with sub-contractor that such large devices can be handled.

Test structures

Test structure 1 Simple CMOS capacitors to study oxide thickness (related to irradiation measurements?)

Design the smallest possible pixel, and with this:

Test structure 2 10 x 10 matrix of pixels with passive readout

Test structure 3 10 x 10 matrix of pixels with 3T-like readout

Test structure 4 Small matrix of pixels for two-photon absorption TCT measurements (this test structure can also be used for standard TCT/edge-TCT measurements, check with I. Vila)

Test structure 5 Single pixels for sensor capacitance measurements

Test structure 6 …

Options

1. **Full mask set with a minimum of 12 engineering wafers**

Maximum design box dimensions:	25,840 mm x 32,480 mm(*)
Full mask set price:	55,780 €
12 engineering wafers:	33,540 €
NRE:	4,800 € (2 different substrate resistivities)
Total price:	94,120 €

2. **1x3 MLM with a minimum of 12 engineering wafers**

Maximum design box dimensions:	25,840 mm x 9,505 mm(*)
MLM 1x3 mask set:	31,500 €
12 MLM engineering wafers:	33,540 €
NRE:	4,800 € (2 different substrate resistivities)
NRE reticle set up:	7,500 €
Total price:	81,335 € (31,500 + 33,540 + 4,800 + 7,500 ≠ 81,335 €!?)

(*) Need to leave space for PCM structure (1,826 mm x 1,826 mm) inside the design box for foundry tests, and need to confirm with sub-contractor that such large devices can be handled