RD50 common project proposal: Thin film-based silicon sensors

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Motivation

- Radiation-hard silicon sensors are used in larger and larger areas
  - Full tracker replacements for HL-LHC, FCC trackers...
  - Calorimetry – see e.g. HGC and as high-granularity direct sensors
  - Timing detectors (e.g. HGTD)

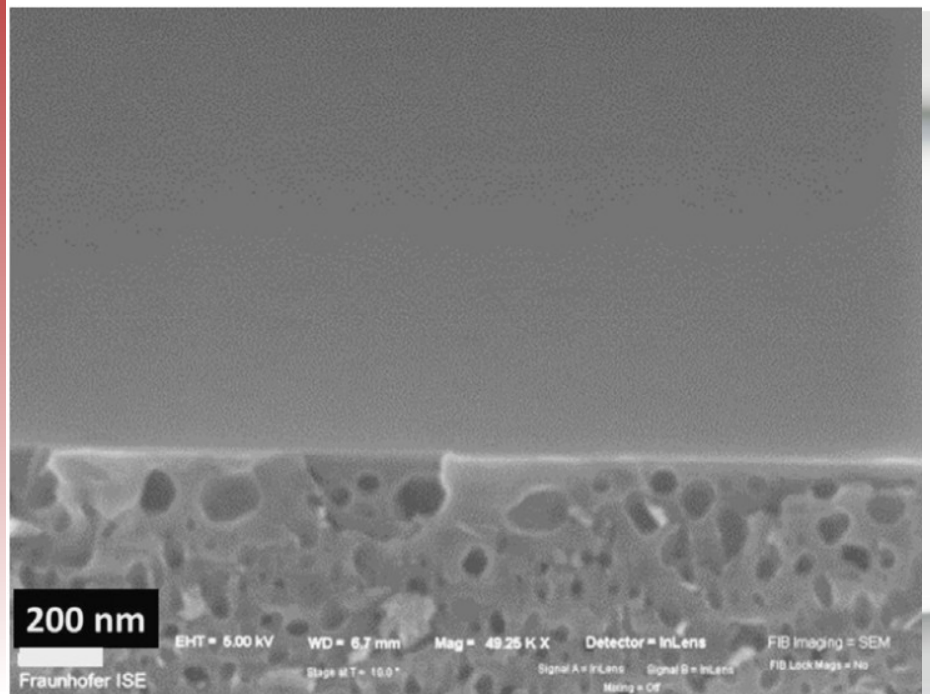
▶ cost-efficiency of increasing importance

  - visible in efforts to establish production on 8” wafers

- The solar cell industry also uses single-crystalline silicon
  - cost-efficiency requirements much more stringent due to competing substrates
    - poly-Si, amorphous Si, CdTe, GaAs, …
  - single-crystalline Si well-established → look for ways to reduce production cost for both substrate and processing
    - might benefit also particle sensors

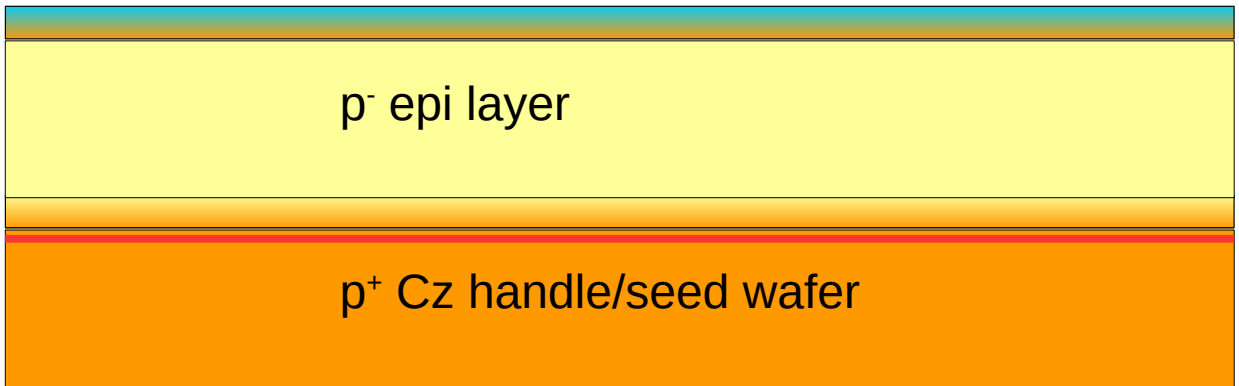
Silicon thin films

- Basic idea:
  - grow silicon epitaxially (and fast) to the desired thickness
    - no thinning/waste of silicon
    - free choice of doping (profile)
  - detach and recycle the handling wafer/seed
    - optional, for cost and inactive material reduction
    - possible thanks to porous silicon interface layer
    - process developed by Fraunhofer ISE, now commercialised by Nexwafe
      - cost goal: less than 1 EUR/substrate (156mm x 156mm)
      - currently: R&D substrates from Fraunhofer, soon (2017) Nexwafe pilot production



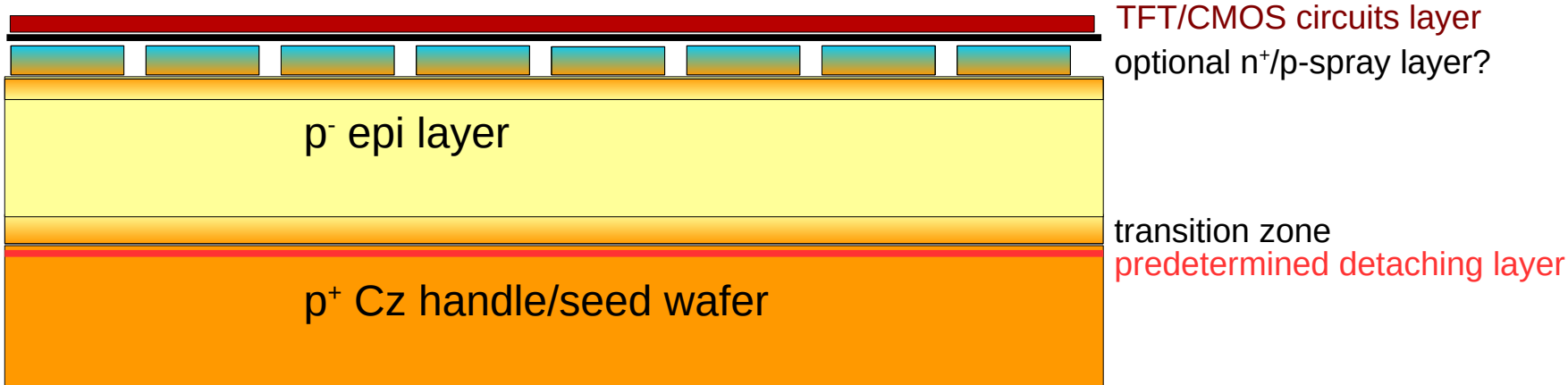
What to do with the substrate?

- Option 1: standard processing to assess sensor performance and radiation tolerance of a plain/"vanilla" epi substrate
  - inquired with CiS whether they would process such substrates
  - for comparability and cost reduction: could recycle existing mask set
  - frame conditions:
    - 4" wafers (from Fraunhofer ISE's research reactor, for flexible trials)
    - "few 10^{13} cm^{-3}" dopant concentrations achievable – some 100 Ohm*cm
      - might have to try with Fraunhofer for higher resistivities
      - but probably not really worth it: look at acceptor removal in HV-CMOS...
    - "thin" film up to 200 µm thick, but as thin as we like
    - p^+-"implant" could be made by epitaxial growth or diffusion from Cz handle wafer
    - could have additional layers → reduction of processing steps
      - n+ layer: etching away n^+-layer outside of pixels instead of implanting?
      - include "p-spray"-like layer underneath surface?



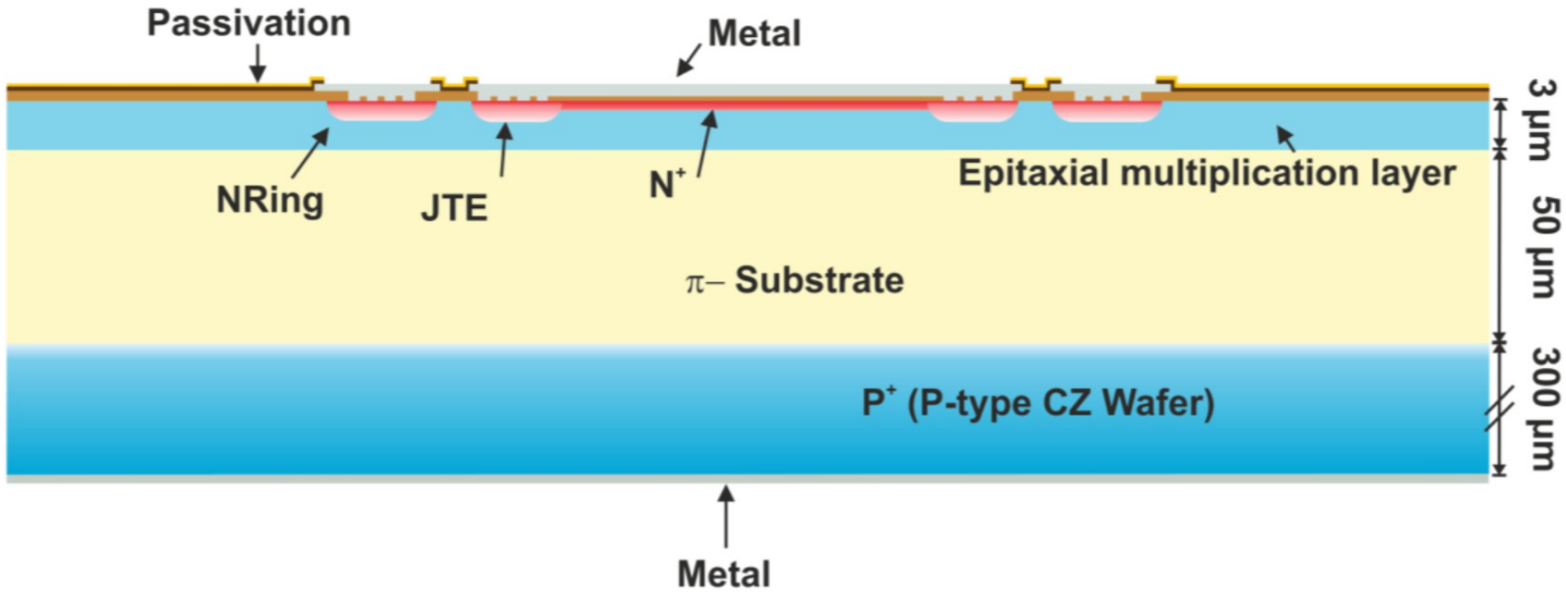
What to do with the substrate?

- Option 2: cheap substrate for active “CMOS”/TFT sensor?
  - in-pixel (or on-pixel) amplification might allow for thin substrates and/or capacitive coupling of readout chips
  - inquired with TU Dortmund (Electrical Engineering) whether they would want to try out to create CMOS amplifiers on such substrates in their CMOS production street
    - were quite interested in the material
    - existing mask set with test structures could be used
  - am working with collaborators in Mexico on creating classical “TFT” transistors on top of thin-film substrates
    - *very* cheap technology (think of TFT screens)
    - not clear whether fast/homogenious enough for sensor applications

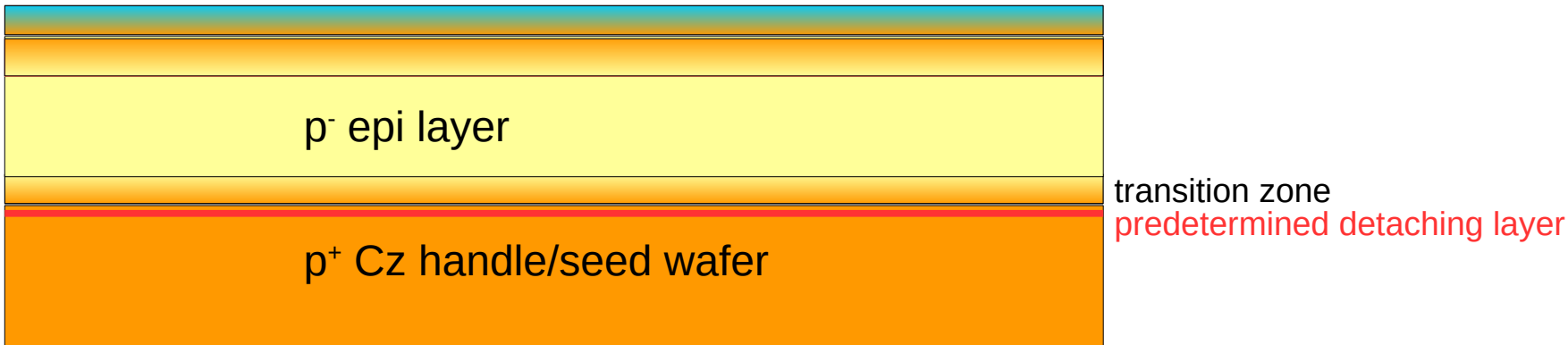


What to do with the substrate?

- Option 3: LGADs?
  - Talk by Maria del Mar Carulla Areste from CNM yesterday proposed an epi layer on top of 50 µm of high-resistivity silicon for LGADs:



- Compare this to this potential stack-up and ignore the colour scheme
  - could be grown instead of wafer-to-wafer bonding?



Proposal: Let's try this substrate option

- Long-term goal: Use Nexwafe's substrates
  - n-bulk pilot production expected in Q1 2017
  - p-bulk subsequently, probably Q4 2017
  - most likely only “homogenious” dopant concentrations
    - we are almost parasitic users...

- Short-term goal: Try things out with Fraunhofer-produced substrates
  - 4” wafers
  - flexible dopant profiles
  - unfortunately probably expensive: will depend on order size, thickness and dopant profile, but ~few 100 EUR/substrate likely

- Processing options:
  - CiS: classical hybrid pixel sensors
  - TU Dortmund: CMOS production street
  - TFT technology: ZnO transistor-based amplifier trials with Benemérita Universidad Autónoma de Puebla
  - LGADs? CNM? Anyone else?

Draft Proposal

- Joint procurement of substrates from Fraunhofer ISE:
  - 1 batch for CiS: ~18 wafers, divided between
    - 150 µm (ATLAS outer Pixel barrel layers) or 200 µm (ATLAS Pixel EC)?
    - 50 µm (innermost layers, has proven hard to produce)
  - 6 wafers for circuit trials at TU Dortmund, 4 wafers for TFT trials
    - thickness probably not relevant → go for cheapest option (thinnest?)
  - 2 wafers for substrate characterisation
    - SIMS, spreading resistance measuremens, …

- Naive costing estimate:
  - 30 wafers à 500 EUR/wafer (~worst case price): 15 kEUR
  - Sensor processing at CiS with existing mask set: ~10 kEUR
  - CMOS trials at TU Dortmund: Probably in-kind contribution if we provide the substrates
  - TFT trials: in-kind contribution from funded UK-Mexico project
  - LGAD production?
  - substrate characterisations: spreading resistance and SIMS: 2 kEUR?

- Initial discussions showed interest from several RD50 groups