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Implementation of the VMM ASIC in the Scalable Readout System

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In the context of the ATLAS New Small Wheel upgrade, a new frontend ASIC called VMM is developed. This chip will play a significant role in the readout of Micro-Pattern Gaseous Detectors not only in ATLAS, but also for other projects within the whole MPGD community and in particular for a detector for the macromolecular crystallography instrument NMX foreseen at the European Spallation Source (ESS).
The RD51 Collaboration has developed a multi-purpose and versatile readout system that can be scaled from a single laboratory detector to LHC-like experiments: The Scalable Readout System (SRS). Different frontend ASICs have been implemented in the SRS so far.

At the moment, the state of the art ASIC used by many groups (R&D for sPHENIX/EIC at the RHIC, SBS Back Tracker and PRad GEM detector at JLAB and detector upgrade R&D for LHC experiments) is the APV25. There is a strong interest of many groups using the SRS with the APV25, to upgrade their systems to the VMM. In several design iterations (VMM1, VMM2 and now VMM3), the capabilities of the VMM have been continuously extended. The VMM3 is intended to reach the final needs as defined in the specifications.

Within the BrightnESS project, the VMM is implemented in the SRS to read out a prototype GEM based neutron detector for the NMX instrument. New FPGA firmware, dedicated hardware and software is under development.

In the laboratory of the Gaseous Detector Development group at CERN we are operating several small scale versions of the final prototype to improve the detectors themselves and test the readout system and the data acquisition software. In addition, test beams with neutrons at the JEEP II reactor of IFE at Kjeller, Norway have been carried out. The current status of the developments, capabilities of the SRS based VMM readout and latest measurement results will be presented.

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