Simulation of the ATLAS New Small Wheel (NSW) System

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LHC upgrade overview

We are here now!

Current Small Wheel be replaced by the New Small Wheel

Nominal luminosity = $10^{34}$ cm$^{-2}$s$^{-1}$

Mean number of interactions per bunch crossing $\mu$: up to 160

$\mu$: up to 80

2 x nominal luminosity

2*10$^{34}$ cm$^{-2}$s$^{-1}$
Current ATLAS Muon System

- Thin-gap chambers (TGC)
- Cathode strip chambers (CSC)
- Barrel toroid
- End-cap toroid
- Resistive-plate chambers (RPC)
- Small Wheel
- Monitored drift tubes (MDT)

Tracker
Trigger
The current Small Wheel is planned to be replaced by NSW during the LHC Long Shutdown 2.

Non-IP originating background could be eliminated by $\Delta \theta > 15$ mrad trigger selection. (Case C in the upper left figure.)

Effectively reduce the trigger rate, and maintain a high efficiency at a high rate environment.
ATLAS NSW Technologies

Two technologies: **sTGC** (Small-strip Thin Gas Chamber) and **MM** (resistive strip MicroMegas) are used for both trackers and triggers.

- **sTGC**: primary *trigger*
- **MM**: primary *precision tracker*

Today's focus!

Each sector contains 8 sTGC layers and 8 MM layers.

Both sTGC and MM are used for triggering and tracking, which will have *robust redundancy*. 
MM Trigger Electronics Path

- **VMM ASIC**: Readout and control (not for trigger)
- **ART ASIC**: Address of real time
- **ART Data Driver Card (ADDC)**
- **FPGA on Trigger Processor (TP)**

In experimental hall:
- 8VMM ASICs per MMFE-8
- 2 ART ASICs per ADDC, connected to trigger processor

In USA15 cavern:
- Optical link (GBTx)
MM Trigger Electronics Path

VMM ASIC

- 64 channels / VMM
- Select 1 out of 64 channels, output strip address only.

In experimental hall

- ART Data Driver Card (ADDC)
- Optical link (GBTx)
- ART ASIC

In USA15 cavern

- Trigger Processor
- FPGA on Trigger Processor (TP)

- 8 layer hit coincidence. (Look for hits every 50 ns.)
- Reconstruct track segment and angle.
- Maximum output 8 track segments per sector every 25 ns.
MM readout scheme at VMM

- **Challenge:** large amount of strips (~2M strips), impossible to output all the data. → **NEED REDUCTION!**

- **Solution:** only output the strip address of the fastest channel readout out of 64-channels (per VMM).
  - Only 1 output out of 64-channels
    - Fastest readout corresponding to the shortest drift distance.
    - A good enough approximation for hit position due to the fine strip pitch (~0.4mm).
  - Only output the strip address
    - Information on charge and timing are not output.

>>> ART data: address in real time
Drift timing distribution on MM trigger signal

- Simulated VMM ART *signal for single muon* (100 GeV pT, flat distribution in η and φ).
- Counting 2 bunch crossing (50 ns) will give a promising efficiency.
- Using a small charge threshold → optimum results.
MM Trigger Electronics Path

**VMM ASIC**

- 64 channels / VMM
- Select 1 out of 64 channels, output strip address only.

**ART Data Driver Card (ADDC)**

- Aggregate addresses from 32 VMMs and choose 8.

**ART ASIC**

- 8 layer hit coincidence. (Look for hits every 50 ns.)
- Reconstruct track segment and angle.
- Maximum output 8 track segments per sector every 25 ns.

**FPGA on Trigger Processor (TP)**

- In experimental hall
- In USA15 cavern

**To Sector Logic**
MM Trigger Electronics Path

- **VMM ASIC**
  - Readout and control (not for trigger)
  - 64 channels / VMM
  - Select 1 out of 64 channels, output strip address only.

- **ART Data Driver Card (ADDC)**
  - Aggregate addresses from 32 VMMs and choose 8.

- **ART ASIC**
  - 8 layer hit coincidence. (Look for hits every 50 ns.)
  - Reconstruct track segment and angle.
  - Maximum output 8 track segments per sector every 25 ns.

- **FPGA on Trigger Processor (TP)**

- **In experimental hall**
  - Optical link (GBTx)
  - Trigger Processor

- **In USA15 cavern**
  - To Sector Logic

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Some MM planes have a slight stereo tilt (1.5°) for azimuthal angle $\phi$ measurement.

Convert hits to slopes. Find the track segment aligned to a slope road.

Coincidence thresholds will effect the trigger efficiency.

- **4X4UV:** 4 out of 4 x layers + 4 out of 4 u or v layers → *expect lowest efficiency.*
- **3X3UV:** 3 out of 4 x layers + 3 out of 4 u or v layers.
- **2X2UV:** 2 out of 4 x layers + 2 out of 4 u or v layers.
64 channels / VMM

Select 1 out of 64 channels, output strip address only.

8 layer hit coincidence. (Look for hits every 50 ns.)

Reconstruct track segment and angle.

Maximum output 8 track segments per sector every 25 ns.
MM Trigger Algorithm: Angle Reconstruction

- Calculation of $(\eta, \varphi)$ and $\Delta \theta$ for candidates after hit coincidence.

- $\theta_x^{\text{local}}$ calculated using a least square fit of $X$ hits with analytic solution.

- $\theta_x^{\text{global}}$ reconstructed by connecting IP and the average of registered hits.

Output:

- Hit position $(\eta, \varphi)$:
  - $\Delta \theta = |\theta_x^{\text{local}} - \theta_x^{\text{global}}|

  - Defined as angular derivation of MM track with respect to an infinite momentum track from IP.

  - Cut at $\Delta \theta > 15 \text{ mrad}$ to eliminate non-IP pointing background.

- $\eta$: derived from $\theta_x^{\text{global}}$

- $\varphi$: derived from stereo slopes using a look-up table.
MM Angular Resolution Performance

Δθ requirement: 1 mrad

φ requirement: 20 mrad

Residual = |truth - reconstructed|

Consider hit coincidence threshold of 3X3UV, 160 events per bunch crossing.

Gaussian fit on the residual distributions.

η requirement: $5 \times 10^{-3}$

Good performance compared to the requirement.
Track segment finding efficiency as a function of $\mu$.

- Considering 3 different LHC scenarios.
- Compare the efficiency requiring different hit coincidences.
  - 4X4UV: lowest efficiency as expected.
  - 3X3UV & 2X2UV: get 99% efficiency.

Track segment finding efficiency as a function of $\eta$

- 3 different LHC scenarios and 2 different hit coincidence thresholds (2X2UV and 3X3UV) are considered.
- Combining all cases, the efficiency is about 99%.
MM Trigger Electronics Path

- VMM ASIC
  - 64 channels / VMM
  - Select 1 out of 64 channels, output strip address only.

- ART ASIC
  - Aggregate addresses from 32 VMMs and choose 8.

- ART Data Driver Card (ADDC)
  - Optical link (GBTx)

- Trigger Processor
  - FPGA on Trigger Processor (TP)
  - 8 layer hit coincidence. (Look for hits every 50 ns.)
  - Reconstruct track segment and angle.
  - Maximum output 8 track segments per sector every 25 ns.

In experimental hall

In USA15 cavern

To Sector Logic
Average rate of track segments

- Average rate of track segments in one sector

  - 3 different LHC scenarios and 3 different hit coincidence thresholds are considered.

  - The occupancy is small enough the bandwidth limitation, which is at most 8 track segments per bunch crossing.
The ATLAS New Small Wheel is motivated to improve the tracking efficiency and reduce the fake trigger rate in future LHC runs.

The design of the electronics for both sTGC and MM has been almost completed.

The trigger algorithms have been developed and currently being commissioned in hardware.

The simulations show the good performance at efficiency and resolutions.

- Different numbers of interactions per bunch crossing has been considered.
- Need to implement the cavern background of neutral particles.

The simulation is for ideal case, now taking data to get a more realistic approach.

We are looking forward the installation of the NSW in 2019!
Backups
NSW Terminologies

- **Sector**: 1 Sector = 1 Station
- **Chamber**: 1 Station = 2 sTGC Wedges + 1 MM Chamber (in z-direction)
- **Wedge (Supermodule)**: 1 MM Chamber = 2 MM Wedges (in z-direction)
- **Module**: 1 MM Wedge = 4 MM Modules (in r-direction)
- **Multiple**: 1 MM Module = 1 MM Multiplet (in r-direction)
- **Plane**: 1 MM Multiplet = 4 MM Planes (in z-direction)

Diagram:

- 1 Sector -> 2 sTGC Wedges + 1 MM Chamber
- 1 Station -> 2 sTGC Wedges + 1 MM Chamber
- 1 MM Chamber -> 2 MM Wedges (in z-direction)
- 1 MM Wedge -> 4 MM Modules (in r-direction)
- 1 MM Module -> 1 MM Multiplet (in r-direction)
- 1 MM Multiplet -> 4 MM Planes (in z-direction)
VMM ASIC operates for both sTGC and MM
## MM ADDC Output Data Format

<table>
<thead>
<tr>
<th>0b1010</th>
<th>BCID</th>
<th>ERR_FLAGS</th>
<th>HIT_LIST</th>
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NSW Trigger Output Data Format

<table>
<thead>
<tr>
<th>Field:</th>
<th>sTGC type</th>
<th>MM type</th>
<th>$\Delta\theta$ (mrad)</th>
<th>$\phi$ index</th>
<th>$R$ index</th>
<th>spare</th>
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<tbody>
<tr>
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<td>2</td>
<td>5</td>
<td>6</td>
<td>8</td>
<td>1</td>
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</table>

Table 5: Data format of the output of the trigger processor sent to the Sector Logic. Format of a track vector candidate from the NSW (24-bits/track vector). The sTGC and MM type information can encode the quality of the candidate.
Phi Bias Explain

Face up

Drift Electrode
E Field
Micromesh

Overlap these two layers,
Reconstructed phi shifts.

Face down

Drift Electrode
E Field
Micromesh

Face up
Signal comes from Lower

Face down
Signal comes from Upper

φ shifts for minus

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