

Simulation of the ATLAS New Small Wheel (NSW) System

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on behalf of the **ATLAS Muon Collaboration**

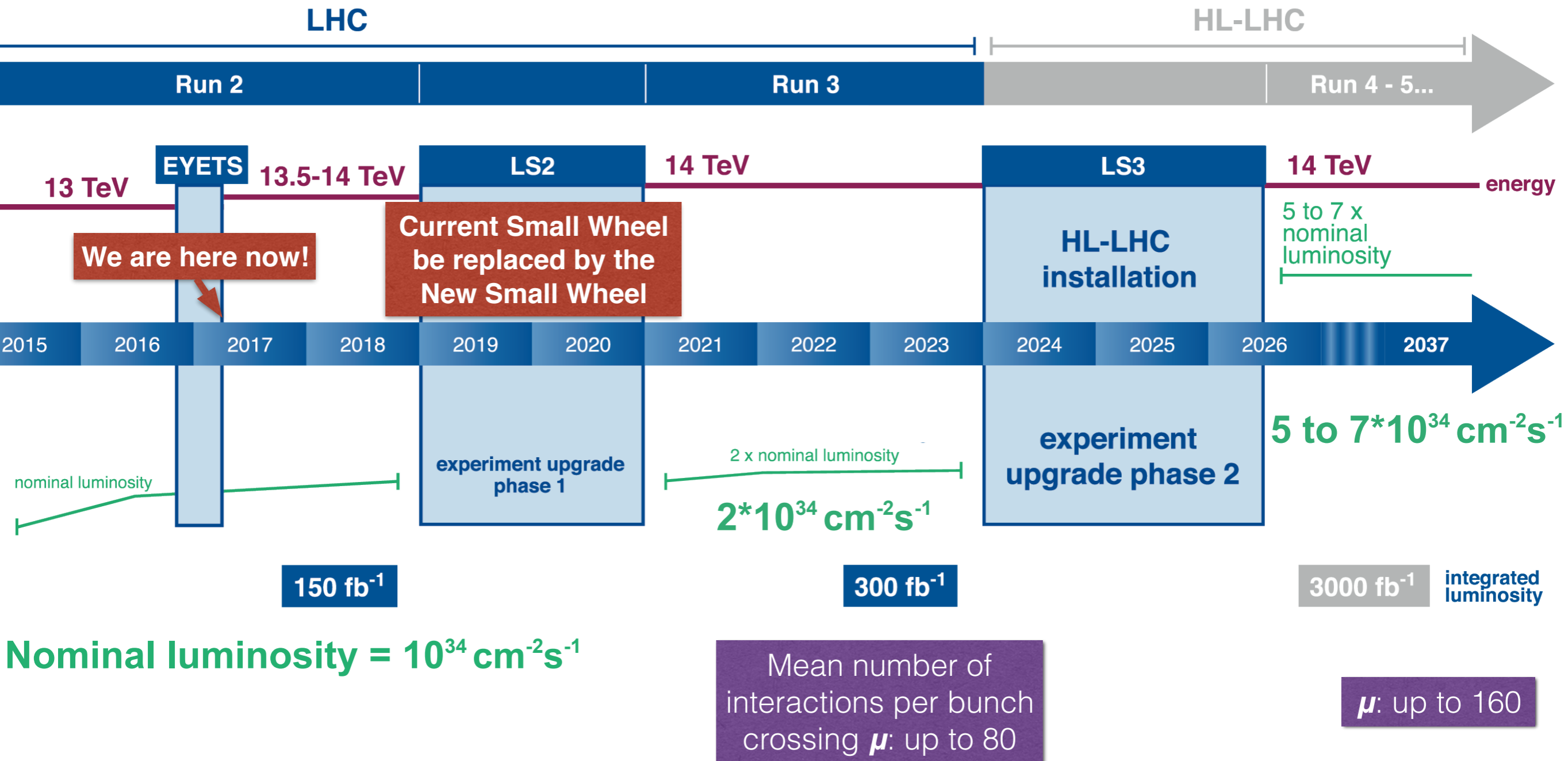
5th International Conference on Micro-Pattern Gas Detectors
and
RD51 Collaboration Meeting

Temple University, Philadelphia, USA
May 22-26, 2017





LHC upgrade overview

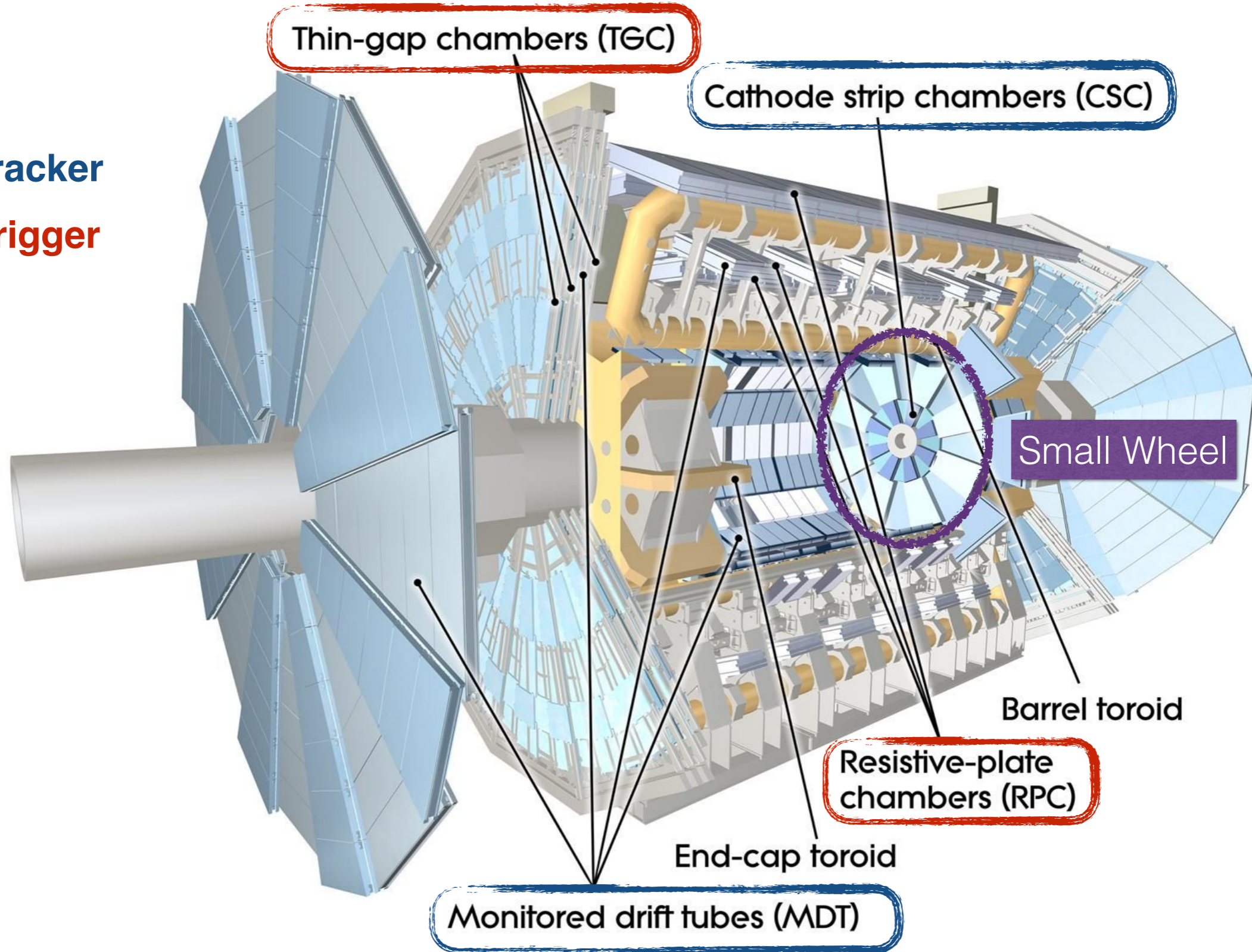




Current ATLAS Muon System

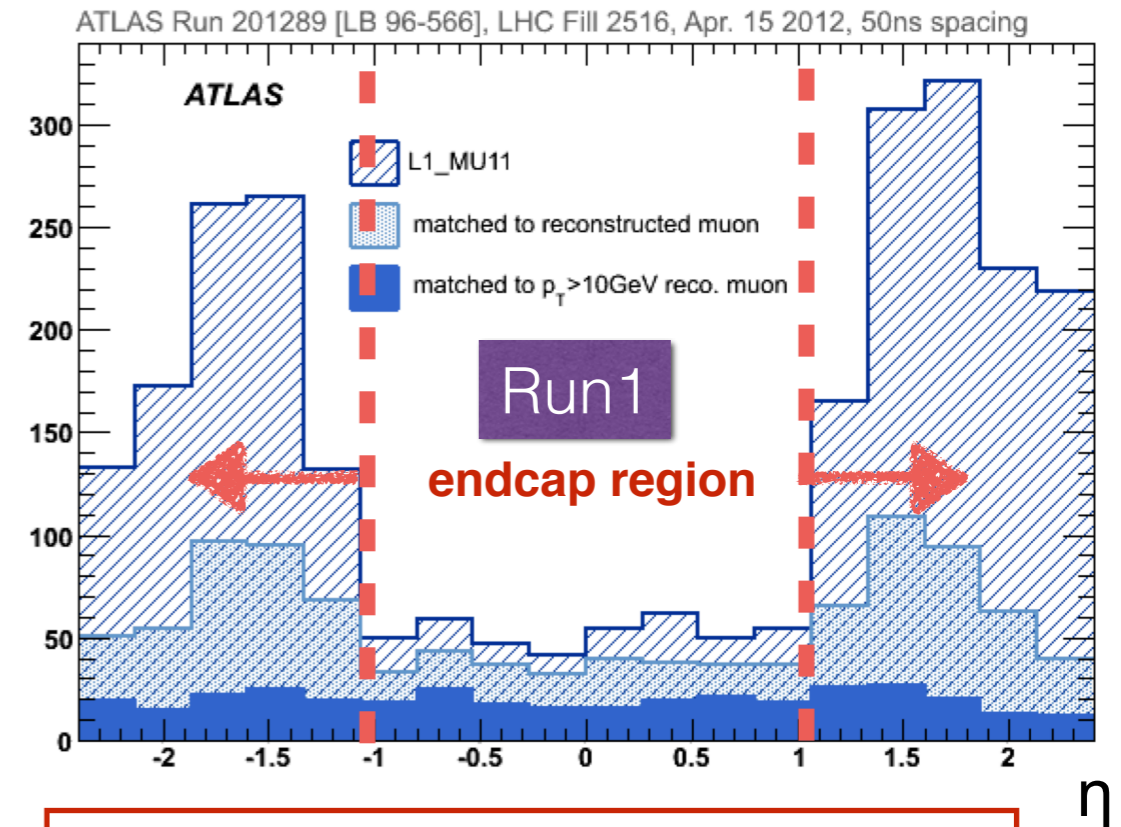
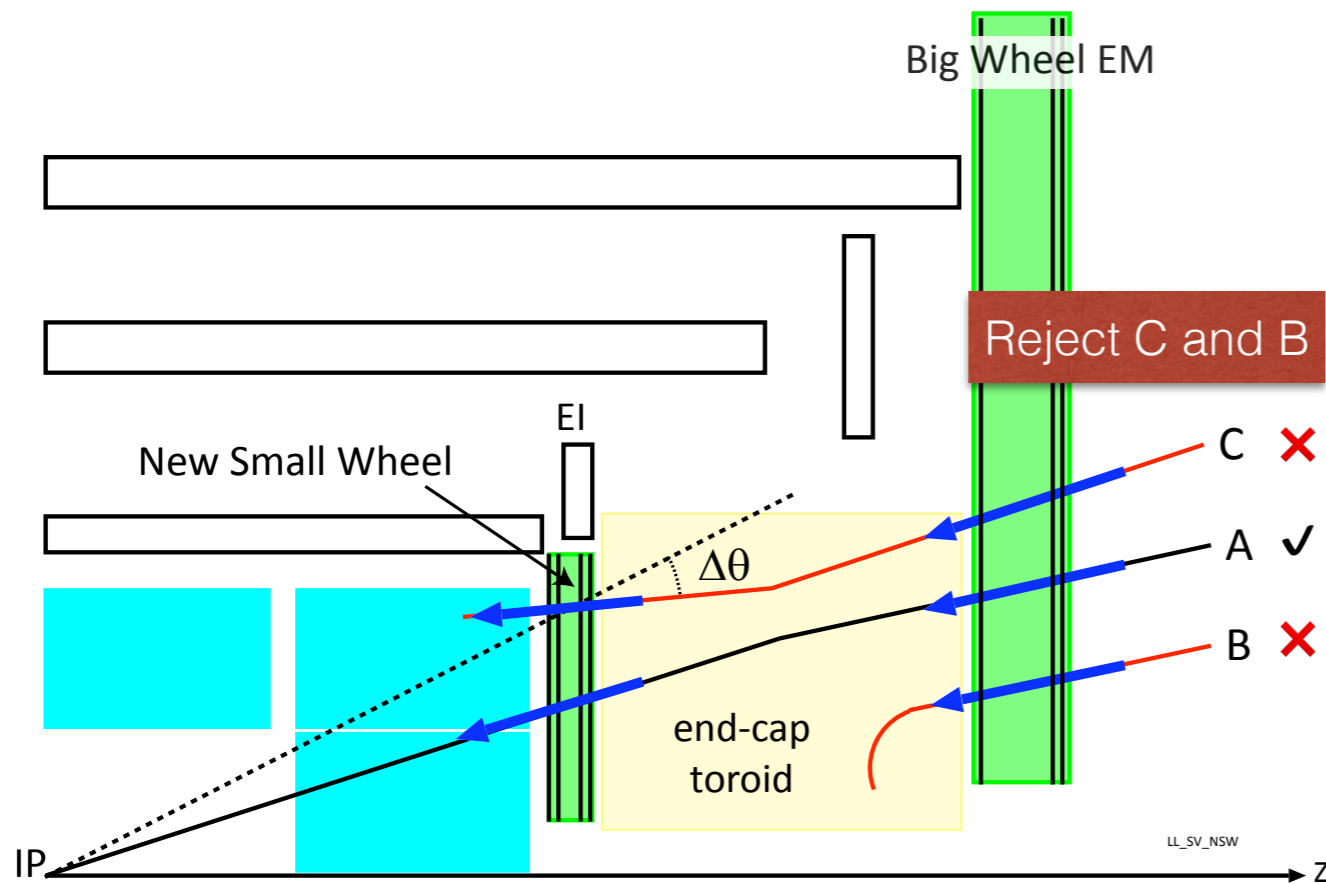


-  Tracker
-  Trigger



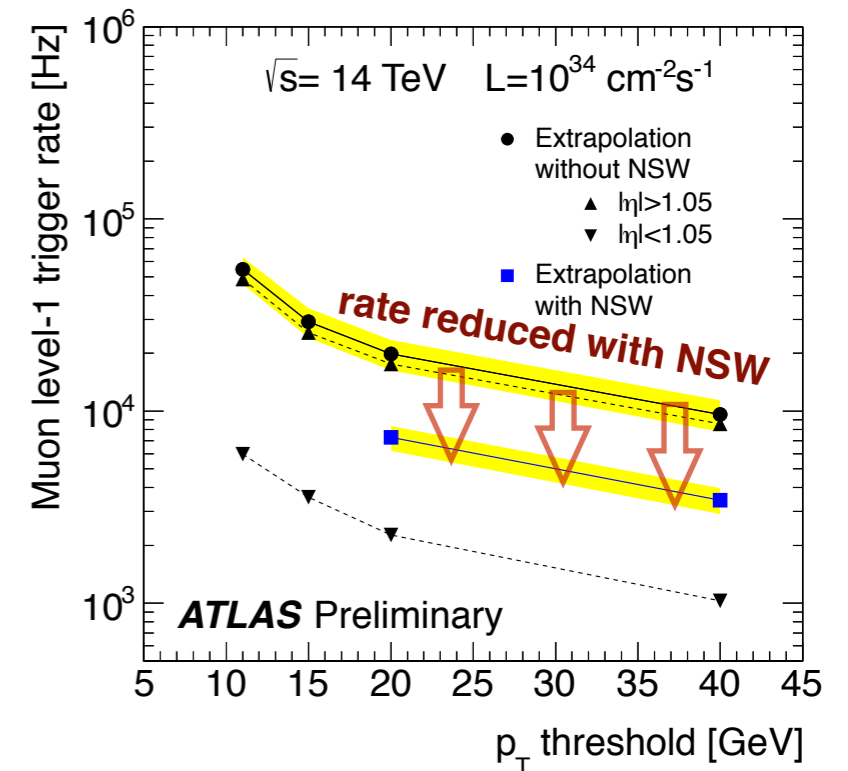


ATLAS New Small Wheel Upgrade



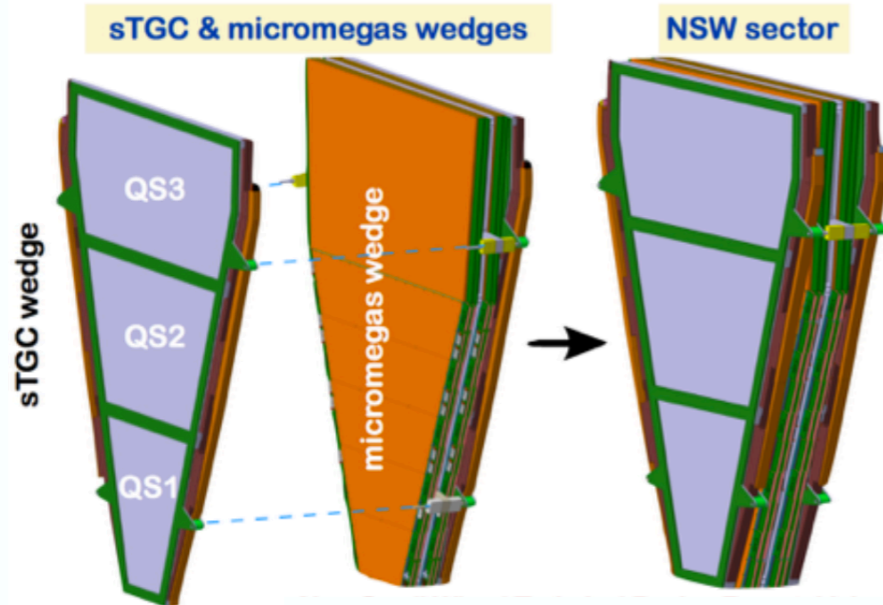
Large amount of background and high trigger rate at end-cap region!

- The current Small Wheel is planned to be replaced by NSW during the LHC Long Shutdown 2.
- Non-IP originating background could be eliminated by $\Delta\theta > 15 \text{ mrad}$ trigger selection. (Case C in the upper left figure.)
- Effectively reduce the trigger rate, and maintain a high efficiency at a high rate environment.





ATLAS NSW Technologies

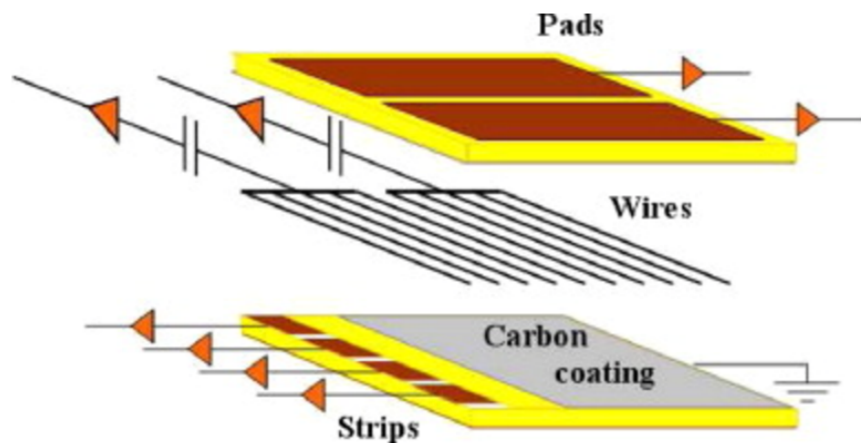


Two technologies: **sTGC** (Small-strip Thin Gas Chamber) and **MM** (resistive strip MicroMegas) are used for both trackers and triggers.

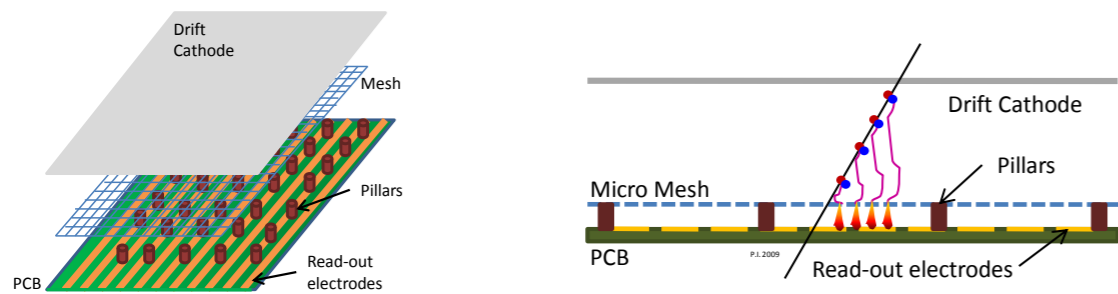
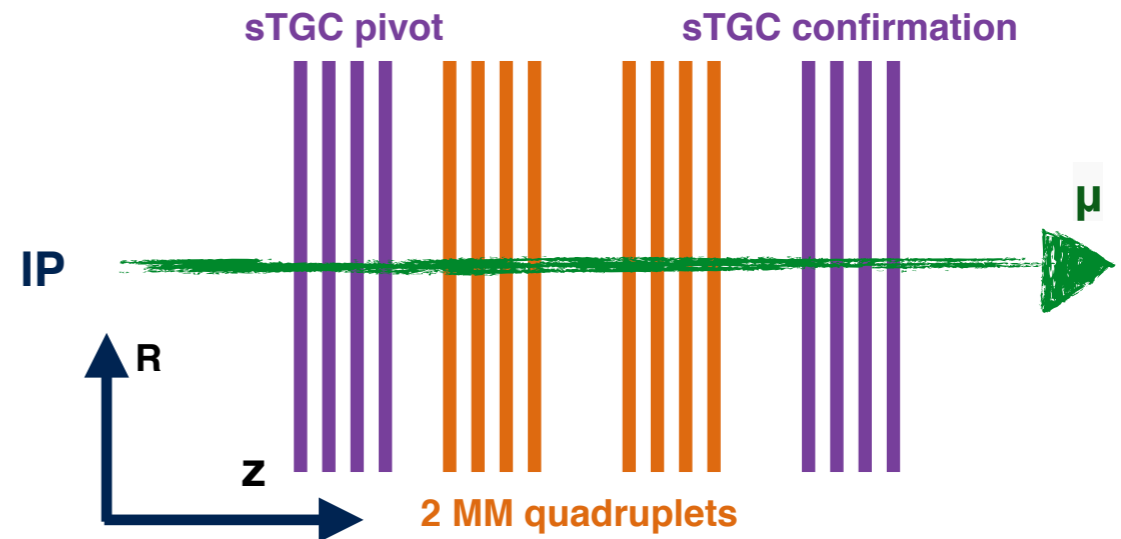
▶ **sTGC**: primary *trigger*

▶ **MM**: primary *precision tracker*

Today's focus!



Sketch of the layout of a **sTGC** detector



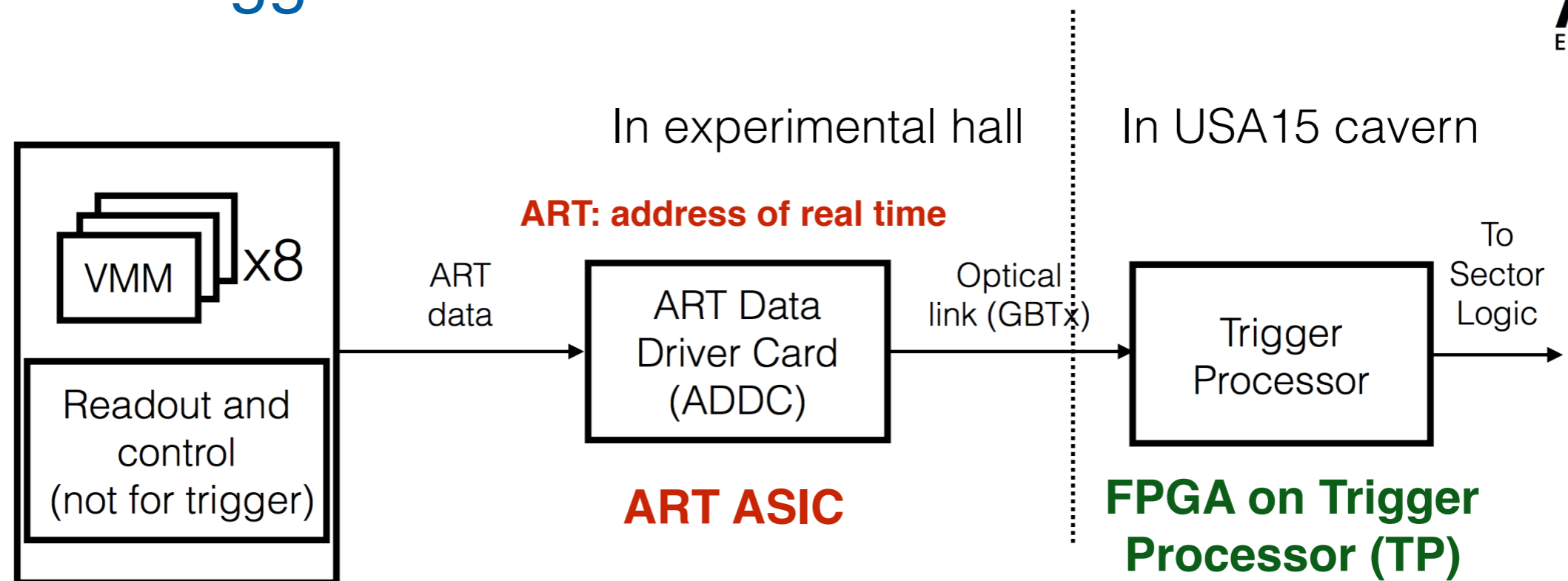
Sketch of the layout of a **MM** detector

Each sector contains 8 **sTGC** layers and 8 **MM** layers.

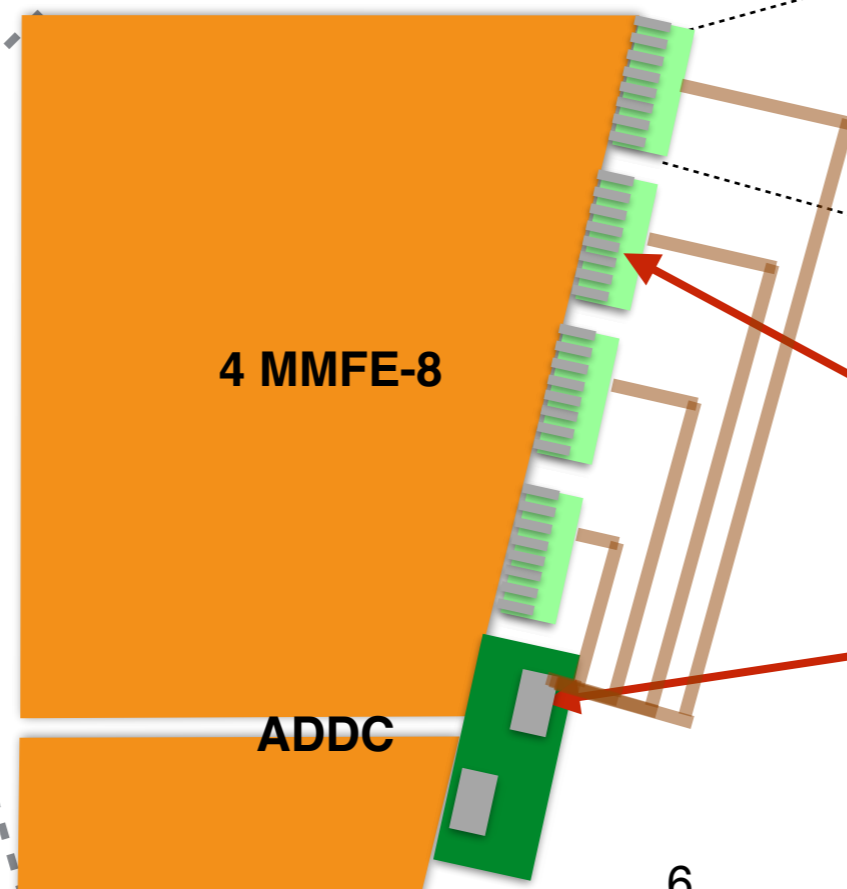
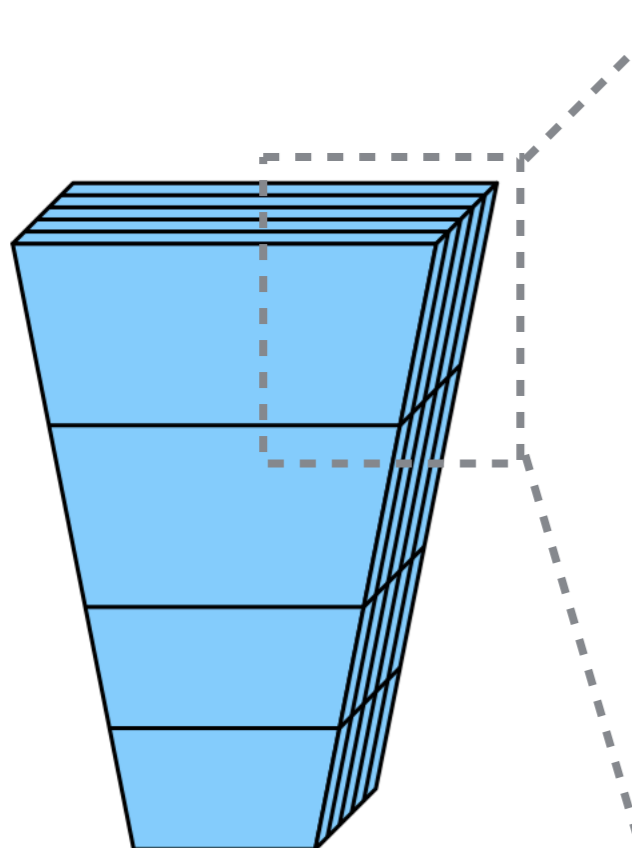
* Both **sTGC** and **MM** are used for triggering and tracking, which will have **robust redundancy**.



MM Trigger Electronics Path



VMM ASIC



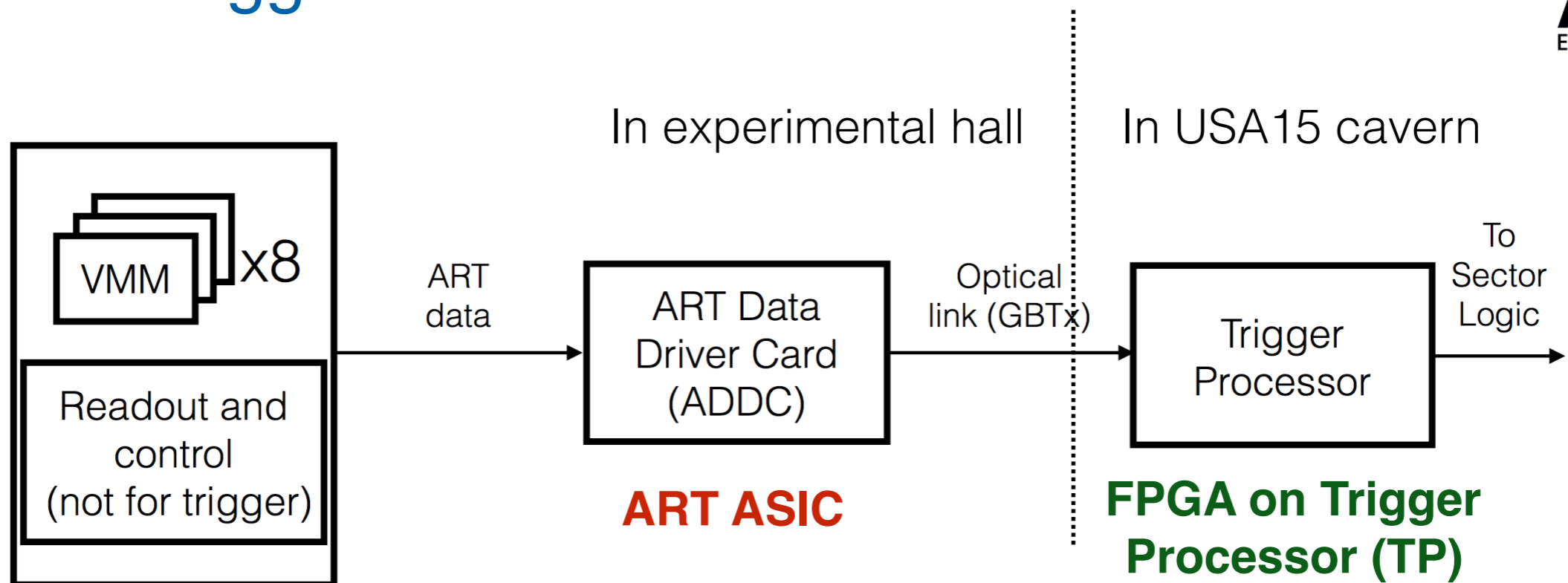
MMFE-8

8 VMM ASICs per MMFE-8

2 ART ASICs per ADDC, connected to trigger processor



MM Trigger Electronics Path



VMM ASIC

- ▶ 64 channels / VMM

▶ Select 1 out of 64 channels, output strip address only.

ART ASIC

- ▶ Aggregate addresses from 32 VMMs and choose 8.

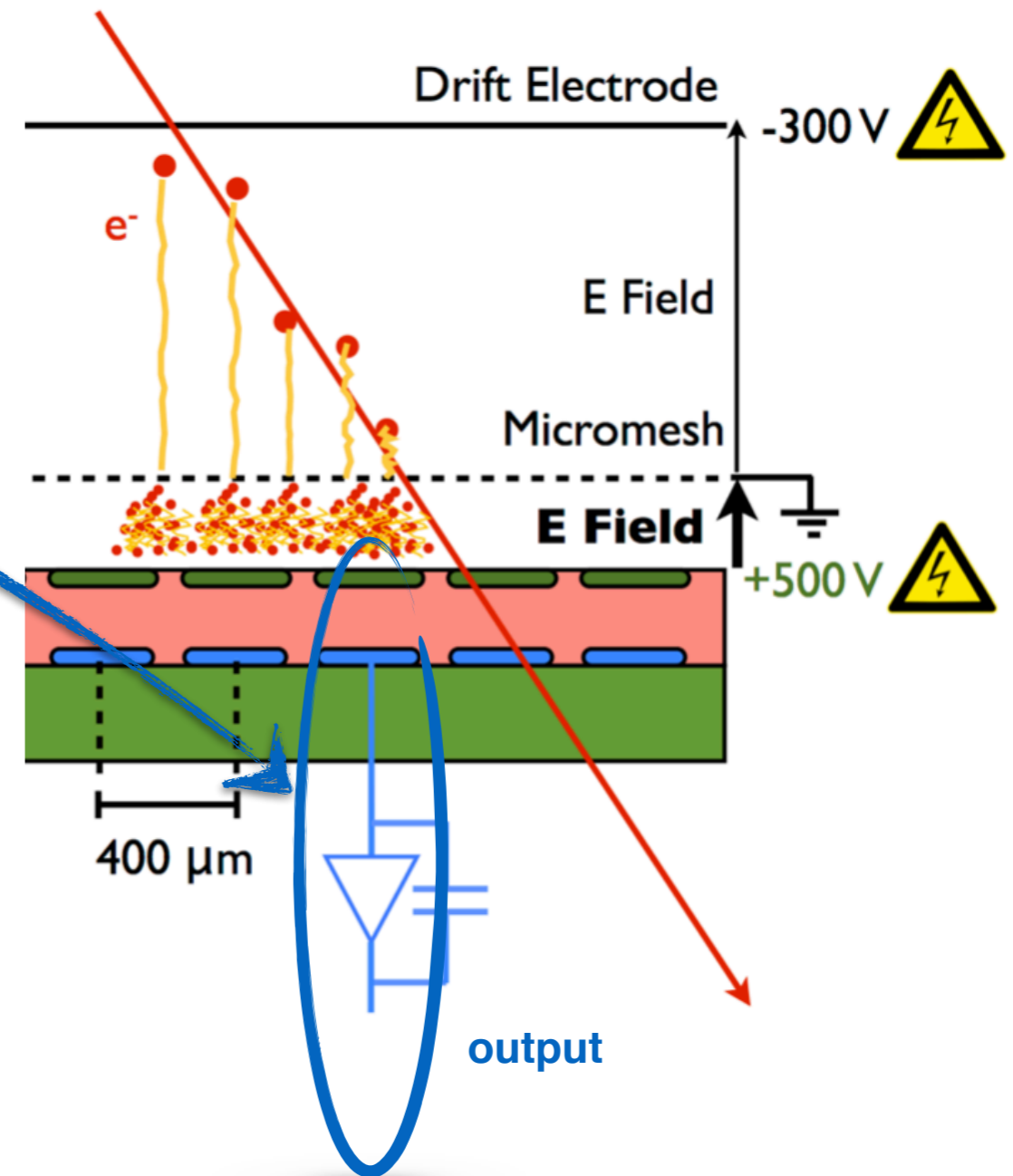
FPGA on Trigger Processor (TP)

- ▶ 8 layer hit coincidence. (Look for hits every 50 ns.)
- ▶ Reconstruct track segment and angle.
- ▶ Maximum output 8 track segments per sector every 25 ns.



MM readout scheme at VMM

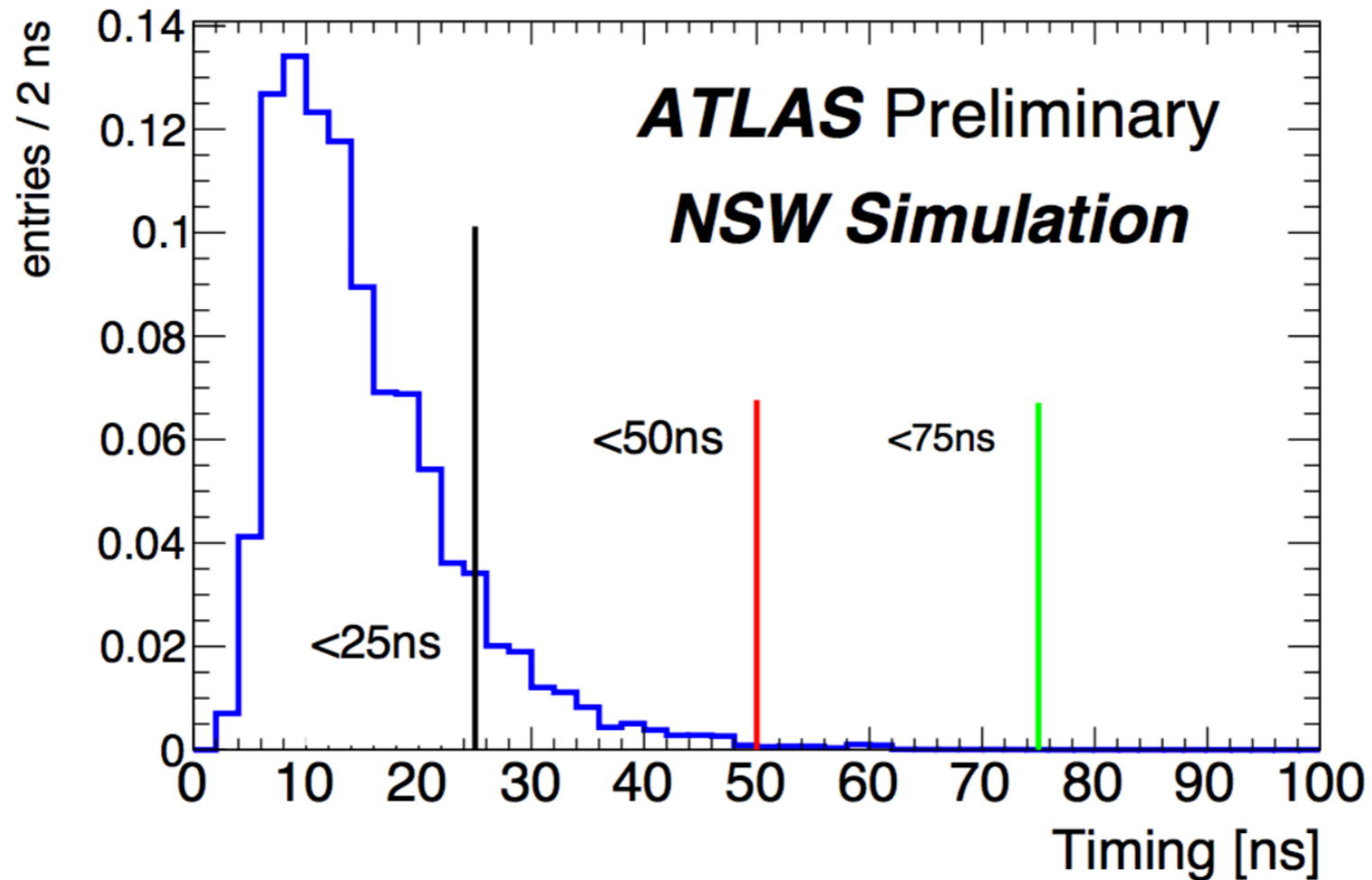
- **Challenge:** large amount of strips (~2M strips), impossible to output all the data. → **NEED REDUCTION!**
- **Solution:** only output the strip address of the fastest channel readout out of 64-channels (per VMM).
 - Only 1 output out of 64-channels
 - ▶ Fastest readout corresponding to the shortest drift distance.
 - ▶ A good enough approximation for hit position due to the fine strip pitch (~0.4mm).
 - Only output the strip address
 - ▶ Information on charge and timing are not output.



>>> ART data: address in real time



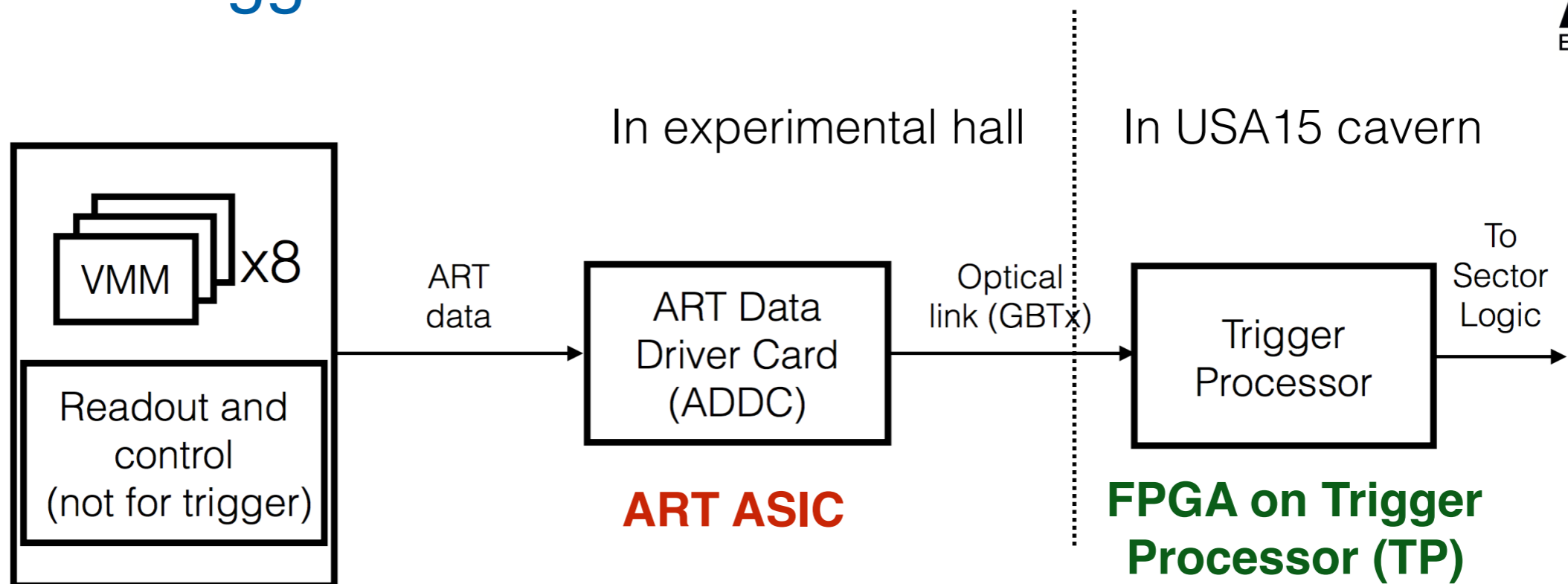
VMM Timing Simulation Performance



- Drift timing distribution on MM trigger signal
 - Simulated VMM ART **signal for single muon** (100 GeV pT, flat distribution in η and ϕ).
 - Counting 2 bunch crossing (50 ns) will give a promising efficiency.
 - Using a small charge threshold → optimum results.



MM Trigger Electronics Path



VMM ASIC

- ▶ 64 channels / VMM
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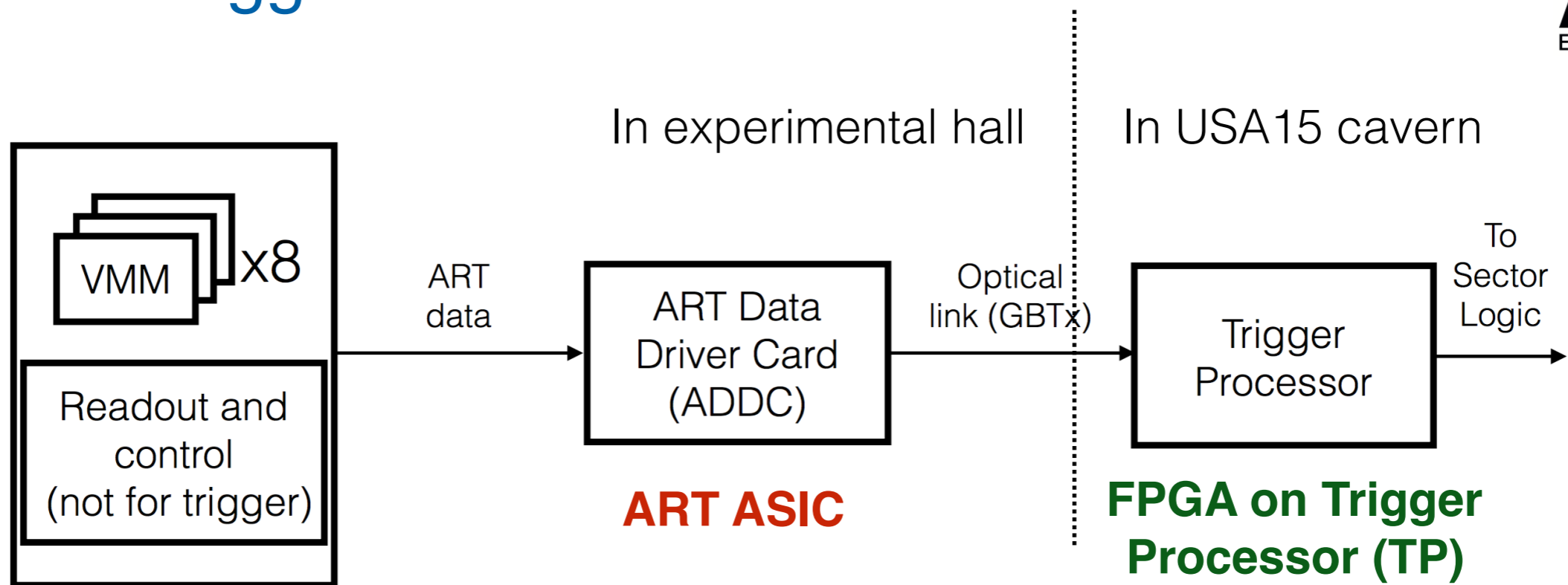
▶ Aggregate addresses from 32 VMMs and choose 8.

FPGA on Trigger Processor (TP)

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MM Trigger Electronics Path



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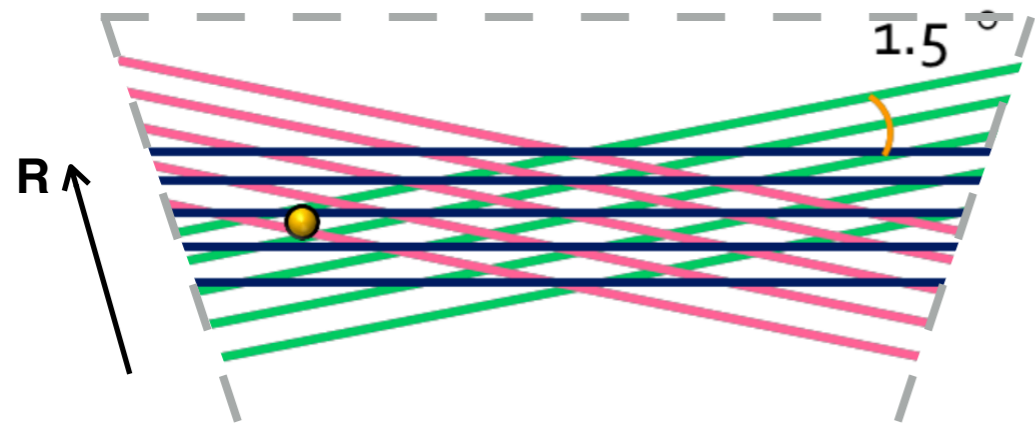
- ▶ 8 layer hit coincidence. (Look for hits every 50 ns.)

- ▶ Reconstruct track segment and angle.

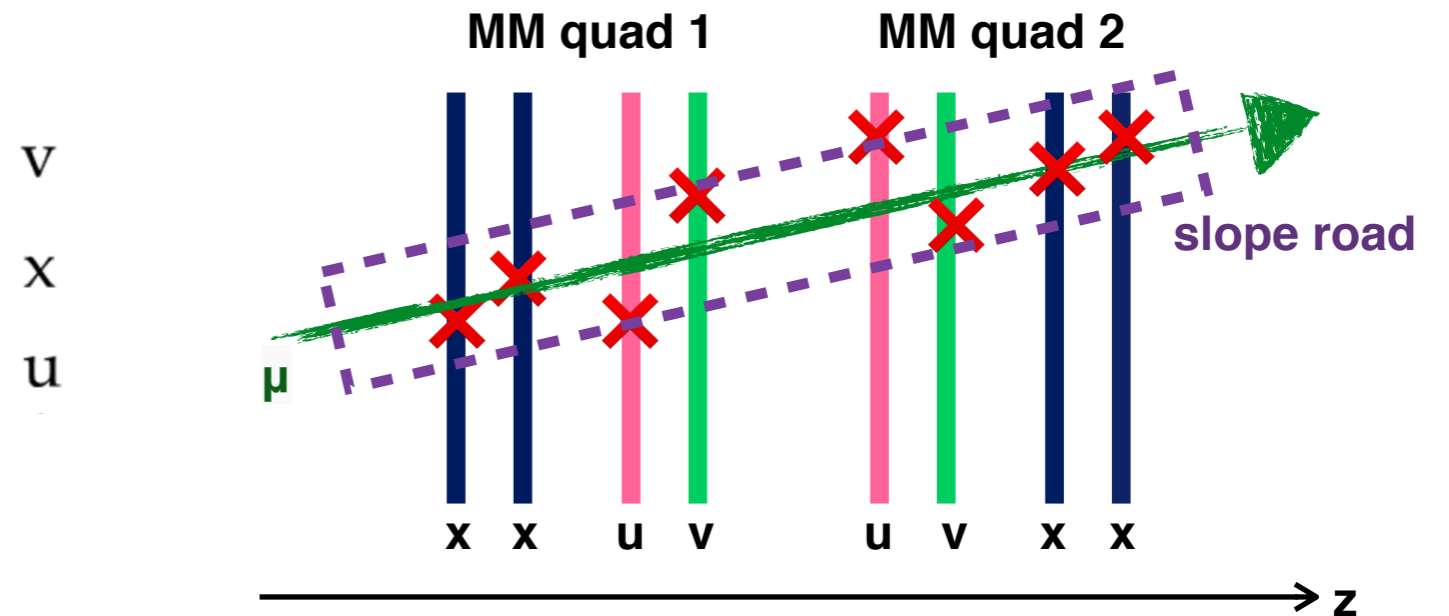
- ▶ Maximum output 8 track segments per sector every 25 ns.



MM Trigger Algorithm: Track Segment Finding



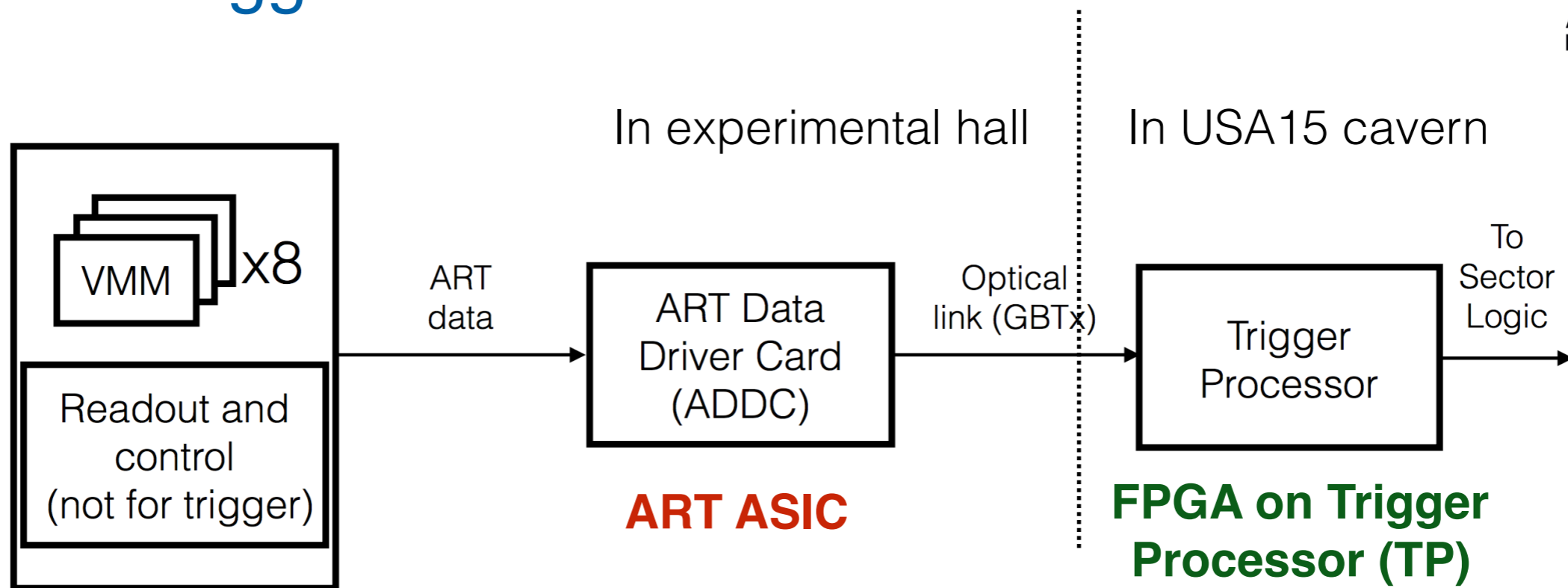
x: horizontal strip (2 plans per quad.)
u,v: stereo strip (1 each per quad.)



- Some MM planes have a slight stereo tilt (1.5°) for azimuthal angle φ measurement.
- Convert hits to slopes. Find the track segment aligned to a slope road.
- Coincidence thresholds will effect the trigger efficiency.
 - 4X4UV: 4 out of 4 x layers + 4 out of 4 u or v layers \rightarrow *expect lowest efficiency.*
 - 3X3UV: 3 out of 4 x layers + 3 out of 4 u or v layers.
 - 2X2UV: 2 out of 4 x layers + 2 out of 4 u or v layers.



MM Trigger Electronics Path



- ▶ 64 channels / VMM
- ▶ Select 1 out of 64 channels, output strip address only.

- ▶ Aggregate addresses from 32 VMMs and choose 8.

- ▶ 8 layer hit coincidence. (Look for hits every 50 ns.)

▶ Reconstruct track segment and angle.

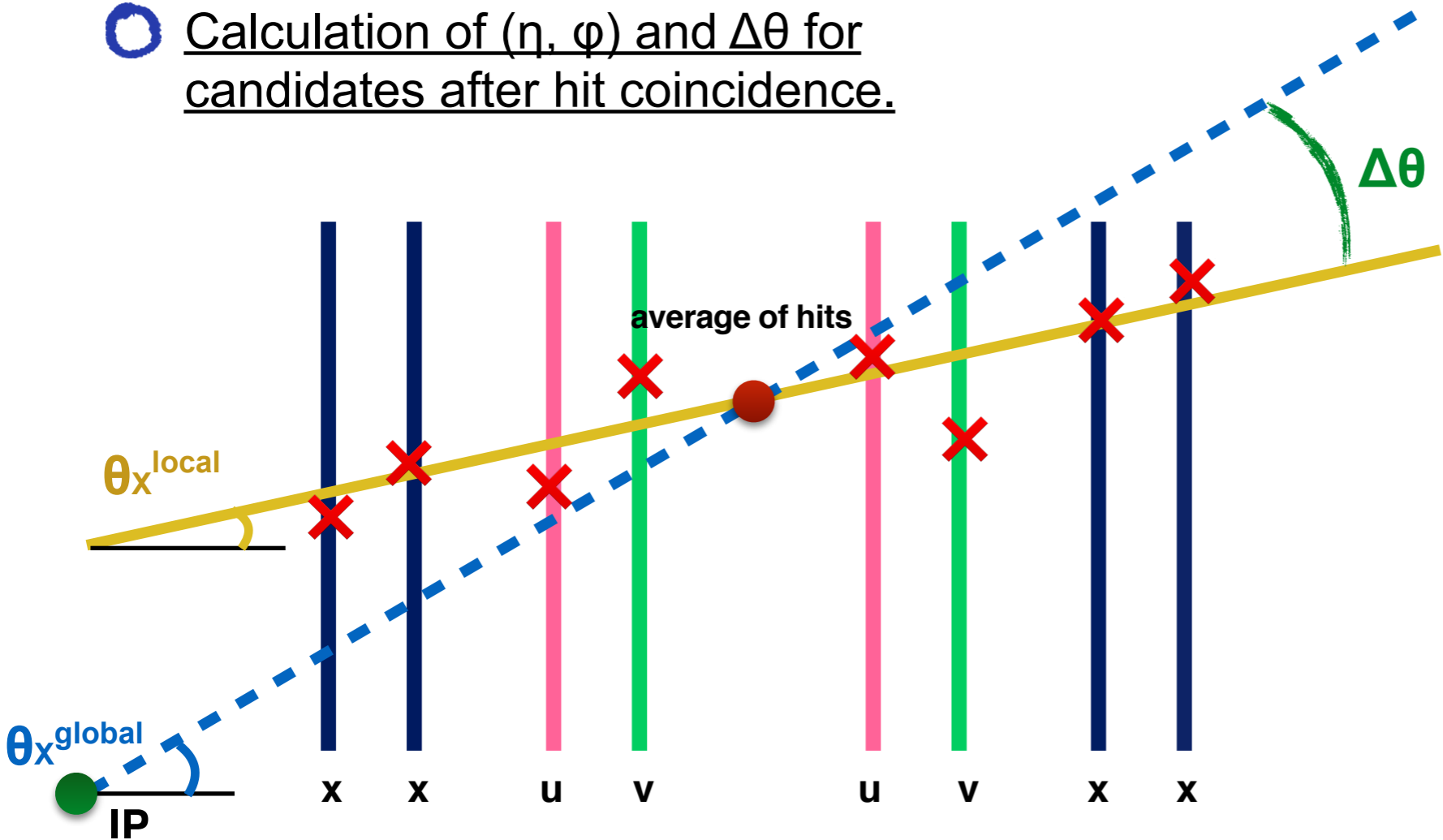
- ▶ Maximum output 8 track segments per sector every 25 ns.



MM Trigger Algorithm: Angle Reconstruction



- Calculation of (η, φ) and $\Delta\theta$ for candidates after hit coincidence.



- θ_x^{local} calculated using a least square fit of X hits with analytic solution.
- θ_x^{global} reconstructed by connecting IP and the average of registered hits.

○ Output:

□ Hit position (η, φ) :

□ $\Delta\theta = |\theta_x^{local} - \theta_x^{global}|$

◆ Defined as angular derivation of MM track with respect to an infinite momentum track from IP.

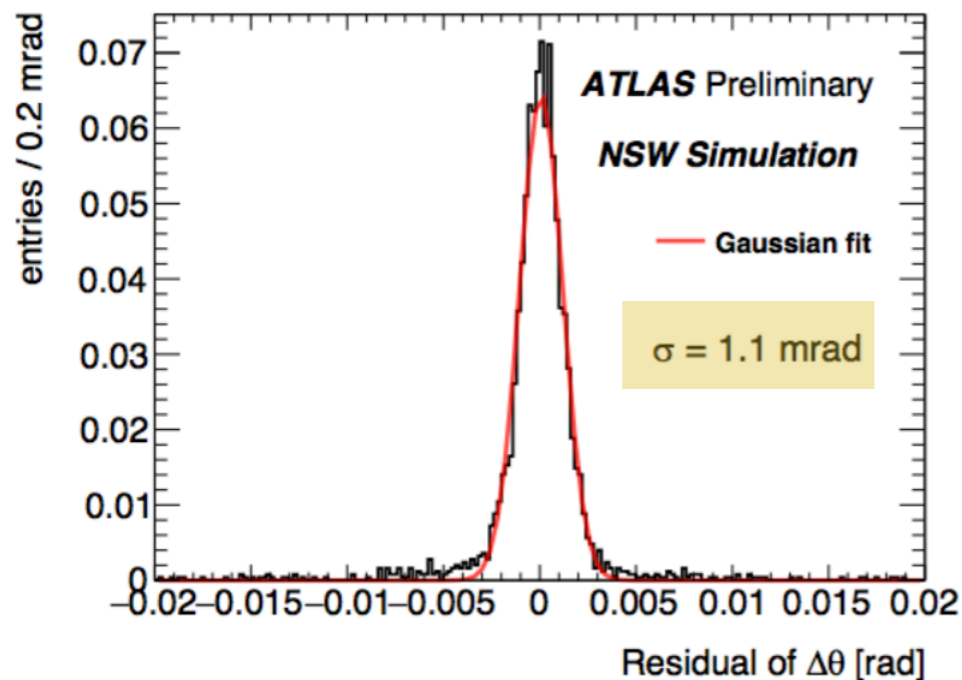
◆ Cut at $\Delta\theta > 15$ mrad to eliminate non-IP pointing background.

□ η : derived from θ_x^{global}

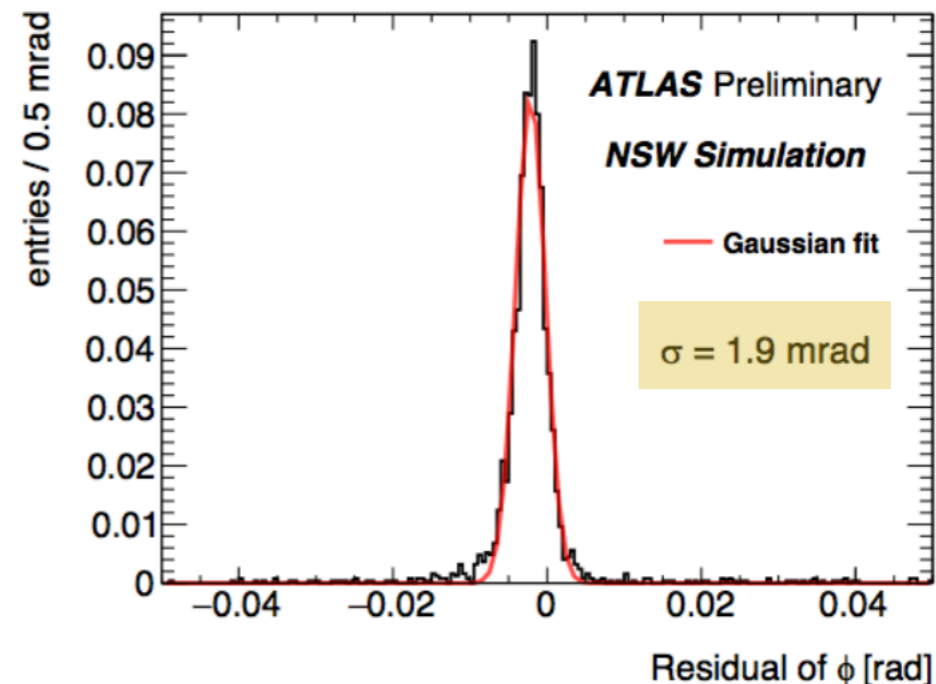
□ φ : derived from stereo slopes using a look-up table.



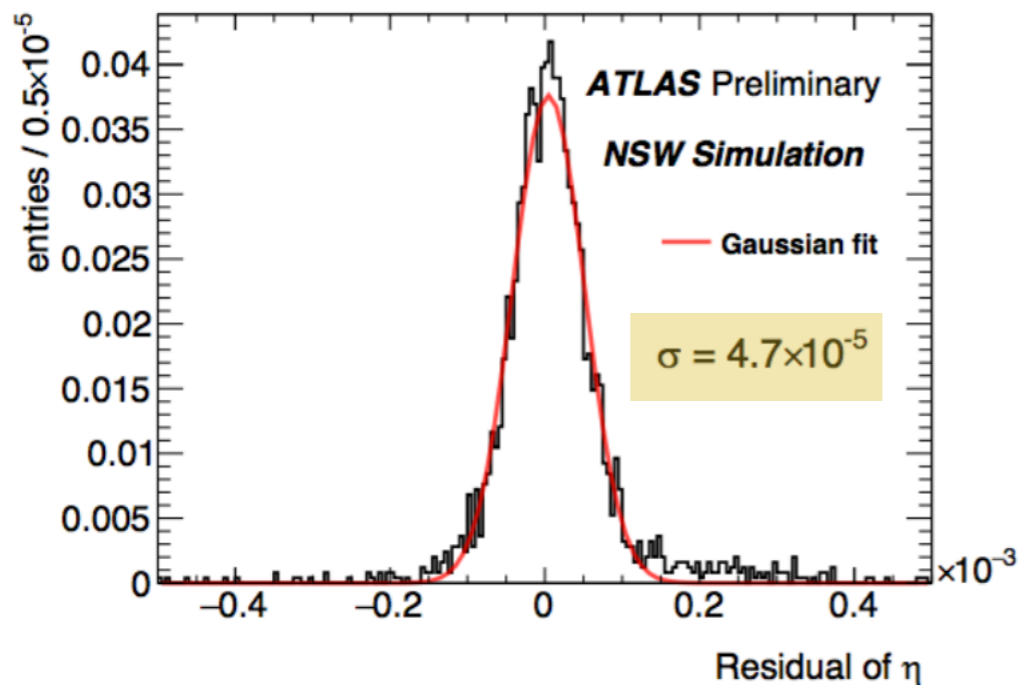
MM Angular Resolution Performance



$\Delta\theta$ requirement: 1 mrad



ϕ requirement: 20 mrad



η requirement: 5×10^{-3}

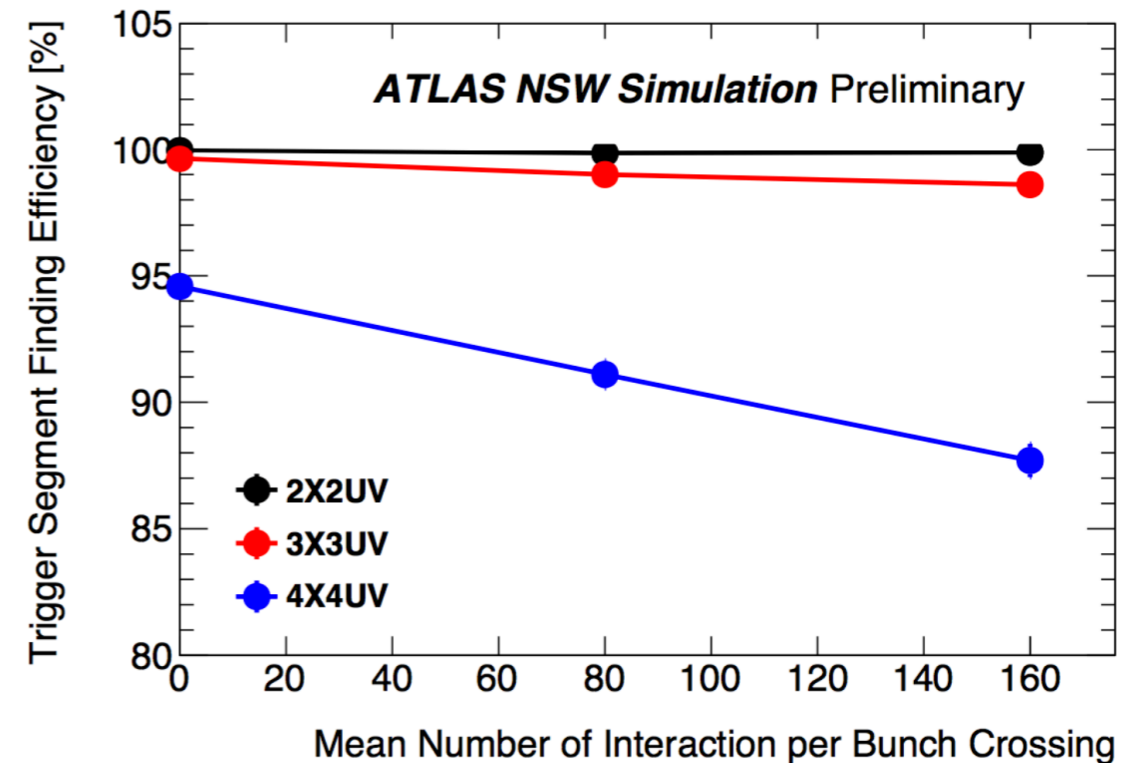
- Residual = |truth - reconstructed|
- Consider hit coincidence threshold of **3X3UV**, 160 events per bunch crossing.
- Gaussian fit on the residual distributions.
- Good performance compared to the requirement.



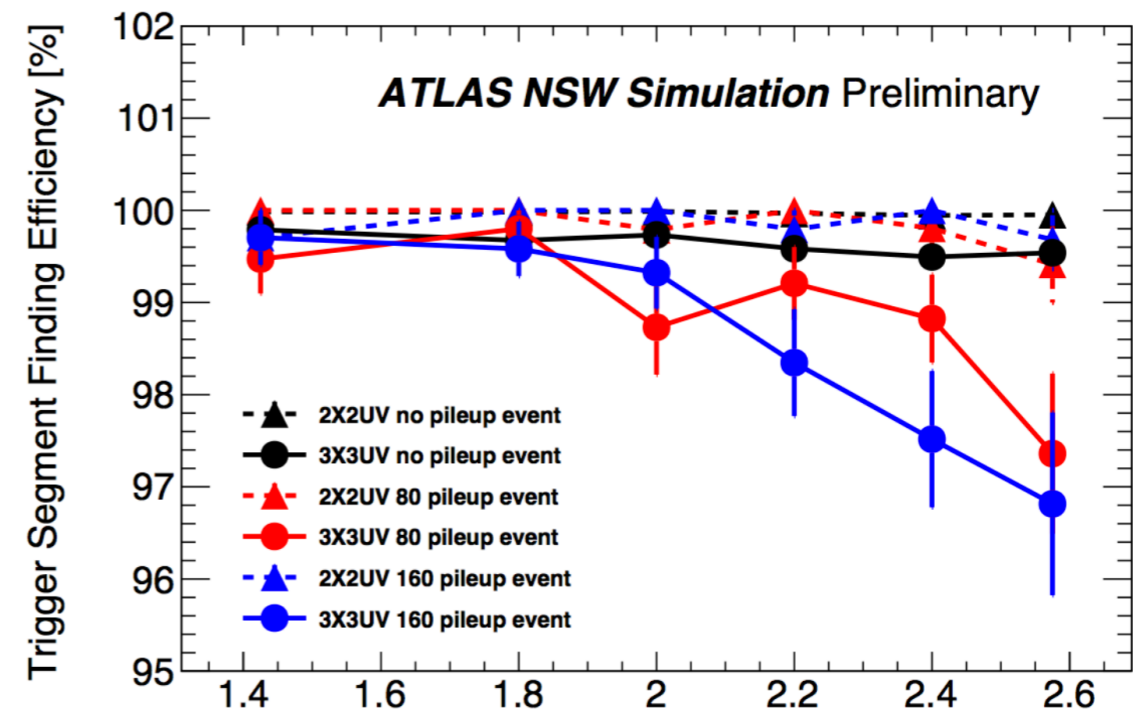
MM Trigger Simulation Performance



- Track segment finding efficiency as a function of μ .
 - Considering 3 different LHC scenarios.
 - Compare the efficiency requiring different hit coincidences.
 - ▶ 4X4UV: lowest efficiency as expected.
 - ▶ 3X3UV & 2X2UV: get 99% efficiency.

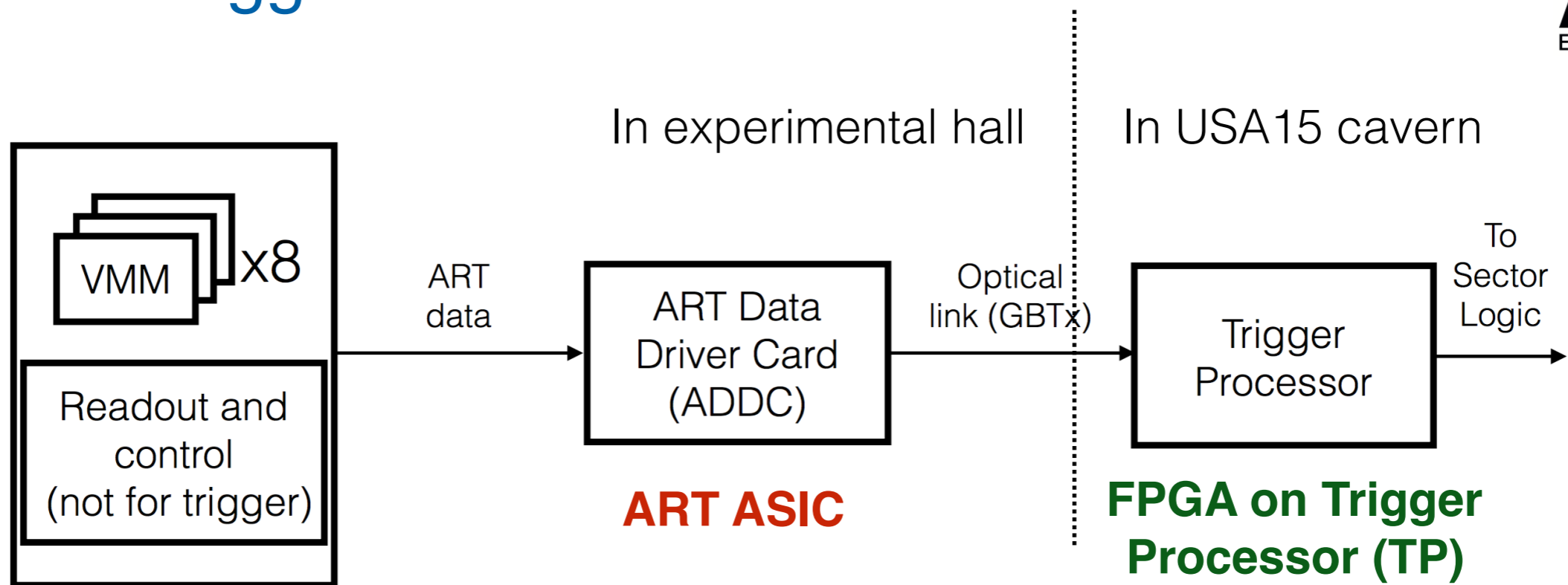


- Track segment finding efficiency as a function of η
 - 3 different LHC scenarios and **2 different hit coincidence thresholds** (2X2UV and 3X3UV) are considered.
 - Combining all cases, the efficiency is about 99%.





MM Trigger Electronics Path



- ▶ 64 channels / VMM
- ▶ Select 1 out of 64 channels, output strip address only.

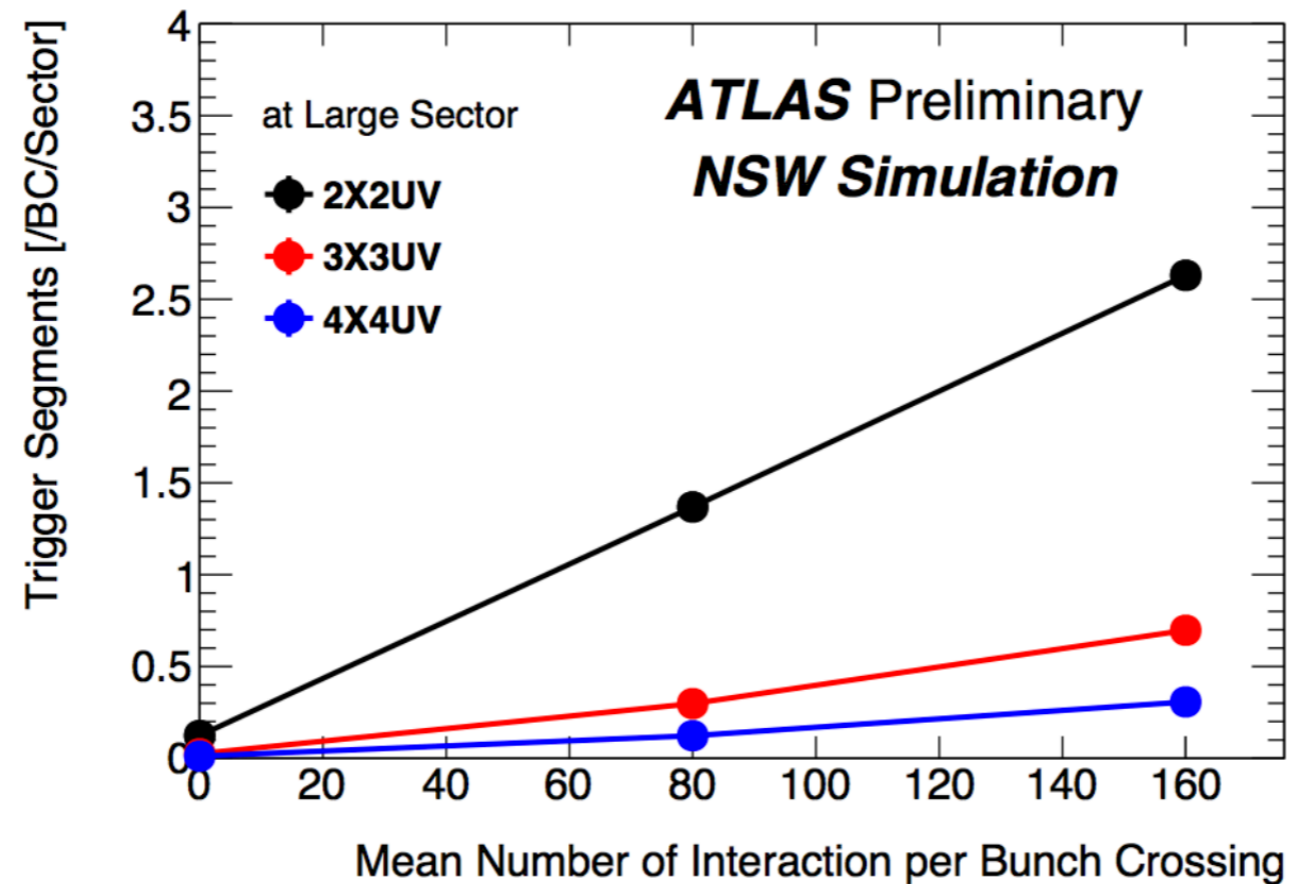
- ▶ Aggregate addresses from 32 VMMs and choose 8.

- ▶ 8 layer hit coincidence. (Look for hits every 50 ns.)
- ▶ Reconstruct track segment and angle.

▶ Maximum output 8 track segments per sector every 25 ns.



Average rate of track segments



○ Average rate of track segments in one sector

□ 3 different LHC scenarios and **3 different hit coincidence thresholds** are considered.

□ The occupancy is small enough the bandwidth limitation, which is at most 8 track segments per bunch crossing.



Summary & Future Look



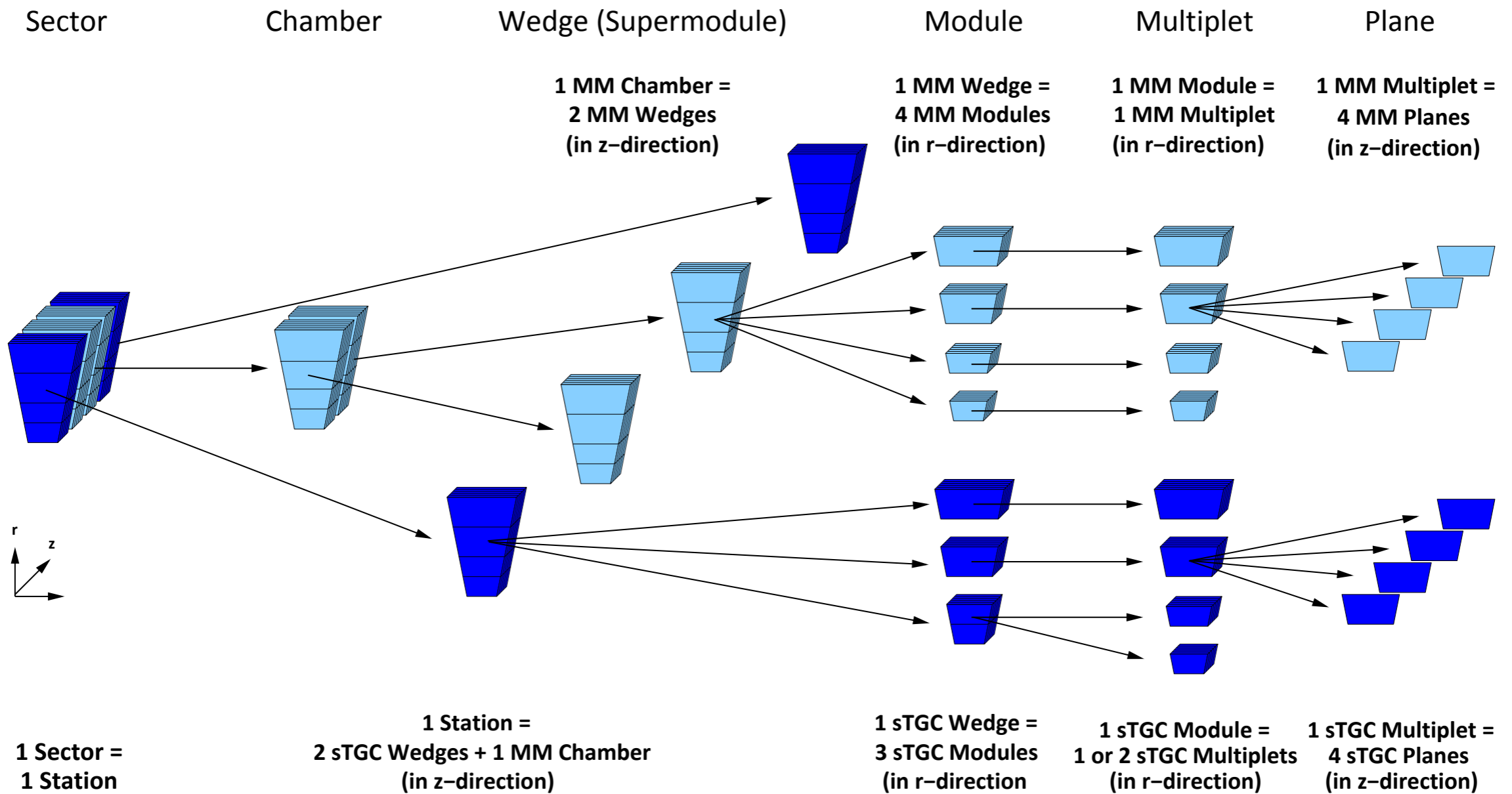
- The ATLAS New Small Wheel is motivated to improve the tracking efficiency and reduce the fake trigger rate in future LHC runs.
- The design of the electronics for both sTGC and MM has been almost completed.
- The trigger algorithms have been developed and currently being commissioned in hardware.
- The simulations show the good performance at efficiency and resolutions.
 - Different numbers of interactions per bunch crossing has been considered.
 - Need to implement the cavern background of neutral particles.
- The simulation is for ideal case, now taking data to get a more realistic approach.
- We are looking forward the installation of the NSW in 2019!



Backups



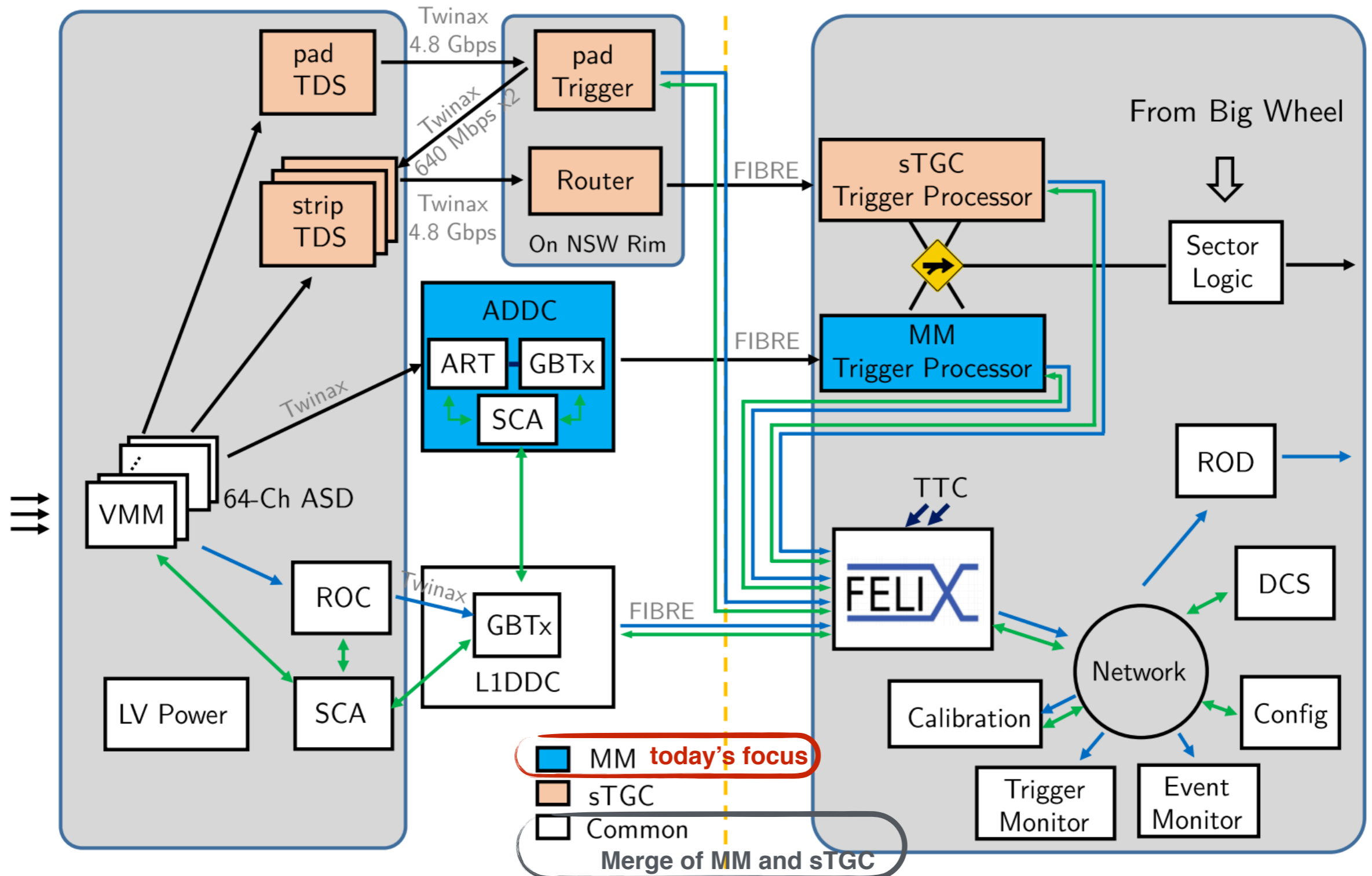
NSW Terminologies





NSW Trigger Electronics Path

VMM ASIC operates for both sTGC and MM





MM ADDC Output Data Format



0b1010	BCID (12)	ERR_FLAGS (8)	HIT_LIST (32)	ARTDATA_ PARITY(8)	ART (6)	ART (6)	ART (6)	ART (6)	ART (6)	ART (6)	ART (6)	ART (6)
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NSW Trigger Output Data Format



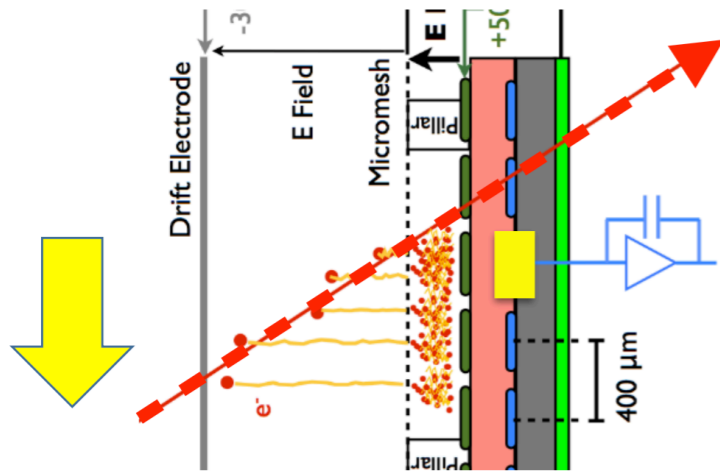
Field:	sTGC type	MM type	$\Delta\theta$ (mrad)	ϕ index	R index	spare
Num of bits:	2	2	5	6	8	1

Table 5: Data format of the output of the trigger processor sent to the Sector Logic. Format of a track vector candidate from the NSW (24-bits/track vector). The sTGC and MM type information can encode the quality of the candidate.

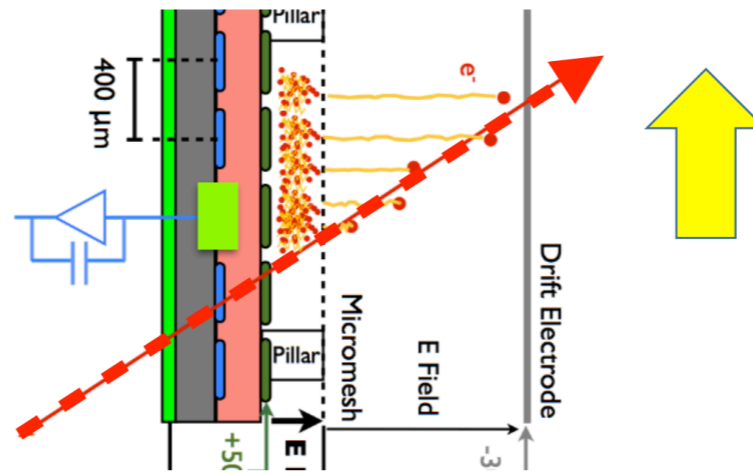


Phi Bias Explain

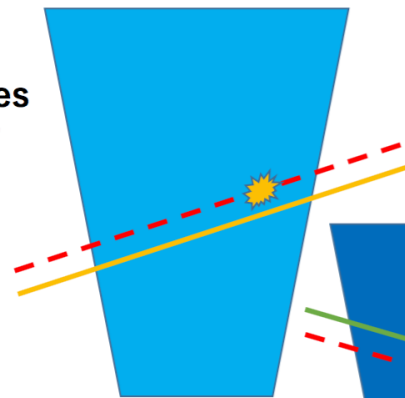
Face up



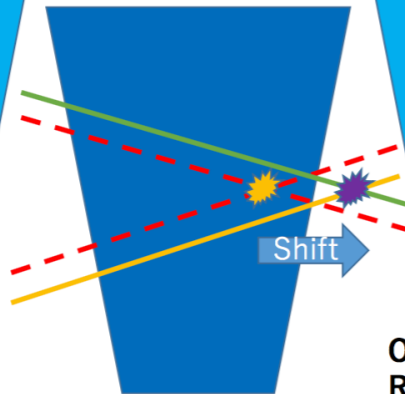
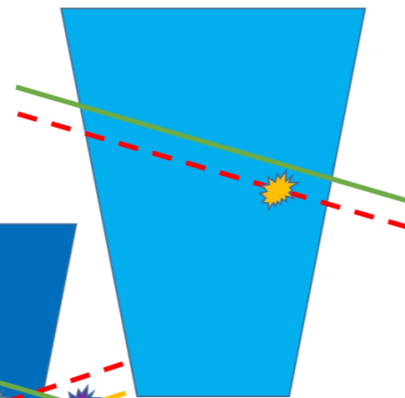
Face down



Face up
Signal comes from Lower



Face down
Signal comes from Upper



Overlap these two layers,
Reconstructed phi shifts.

