5th International Conference on
Micro-Pattern Gas Detectors (MPGD2017)
and RD51 Collaboration Meeting

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A custom readout electronics for the BESIII CGEM detector

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Outline

Giulio Mezzadri' s talk → Introduction

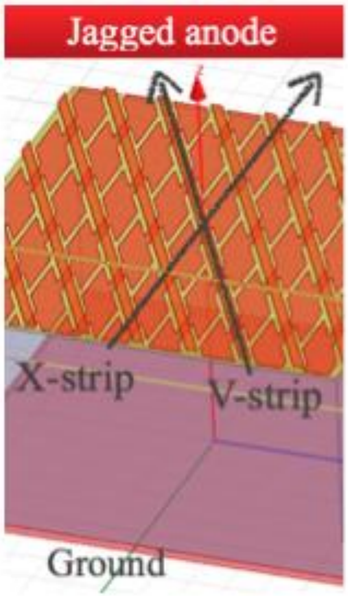
Overview of the readout electronics for the BESIII-CGEM IT

On detector electronics

- Design of a dedicated ASIC for CGEM Readout (TIGER)
- In silicon characterization of TIGER prototype
- First tests on CGEM detector

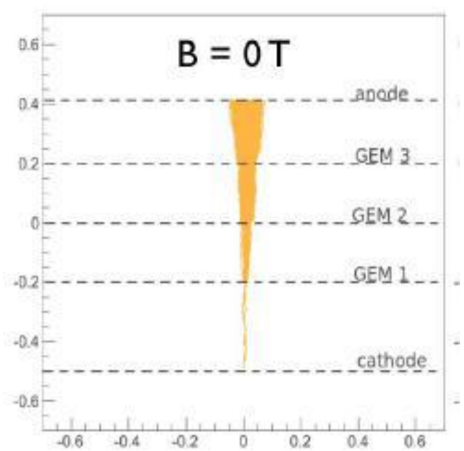
Outlook

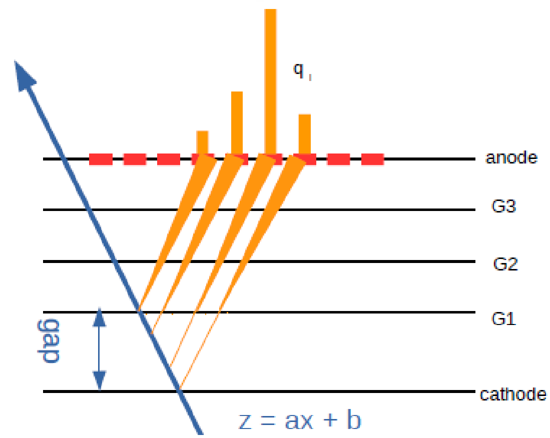
CGEM Inner Tracker readout



- ❑ **Charge centroid method**
  - ▶ Digital Readout
  - ▶ **Analog Readout**
    Loosening pitch (650 μm) & less channels (about 10 thousand)

- ❑ **μTPC (Time Projection Chamber)**
  time resolution 5 ns

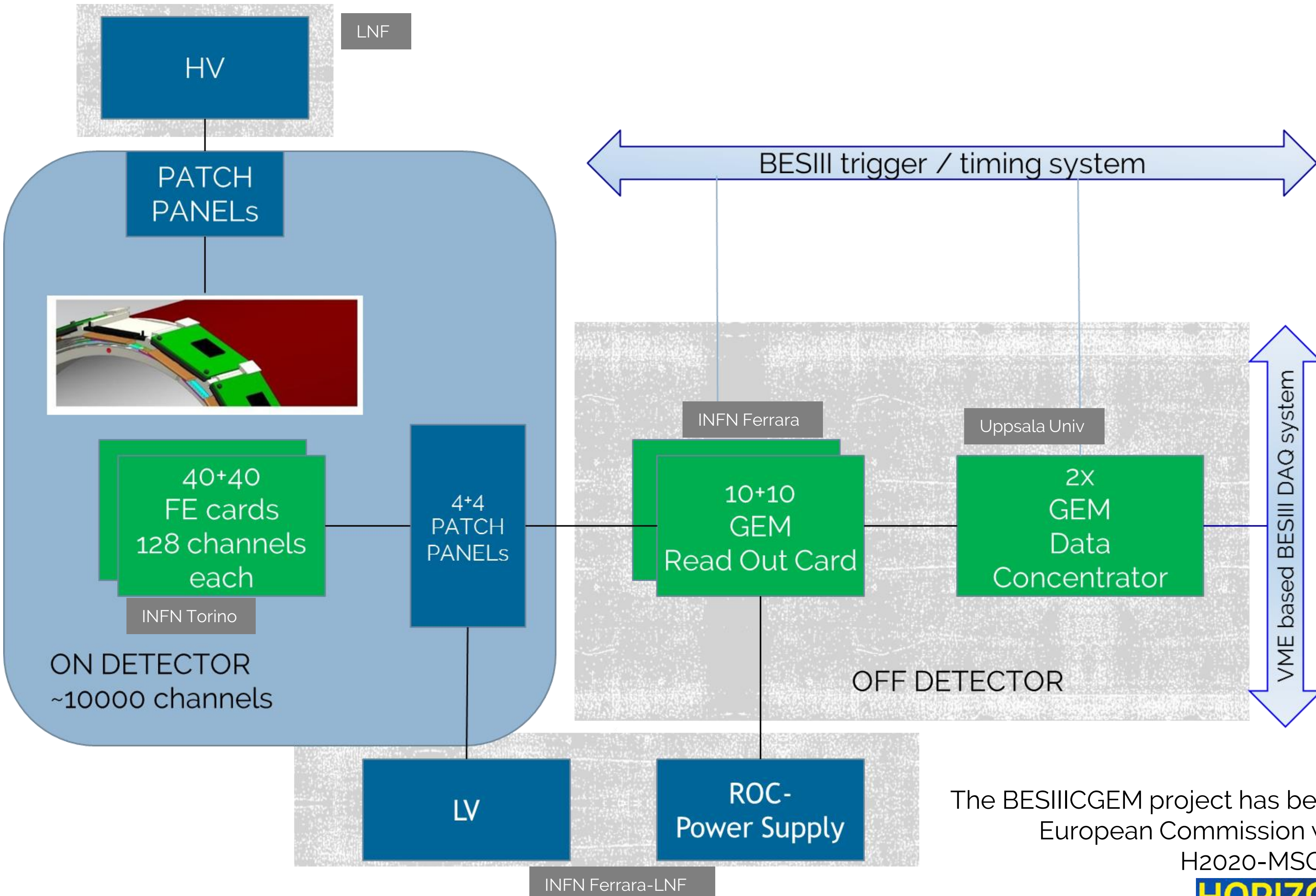




readout with 160 dedicated, integrated 64-channel ASICs

Introduction
Readout electronics
TIGER
In silicon
on detector
Outlook

Overview of CGEM-IT readout electronics



Introduction
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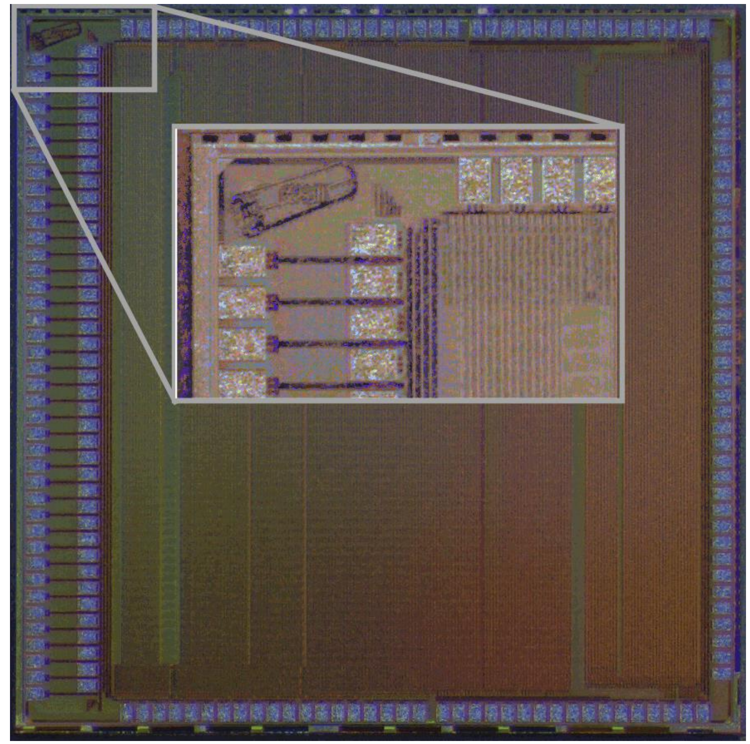
The BESIIICGEM project has been funded by European Commission within the call H2020-MSCA-RISE-2014.
HORIZON 2020

TIGER: Torino Integrated Gem Electronics for Readout

Expected signal from CGEM-IT:
30-50 ns duration,
30-40 ns rising time, 10 ns falling time
depends on gas mixture, gain and electric field

- input charge: 1 - 50 fC
- up to 100 pF sensor capacitance
- 4-5 ns time resolution
- 60 kHz rate per channel
(safety factor of 4 included)
- power ~10 mW/channel

25 mm² UMC110 CMOS



provide time and charge measurement,

feature a fully-digital output

be SEU-tolerant

Chip architecture

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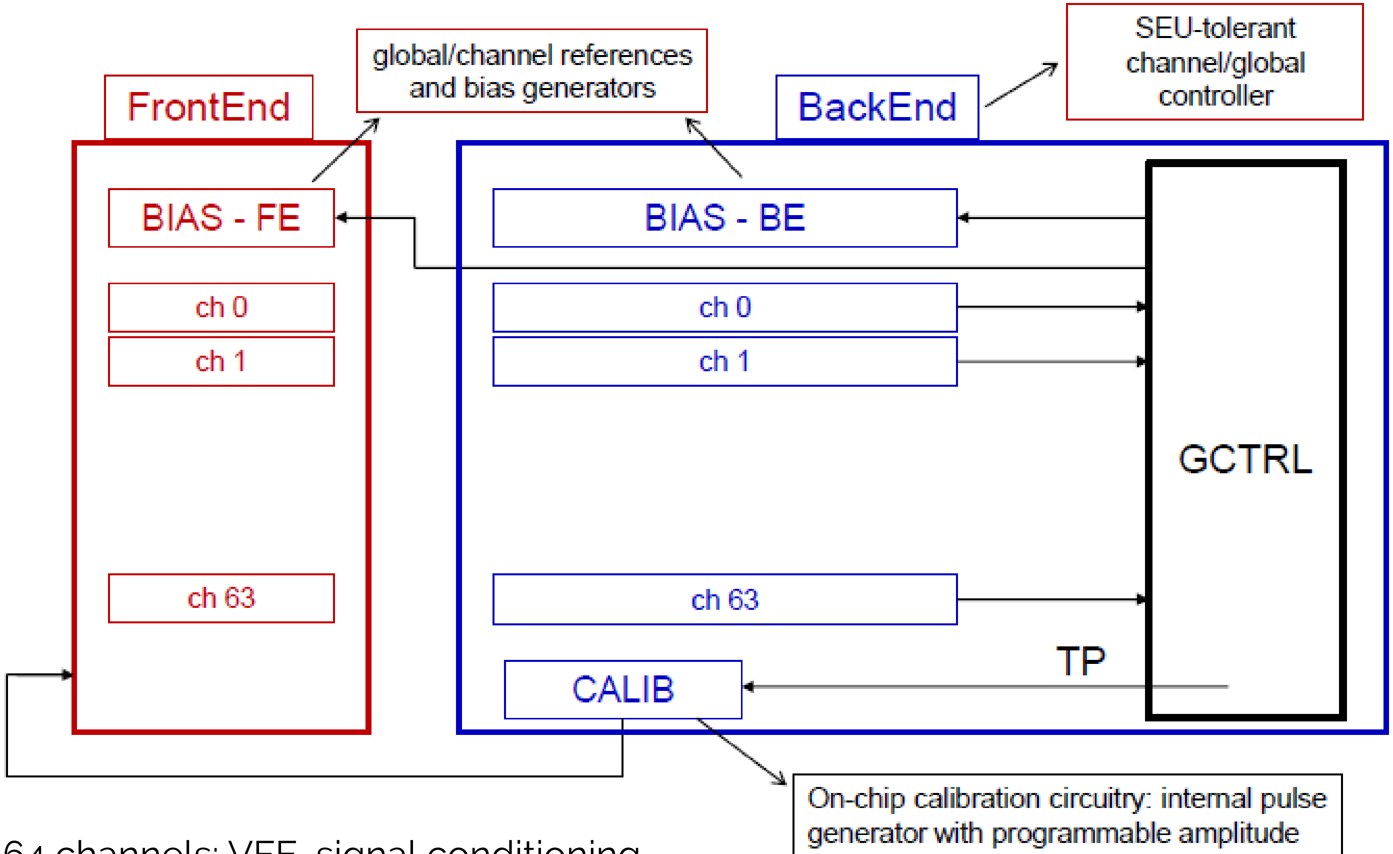
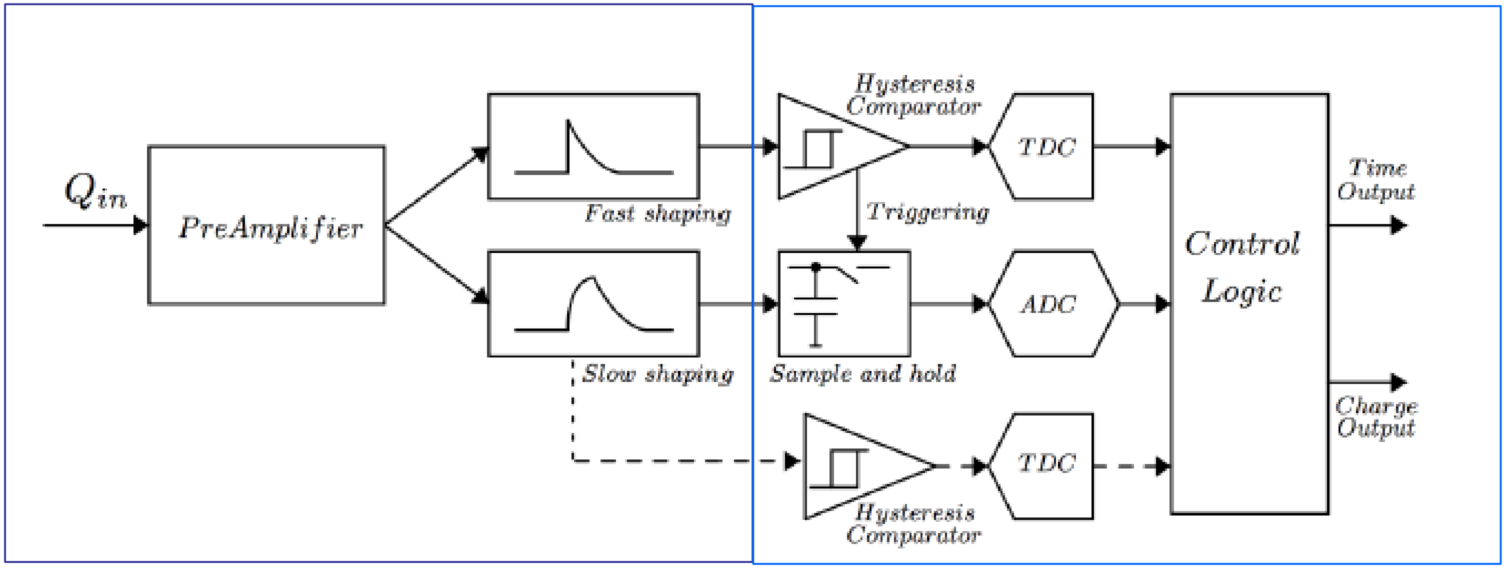


64 channels: VFE, signal conditioning, TDC/ADC, local controller
on-chip bias and power management
on-chip calibration circuitry
fully digital output, LVDS IO
4 TX SDR/DDR links, 8B/10B encoding, 200 MHz
SPI configuration link

Each channel



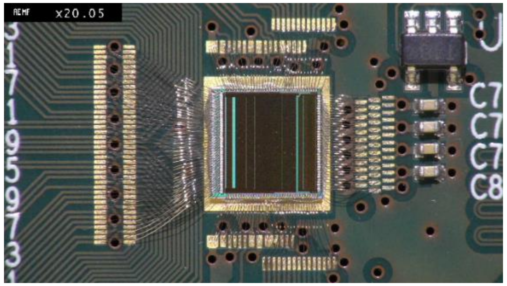
front-end

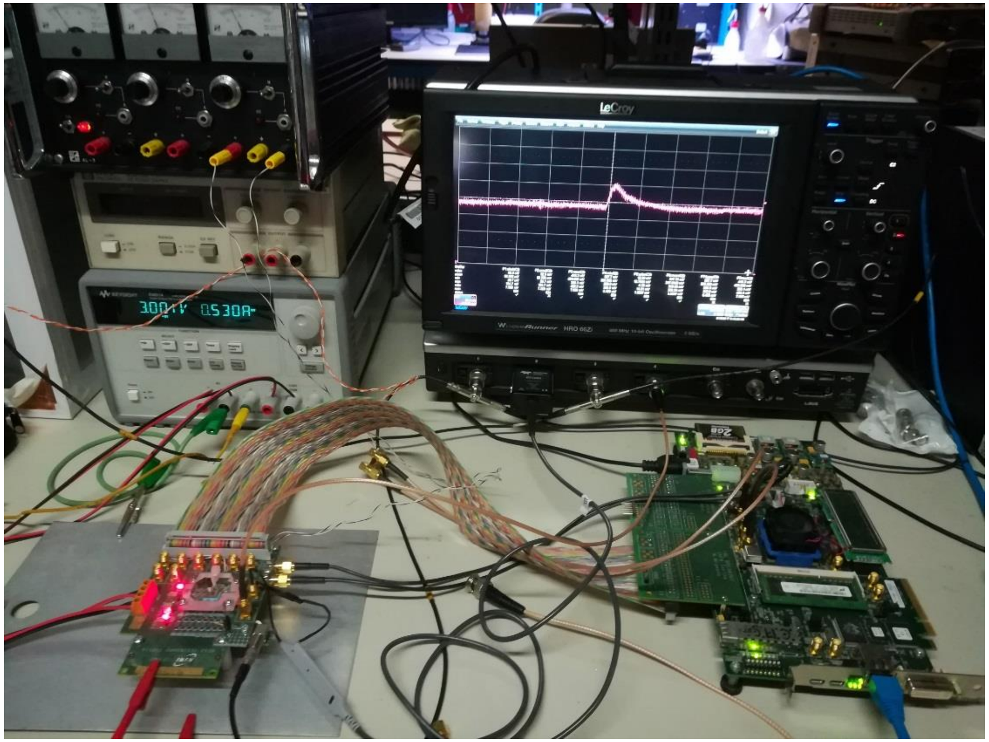
back-end
+SEU protection

T-BRANCH
timestamp on rising/falling edge (sub-50 ps binning quad-buffered TDC)
charge measurement with Time-over-Threshold

E-BRANCH
timestamp on rising edge (sub-50 ps binning quad-buffered TDC)
Sample-and-Hold circuit for peak amplitude sampling
slow shaper output voltage is sampled and digitised with a 10-bit Wilkinson ADC

Test setup





- Project: Tiger.lvproj
  - My Computer
    - Tiger acq analysis
    - Tiger acquisition
      - _subVIs
      - Tiger_Acq_ChannelScan.vi
      - Tiger_Acq_DecodeRawData.vi
      - Tiger_Acquisition.vi
    - Tiger control
      - _subVIs
      - Tiger_TestCommands.vi
    - Tiger debug
      - _subVIs
      - Tiger_DecodeChipScopeFile.vi
      - Tiger_TB_DebugGlobalConfig.vi
      - Tiger_TB_DebugTxData.vi
      - Tiger_TB_DecodeTData.vi
      - Tiger_TB_DecodeTxData.vi
      - Tiger_TB_ReadChannelConfig.vi
      - Tiger_TB_ReadEventsFile.vi
      - Tiger_TB_ReadGlobalConfig.vi
      - Tiger_TB_ReadSPIFile.vi
      - Tiger_TB_WriteChannelConfig.vi
      - Tiger_TB_WriteGlobalConfig.vi
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    - Tiger measurement
      - _subVIs
      - Tiger_ChannelScan.vi
    - Tiger measurement analysis
      - _subVIs
      - Tiger_TDC_Calibration.vi
      - Tiger_VThr_Calibration.vi
    - Tiger Tsensor

Characterization runs in summary

- ✓ R/W Channel/Global configuration registers
- ✓ Data TX and decoding
- ✓ Baseline and threshold equalisation

(dual-) TDC operation

Front-end performance
internal calibration circuitry
external charge injection (channel 63)

unexpected amplifier baseline shift,
may limit linearity of Sample and Hold

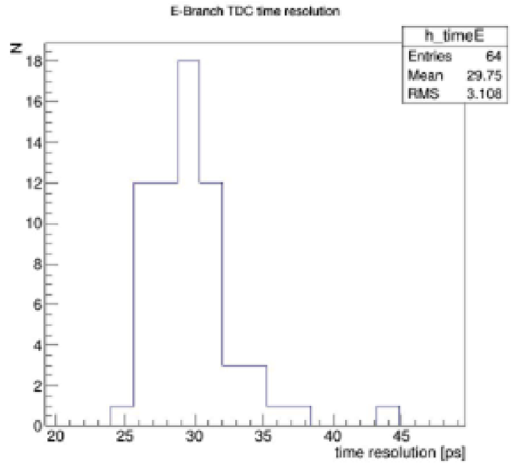
→*operation at higher temperature to recover BL shift*

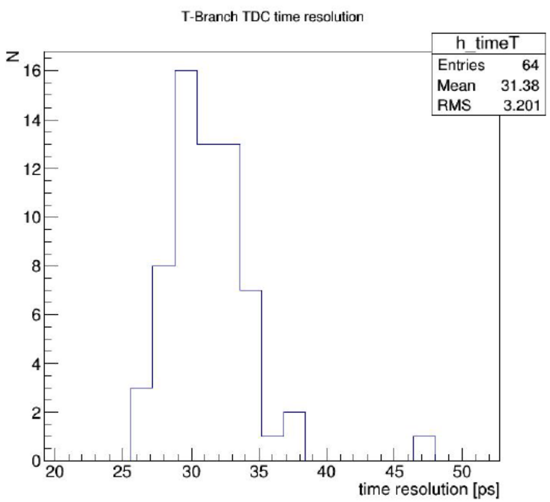
TDC operation: quantization error

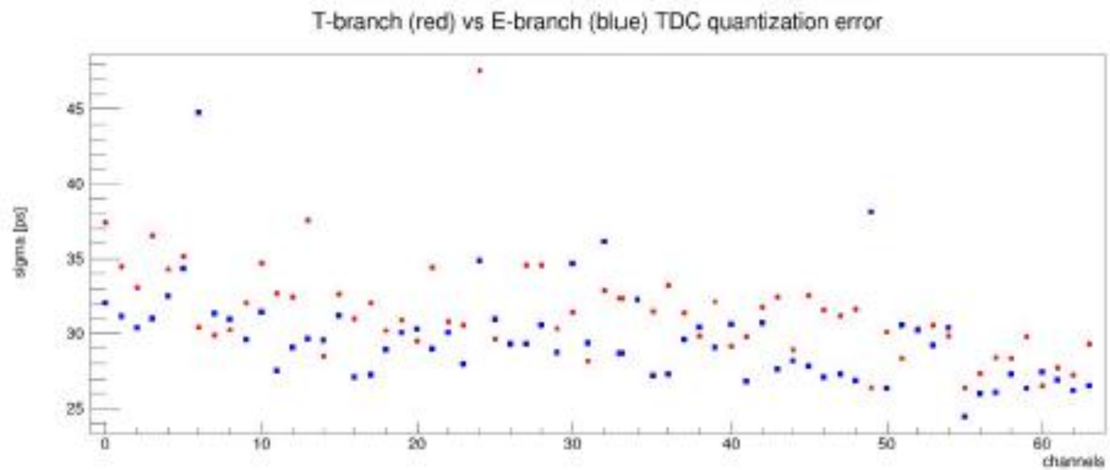
Scan over dynamic range sweeping internal test-pulse phase

Create LUT with gain and offset correction

⇒ Average TDC quantization error after calibration: 30-35 ps r.m.s.

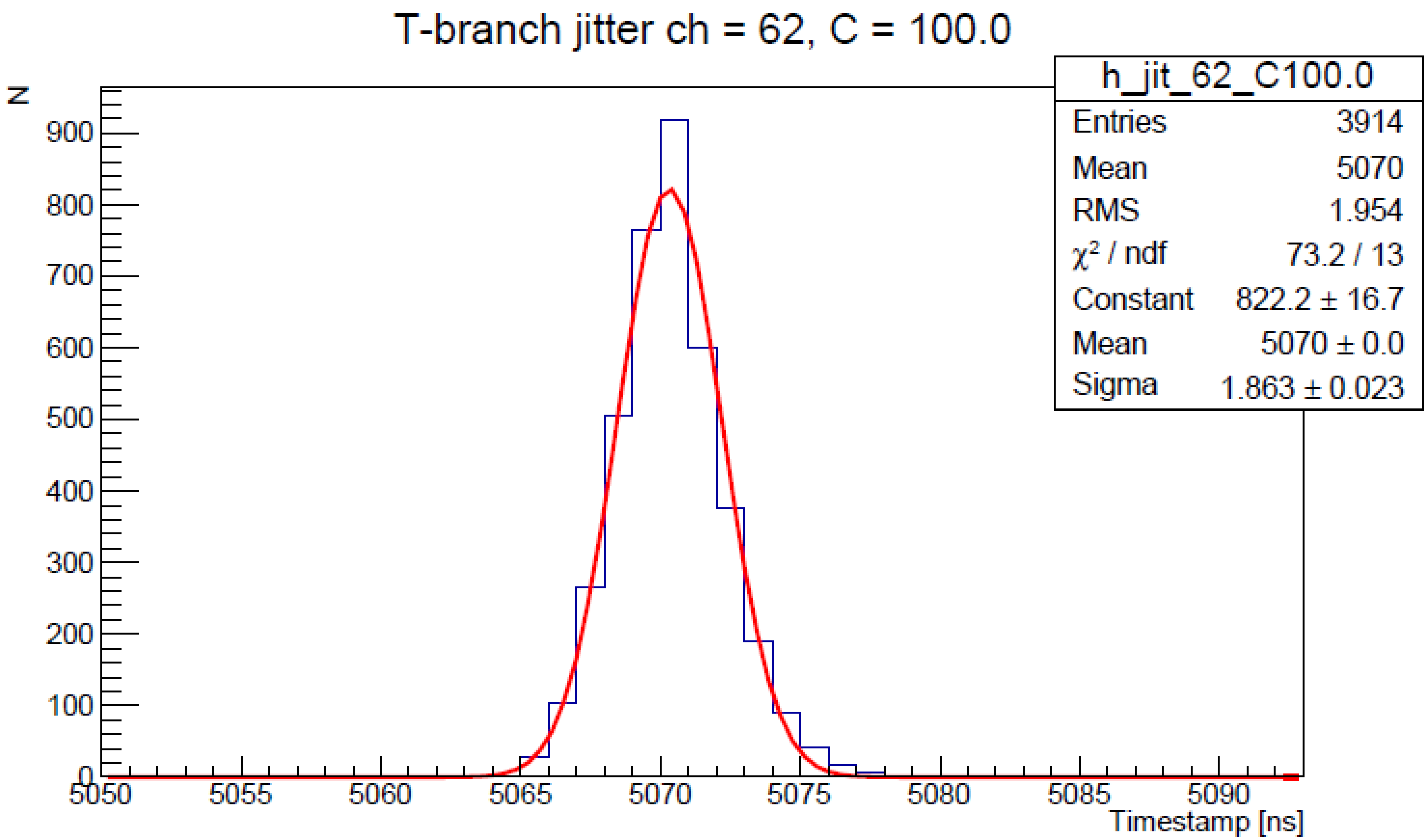






Timing performance: jitter

Jitter measurements using internal calibration circuit test-pulse (e.g. 10 fC) sweeping input capacitance on channel 62



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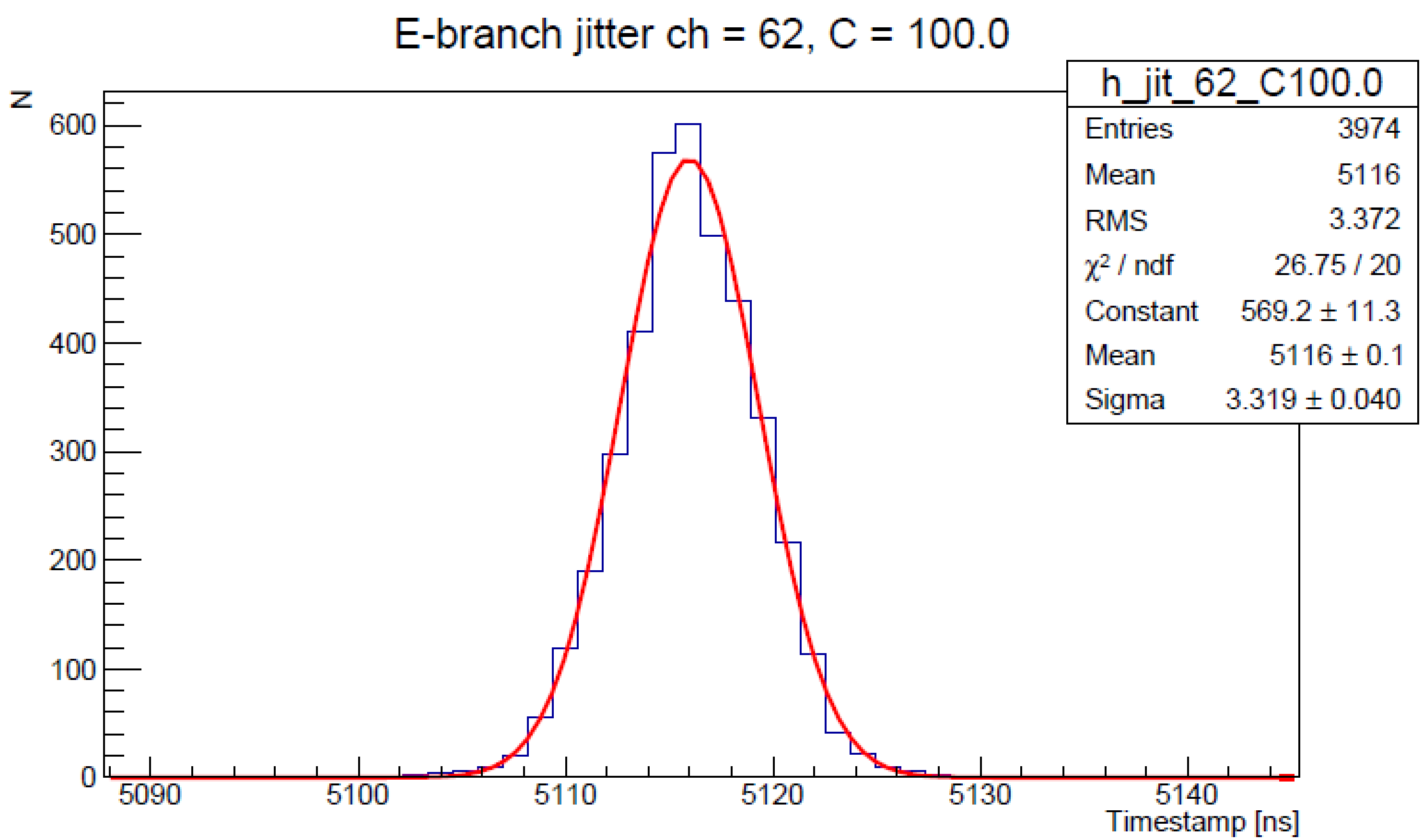
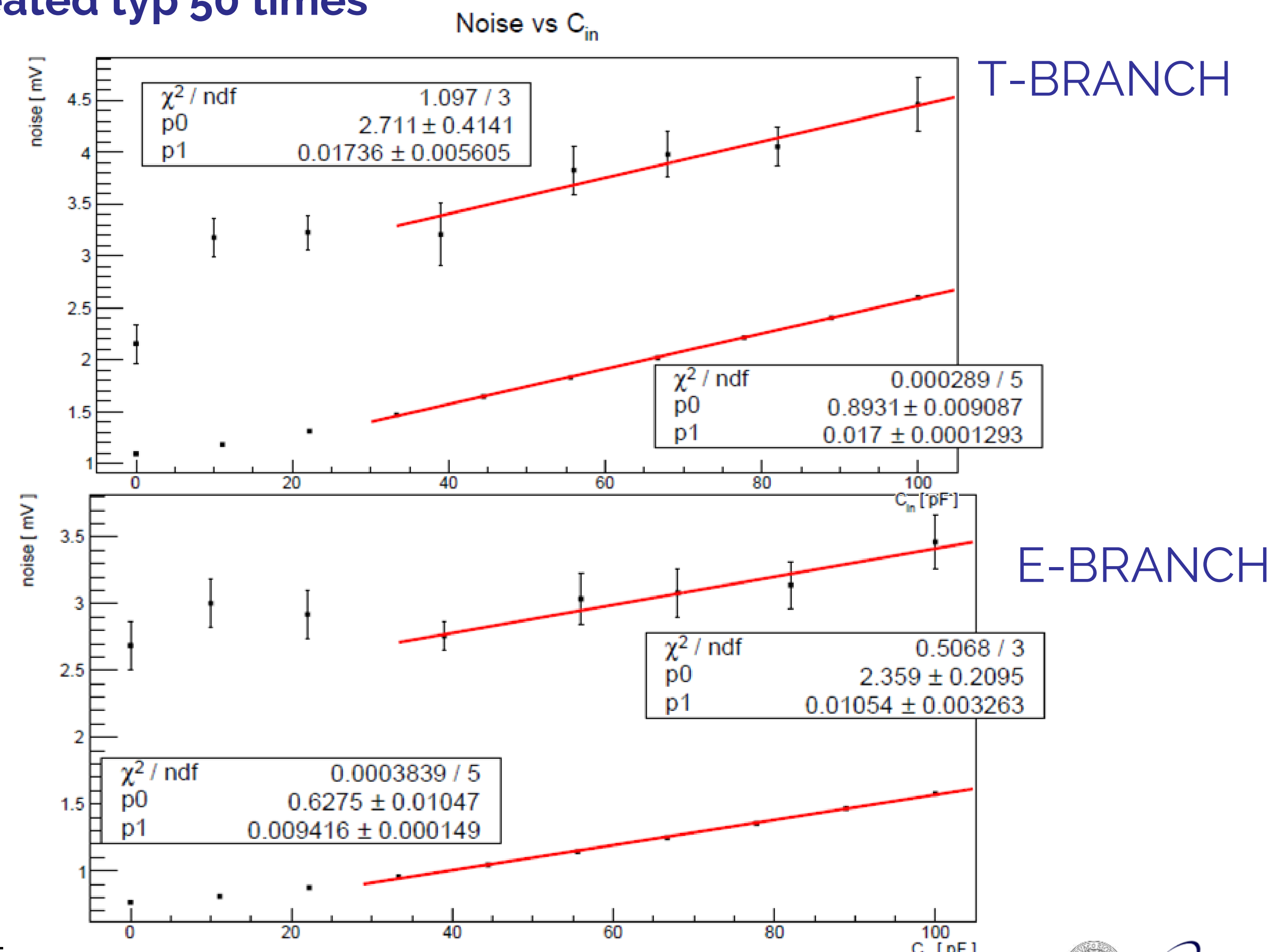


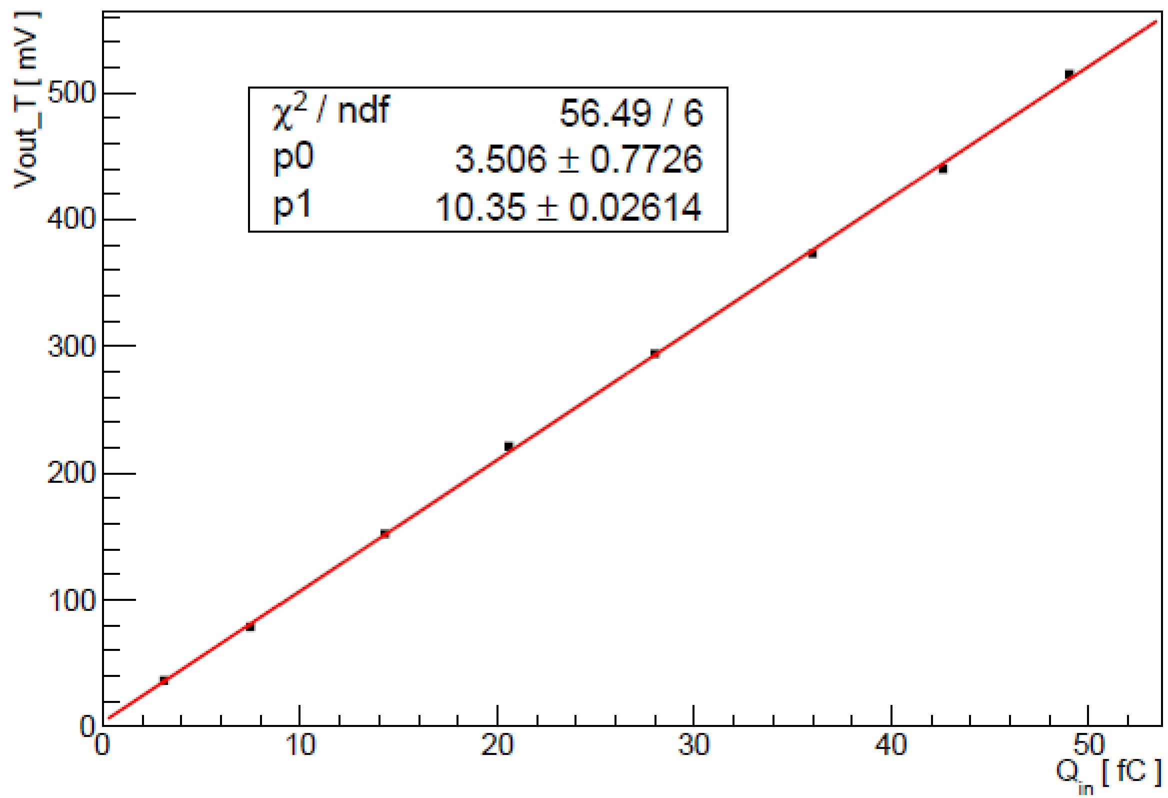
Noise measurements

Noise evaluated for each input capacitance through a sigmoid fit from a typ 500 points threshold-scan with fixed test-pulse (10 fC)
Measure repeated typ 50 times



Gain

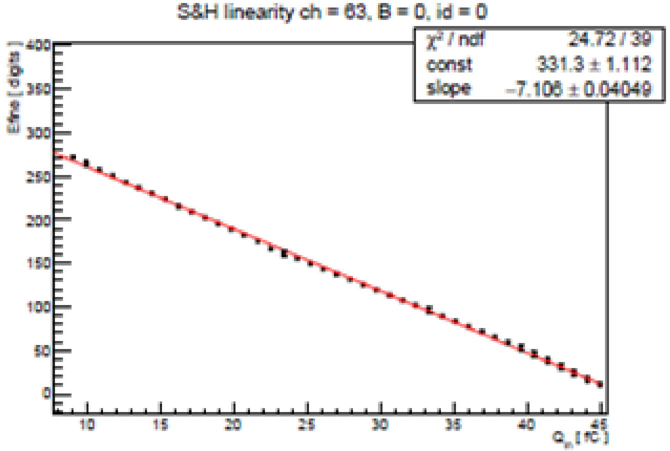
Evaluated on channel 63 using an external pulse generator
Gain: 10.4 mV/fC in agreement with simulations (expected ~11 mV/fC)



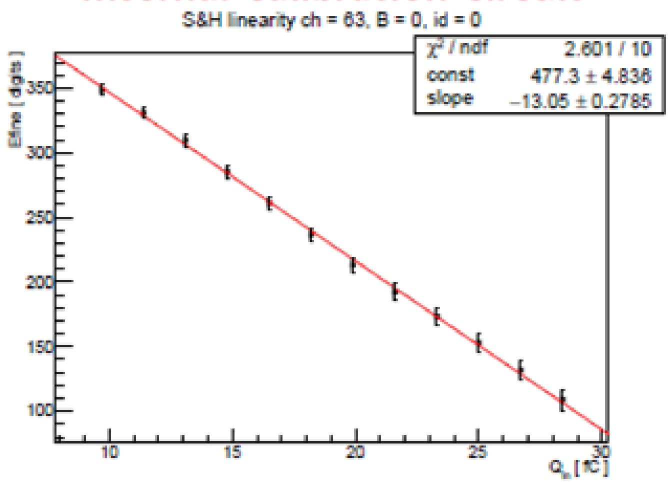
Charge measurements: Sample and Hold

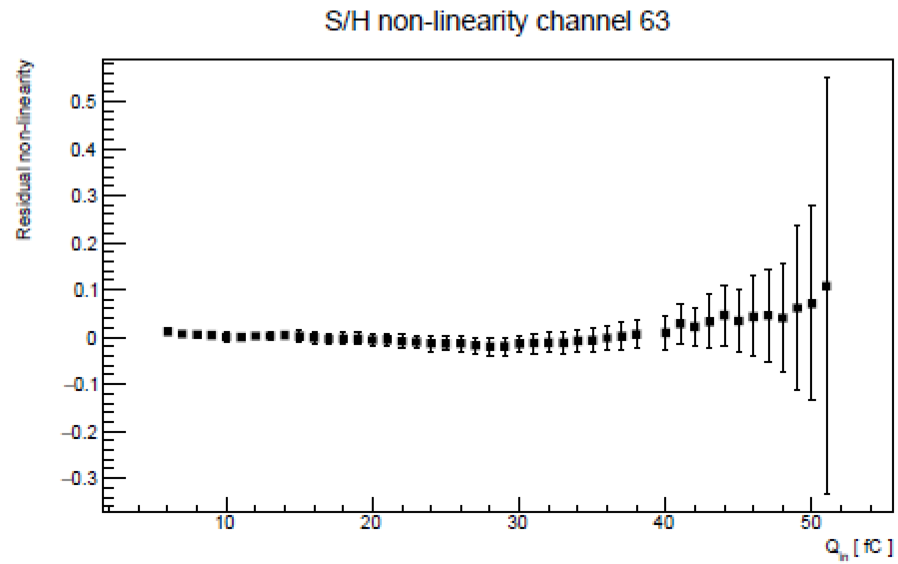
Calibration of dynamic range with external test-pulse generator
Back-annotation to generate a parameter space for the internal calibration circuit

External TP generator



Internal calibration circuit





→Linearity checked
→Dynamic range: 510-520 mV

Charge measurement below 5 fC measured with double-threshold operation (one-channel only)

Characterization results in summary

Time-based readout working properly

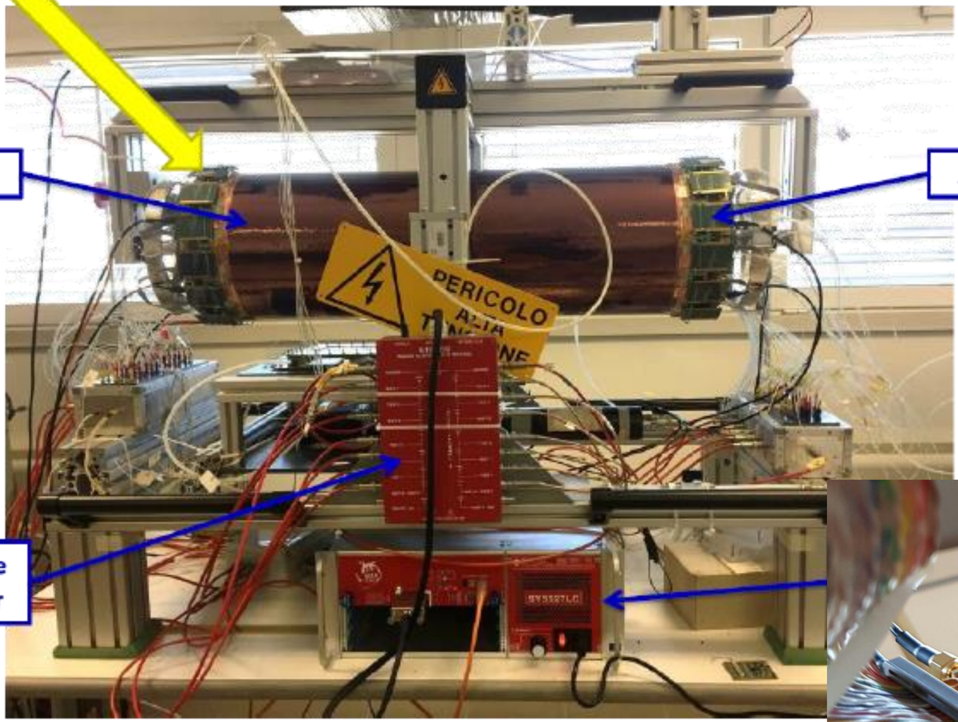
Baseline dependence on temperature
root cause: fragility of bias conditions of baseline holder circuit
reproduced fairly well in simulations
minor revision activities started

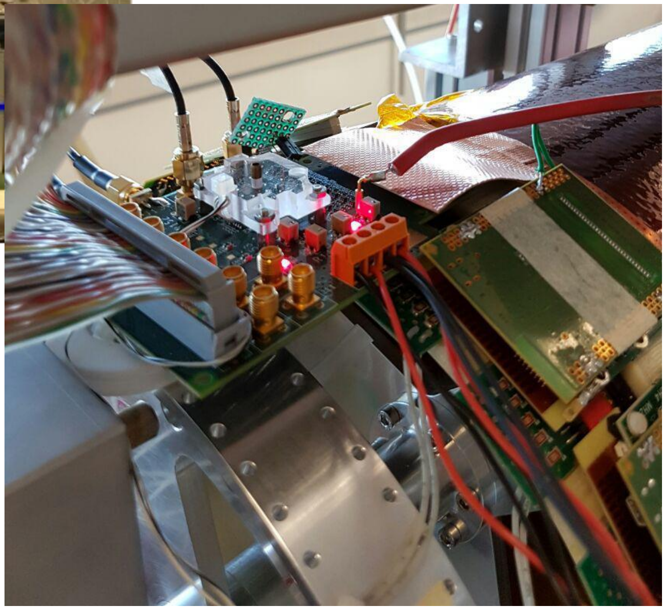
Charge measurement: S/H linearity assessed

Main result: no second prototype needed

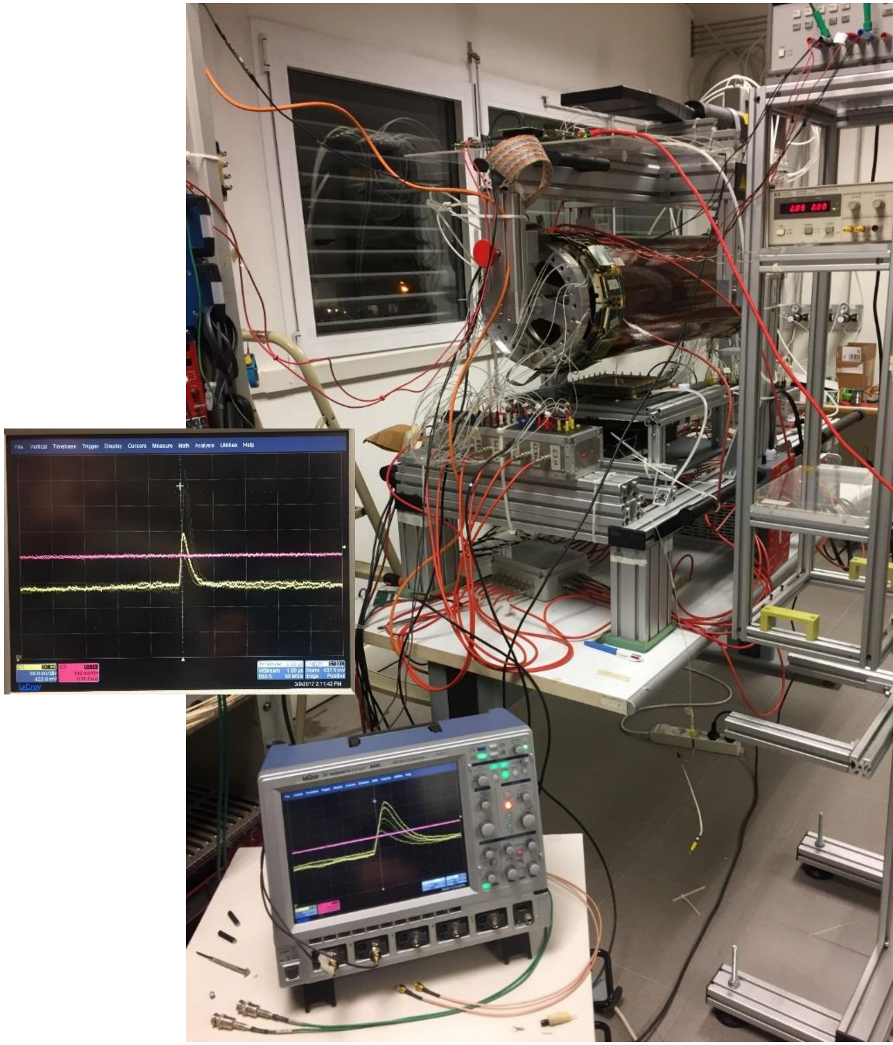
→GEM testing
to assess the performance as it explores a realistic grounding and noise pick-up environment.

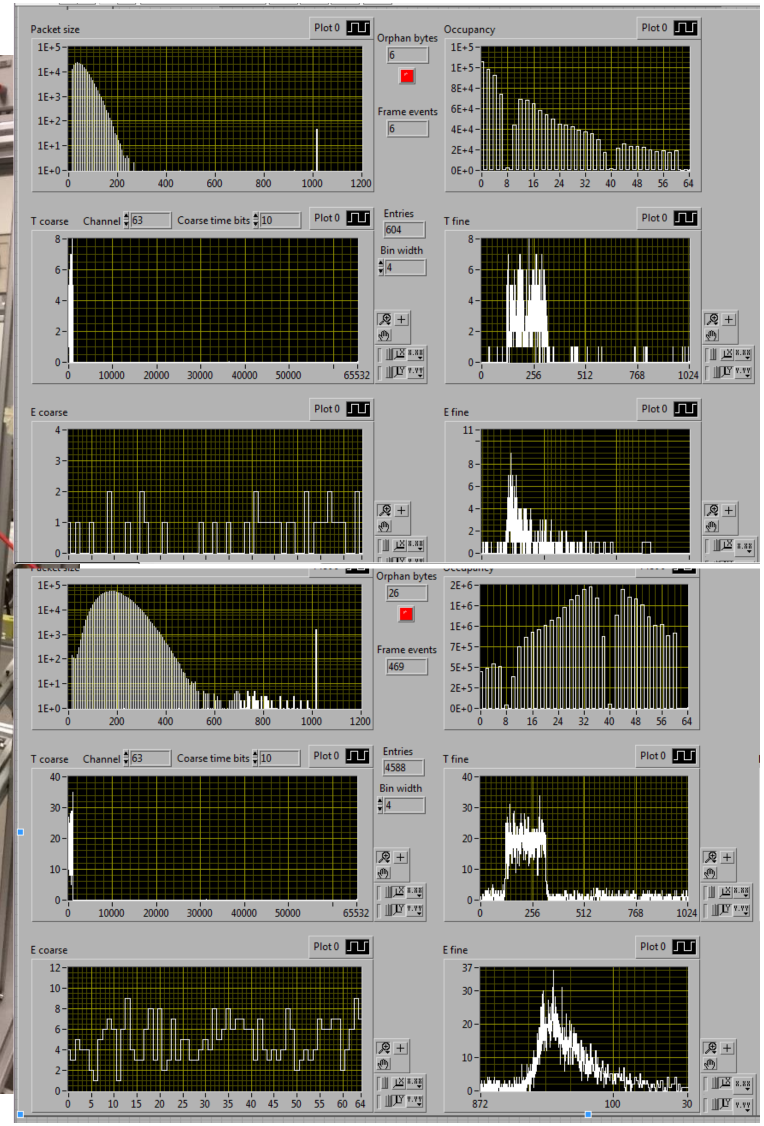
GEM testing





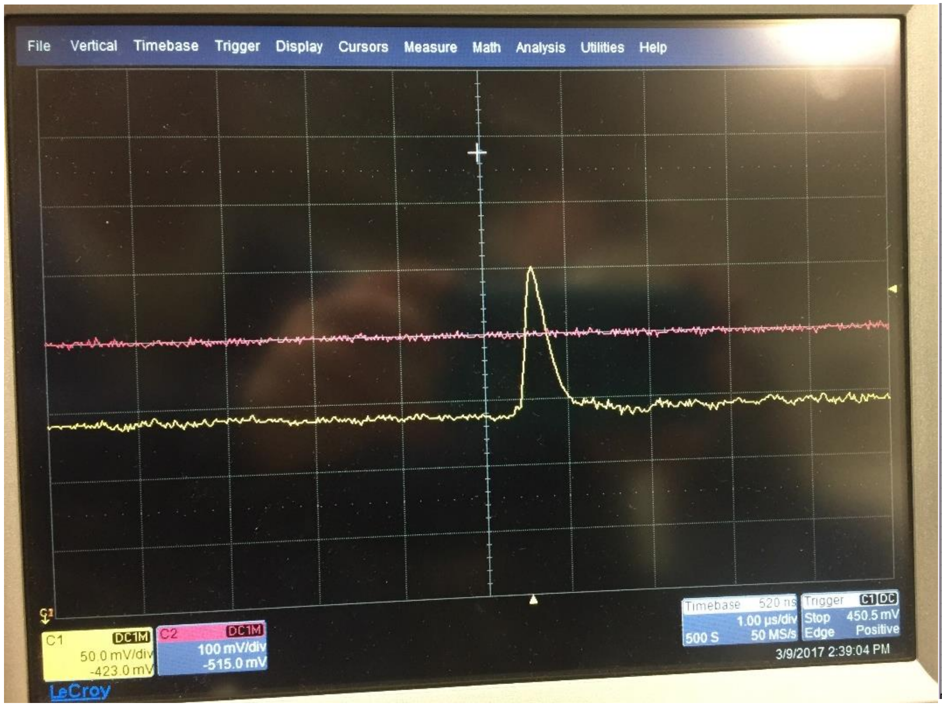
GEM testing

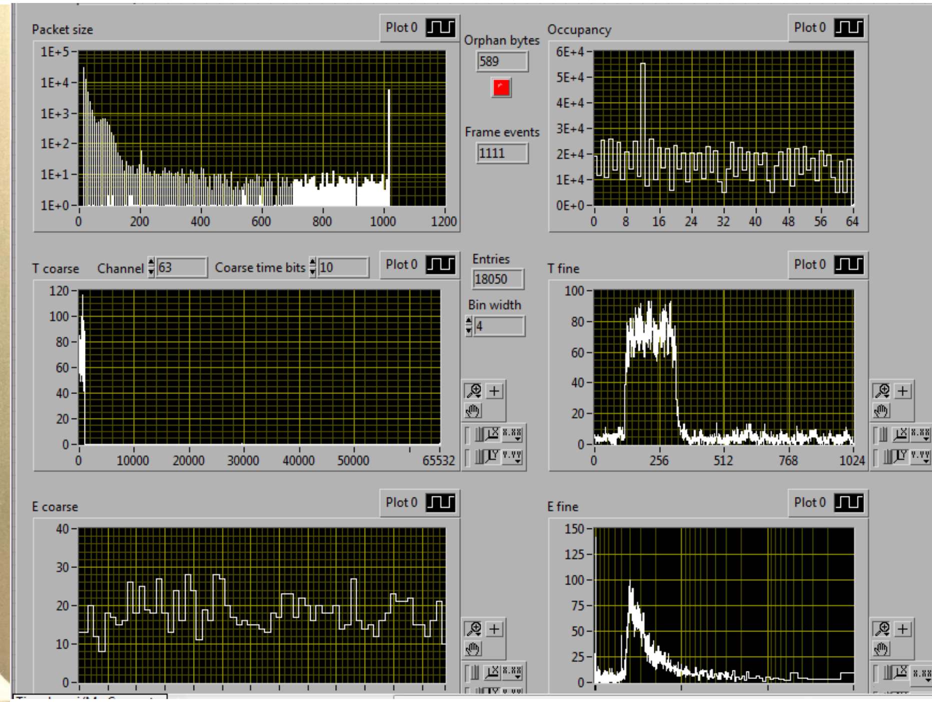




First signals with 90-Sr source

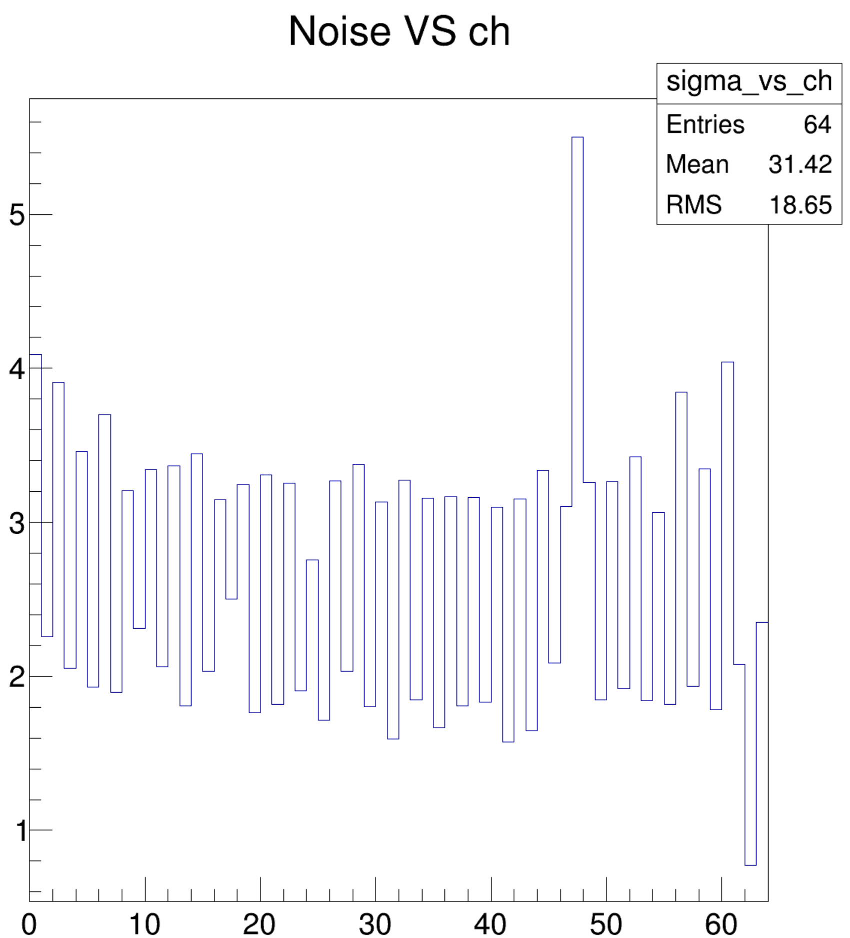
GEM testing

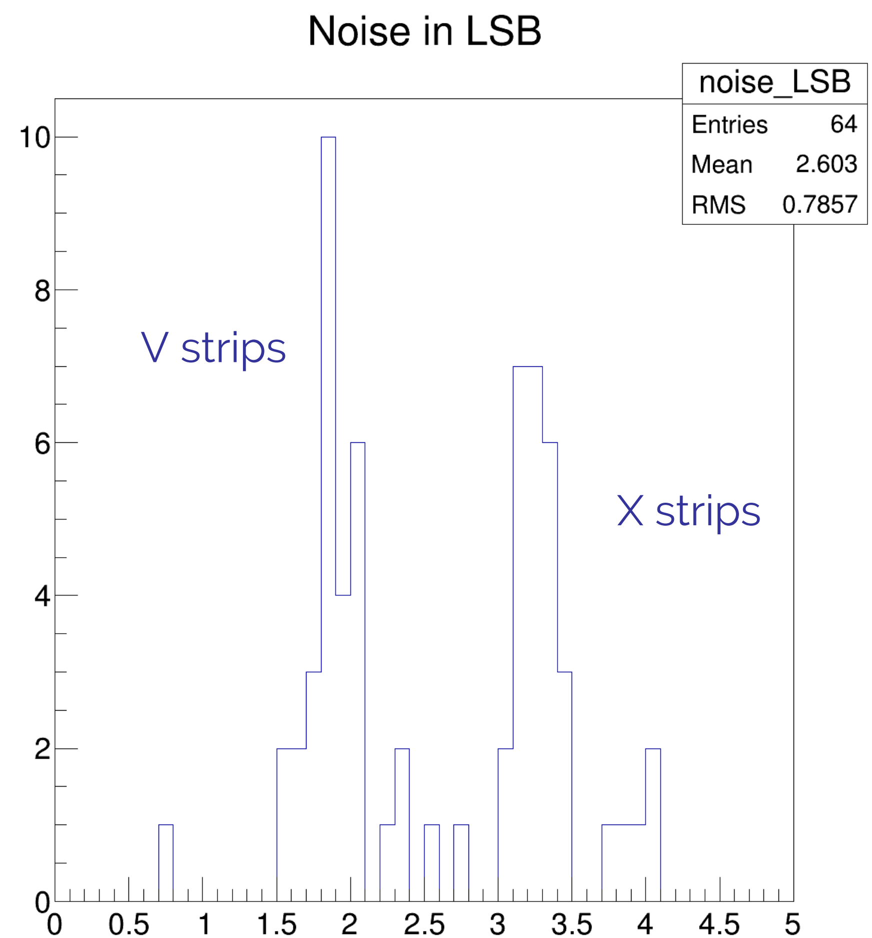




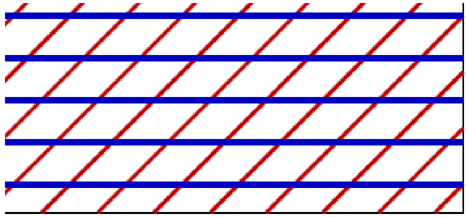
First signals with cosmic rays (night acquisition)

Noise





LSB=3.1 mV

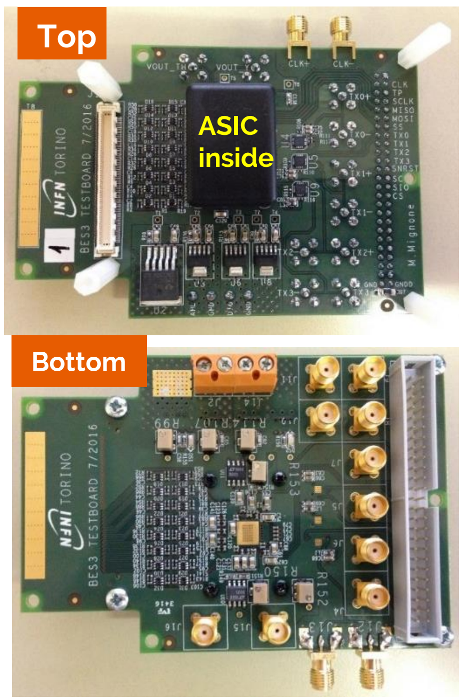


GEM foil

→sensitivity to grounding

Radiation hardness at CERN GIF++ facility

Test board irradiated to about 30 krad to test radiation damage on Voltage Regulators



Analog power: TPS78601KTTT, TPS78601DCQ
Digital power: TPS78601DCQ, TPS78625DCQ

	PRE (V)	POST (V)	%
Analog power			
T1	1,232	1,222	0,992
T2	1,232	1,222	0,992
Digital power			
T3	1,232	1,222	0,992
T4	2,505	2,488	0,993

-0.7/0.8 %
ok!

LT3021
for Voltage reference

	PRE (V)	POST (V)	%
Vref (T5)	0,835	0,867	1,038
Vblh (T7)	0,301	0,327	1,086
Vout_th	0,575	0,452	0,786
Vout_y	0,506	0,5	0,988

we will have
resistor voltage dividers

SEU test→ run at Legnaro Sirad facility
Higher dose TID test on planning

Outlook

TIGER, in silicon electrical characterization

main result! a second prototype is not needed,

minor revisions in engineering run (summer 2017)

First tests with cylindrical GEM & first signals acquired!

S/H dynamic range, noise under study

data analysis ongoing

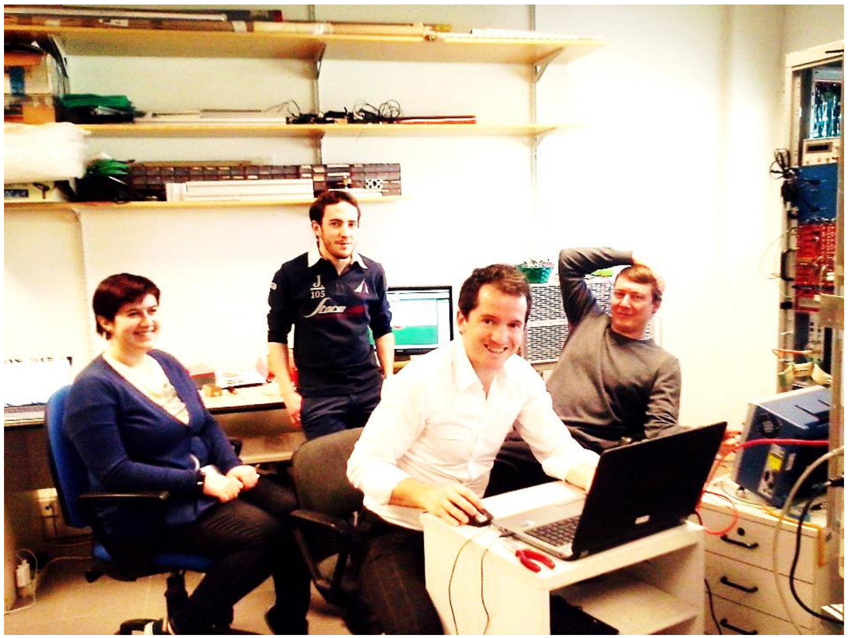
→test with conditions more similar to final ones,

in terms of HV distribution system, FE cards, etc.

Radiation hardness tests:

Good results from first tests on voltage regulators

SEU and other TID tests on planning



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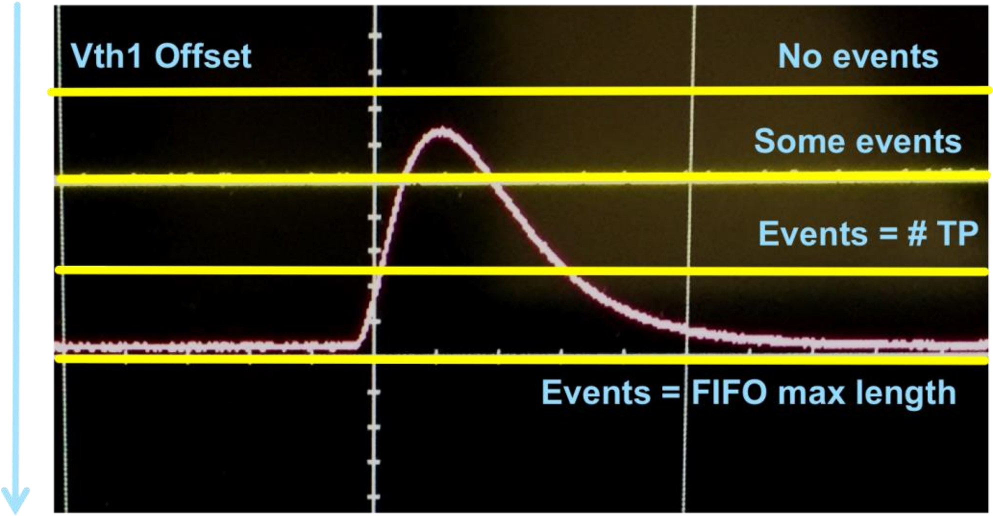
HORIZON 2020

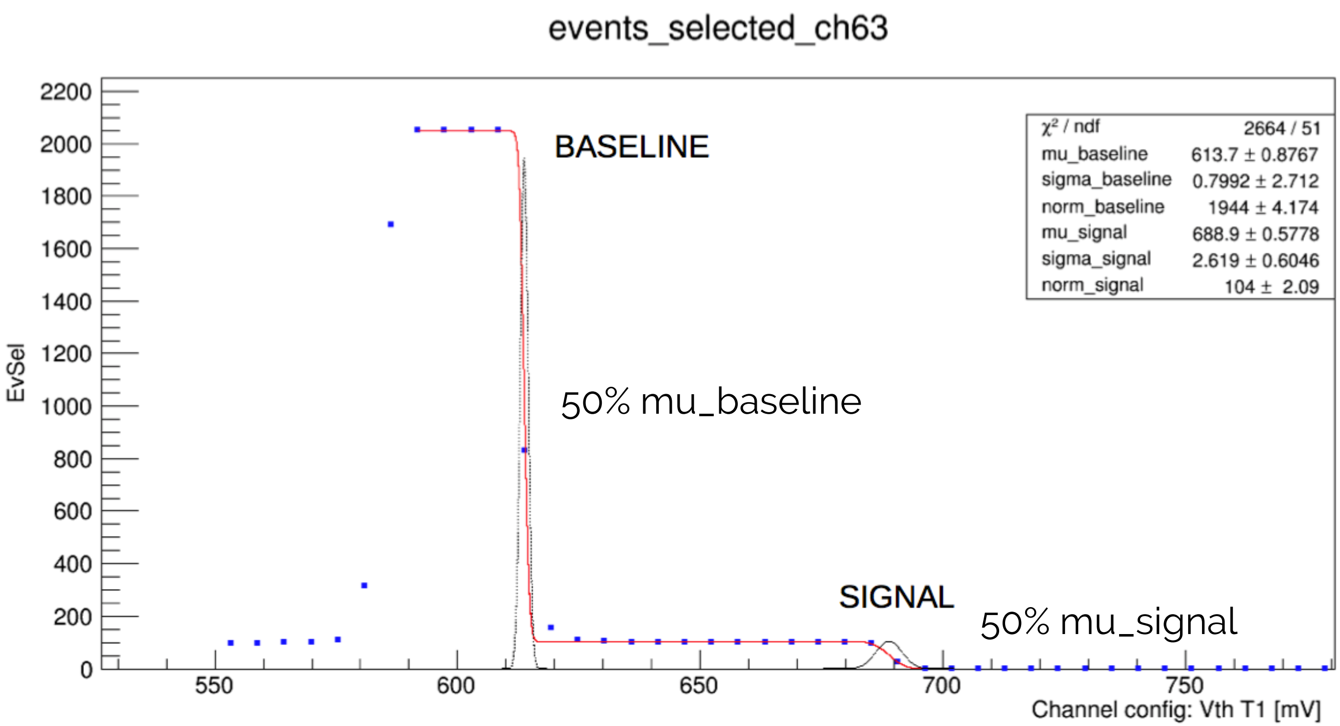
Torino TIGER WG

Fabio Cossio, Marco Mignone, Angelo Rivetti
Manuel Rolo, Richard Wheadon
Maxim Alexeev, Martina Gertosio
Michela Greco, Simonetta Marcello

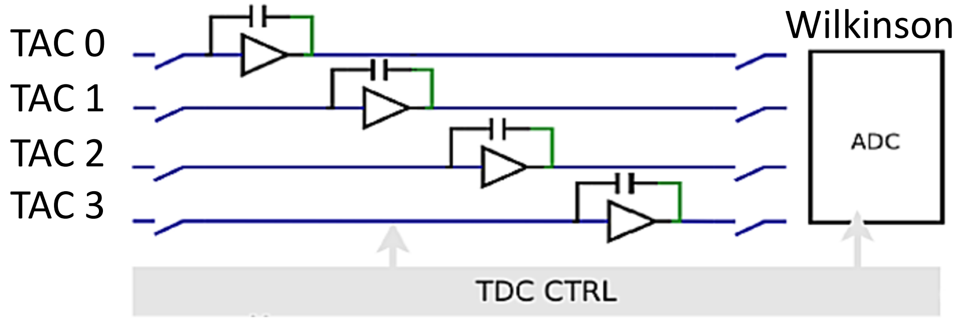
Thank_you

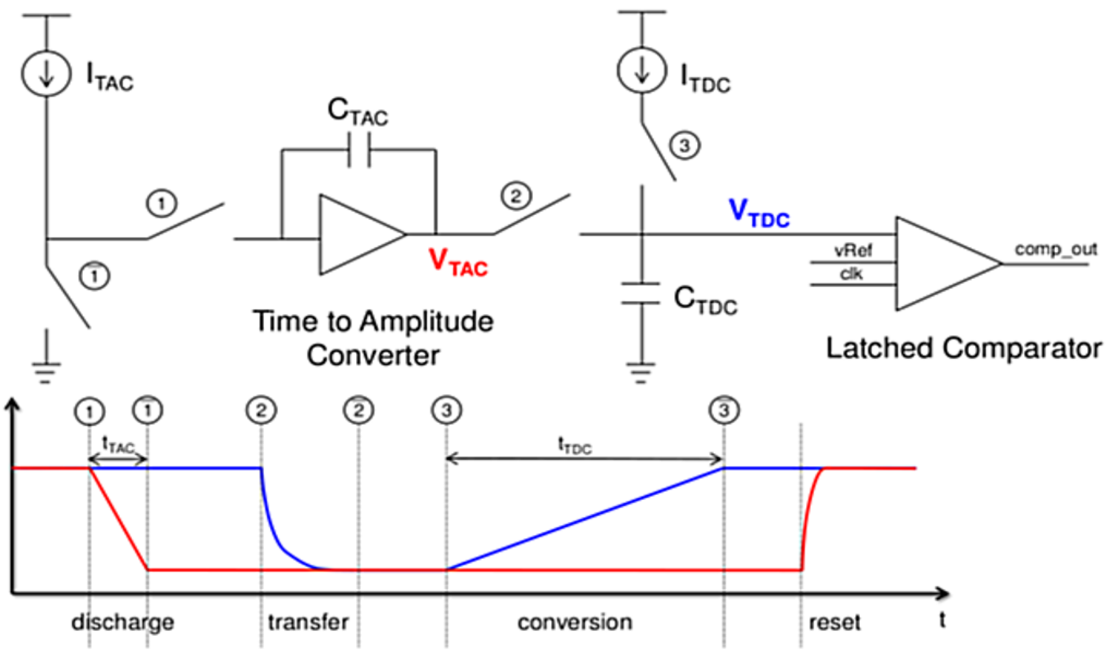
Baseline scan





TDC





Both TAC and S/H circuits employ a quad-buffer scheme to de-randomize the input event rate and lessen the issue of the inherently high conversion time of this approach.

K28.1	10	channel 6 bit	tac	T_coarse 16 bit	E_coarse 10 bit	T_fine 10 bit	E_fine 10 bit