A custom readout electronics for the CGEM detector

Michela Greco
CGEM-IT group
Outline

Introduction

Overview of the readout electronics for the BESIII-CGEM IT

On detector electronics
  Design of a dedicated ASIC for CGEM Readout (TIGER)
  In silicon characterization of TIGER prototype
  First tests on CGEM detector

Outlook
CGEM Inner Tracker readout

- **Charge centroid method**
  - Digital Readout
  - **Analog Readout**
    Loosening pitch (650 µm) & less channels (about 10 thousand)

- **µTPC (Time Projection Chamber)**
  time resolution 5 ns

- **Jagged anode**

- **µTPC (Time Projection Chamber)**
  - Readout with 160 dedicated, integrated 64-channel ASICs
The BESIIICGEM project has been funded by European Commission within the call H2020-MSCA-RISE-2014.
Expected signal from CGEM-IT:
30-50 ns duration,
30-40 ns rising time, 10 ns falling time
depends on gas mixture, gain and electric field

- input charge: 1 - 50 fC
- up to 100 pF sensor capacitance
- 4-5 ns time resolution
- 60 kHz rate per channel
  (safety factor of 4 included)
- power ~10 mW/channel

25 mm² UMC110 CMOS

provide time and charge measurement,
feature a fully-digital output
be SEU-tolerant
64 channels: VFE, signal conditioning, TDC/ADC, local controller on-chip bias and power management on-chip calibration circuitry fully digital output, LVDS IO 4 TX SDR/DDR links, 8B/10B encoding, 200 MHz SPI configuration link
Each channel

![Diagram of a readout system](image)

**T-BRANCH**
timestamp on rising/falling edge (sub-50 ps binning quad-buffered TDC)
charge measurement with Time-over-Threshold

**E-BRANCH**
timestamp on rising edge (sub-50 ps binning quad-buffered TDC)
Sample-and-Hold circuit for peak amplitude sampling
slow shaper output voltage is sampled and digitised with a 10-bit Wilkinson ADC
Test setup
Characterization runs in summary

- R/W Channel/Global configuration registers
- Data TX and decoding
- Baseline and threshold equalisation

(dual-) TDC operation

Front-end performance
internal calibration circuitry
external charge injection (channel 63)

unexpected amplifier baseline shift,
may limit linearity of Sample and Hold

→ operation at higher temperature to recover BL shift
TDC operation: quantization error

Scan over dynamic range sweeping internal test-pulse phase
Create LUT with gain and offset correction
⇒ Average TDC quantization error after calibration: 30-35 ps r.m.s.
Timing performance: jitter

Jitter measurements using internal calibration circuit test-pulse (e.g. 10 fC) sweeping input capacitance on channel 62
Timing performance: jitter

Jitter measurements using internal calibration circuit test-pulse (e.g. 10 fC) sweeping input capacitance on channel 62
Noise measurements

Noise evaluated for each input capacitance through a sigmoid fit from a typ 500 points threshold-scan with fixed test-pulse (10 fC)
Measure repeated typ 50 times
Evaluated on channel 63 using an external pulse generator

**Gain: 10.4 mV/fC** in agreement with simulations (expected ~11 mV/fC)
Charge measurements: Sample and Hold

Calibration of dynamic range with external test-pulse generator
Back-annotation to generate a parameter space for the internal calibration circuit

→ Linearity checked
→ Dynamic range: 510-520 mV

Charge measurement below 5 fC measured with double-threshold operation (one-channel only)
Time-based readout working properly

**Baseline dependence on temperature**
root cause: fragility of bias conditions of baseline holder circuit
reproduced fairly well in simulations
minor revision activities started

**Charge measurement: S/H linearity assessed**

**Main result: no second prototype needed**

➔**GEM testing**
to assess the performance as it explores a realistic grounding and noise pick-up environment.
GEM testing

17
First signals with 90-Sr source
First signals with cosmic rays (night acquisition)
Noise VS ch

Noise in LSB

sigma_vs_ch
Entries: 64
Mean: 31.42
RMS: 18.65

noise_LSB
Entries: 64
Mean: 2.603
RMS: 0.7857

V strips
X strips

LSB = 3.1 mV

→ sensitivity to grounding

GEM foil
Radiation hardness at CERN GIF++ facility

Test board irradiated to about 30 krad to test radiation damage on Voltage Regulators

Test board irradiated to about 30 krad to test radiation damage on Voltage Regulators

Analog power: TPS78601KTTT, TPS78601DCQ
Digital power: TPS78601DCQ, TPS78625DCQ

<table>
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<th></th>
<th>PRE (V)</th>
<th>POST (V)</th>
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<tr>
<td>Analog power</td>
<td></td>
<td></td>
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<tr>
<td>T1</td>
<td>1.232</td>
<td>1.222</td>
<td>0.992</td>
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<tr>
<td>T2</td>
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<tr>
<td>Digital power</td>
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<tr>
<td>T3</td>
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<tr>
<td>T4</td>
<td>2.505</td>
<td>2.488</td>
<td>0.993</td>
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LT3021 for Voltage reference

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<th>PRE (V)</th>
<th>POST (V)</th>
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<td>Vref (T5)</td>
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<td>Vblh (T7)</td>
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<td>Vout_th</td>
<td>0.575</td>
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<td>Vout_y</td>
<td>0.506</td>
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<td>0.988</td>
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-0.7/0.8 % ok!

we will have resistor voltage dividers

SEU test → run at Legnaro Sirad facility
Higher dose TID test on planning
**TIGER, in silicon electrical characterization**
main result! a second prototype is not needed, minor revisions in engineering run (summer 2017)

**First tests with cylindrical GEM & first signals acquired!**
S/H dynamic range, noise under study
data analysis ongoing
→ test with conditions more similar to final ones, in terms of HV distribution system, FE cards, etc.

**Radiation hardness tests:**
Good results from first tests on voltage regulators
SEU and other TID tests on planning
The BESIIICGEM project has been funded by European Commission within the call H2020-MSCA-RISE-2014.
Baseline scan

**Vth1 Offset**

- No events
- Some events
- Events = # TP

**Events = FIFO max length**

**events_selected_ch63**

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**BASELINE**

- 50% mu_baseline

**SIGNAL**

- 50% mu_signal

M. Greco, MPGD2017, 23 May 2017
Both TAC and S/H circuits employ a quad-buffer scheme to de-randomize the input event rate and lessen the issue of the inherently high conversion time of this approach.