VMM discussion

Michael Lupberger (CERN)

SRS + VMM

Poster by George Iakovidis

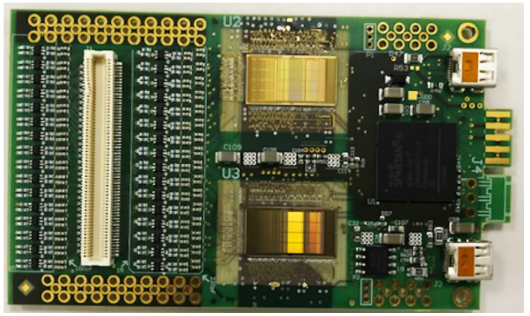
FECv6 with D-Card connects to VMM hybrids

VMM ASIC: Readout chip for ATLAS NSW

- 130 nm CMOS technology
- VMM3 delivered: end 2016
- Configuration via CMOS lines (data+clock)
- 64 channels (preamp and shaper, ADCs)
- Output: digitised data (38 bit/hit), 0-supp.
- Up to 200 MHz clock
- Self triggered

VMM hybrid:

- Two VMM ASICs
- Spartan6 FPGA
- LDOs for power
- Protection circuit



Adapter card:

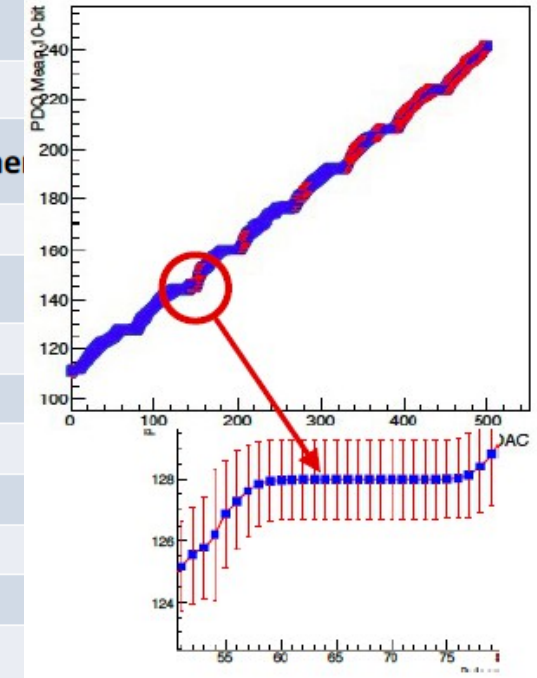
- Mainly SVDS drivers
- Can read up to 8 VMM hybrids
- Work on possible master/slave ongoing

VMM

By George Iakovidis

News from ATLAS (from RD51 Miniweek)

Issue in VMM2	Circuit	Status in VMM3	Notes
Handling sTGC rates	analog front-end	⚑	-
Early saturation	current-out peak detector	⚑	-
ADC accumulation	ADCs	⚑	improveme
Pulser DAC saturation	DAC bias circuit	⚑	-
Pulser rise-time and noise	pulser circuit and injection switch	⚑	-
Prompt output disabled	control logic	⚑	-
Event loss	ADC reset logic	⚑	-
Threshold bit error	discrimination logic	⚑	-
BCID advance-latch issue	Gray-code counter	⚑	-
Other data integrity issues	data, token & FIFO logic	⚑	-
Counter turnaround	counter logic	⚑	-
Front-end off w/SFM	analog front-end	⚑	-
Peak detect hold time	hold node		not tested
Buffer float at bypass	buffer input stage	⚑	-
High baseline (5% samples)	baseline stabilizer	(⚑)	yield, workaround

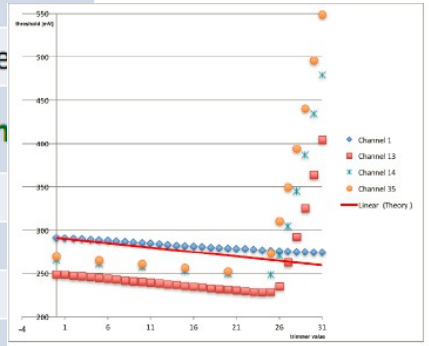


VMM

By George Iakovidis

News from ATLAS (from RD51 Miniweek)

New Function in VMM3	Circuit	Status in VMM3	Notes
Handle sTGC capacitance & charge	analog front-end	⚑	impact of protection resistor
Tail cancellation	analog front-end	⚑	-
Trimming range extension	trimmer analog/logic	⚑	3/4 of targeted
L0 handling logic	digital implementation	⚑	stress tests in progre
Simultaneous readout	various logic changes	(⚑)	locking, workaroun
CMOS IOs config. and new reset	config. logic and IOs	⚑	-
SLVS-400 IOs	digital interface	⚑	-
Timing ramp optimization	timing circuit	⚑	-
Timeout ramp autoreset	timing circuit	⚑	-
Acquisition reset on ENA	control logic	(⚑)	single event, workaround
32-channel skip	inter-channel logic	⚑	-
ART flag synchronization	ART logic	⚑	-
SEU tolerance	logic		tests queued
Pulser range extension	injection circuit	⚑	-
Timing ramp at threshold	timing circuit	⚑	-



VMM

By George Iakovidis

News from ATLAS (from RD51 Miniweek)

- VMM3 is being **extensively tested** at several institutions, and five residual issues have been found two from VMM2 still present in smaller amount:
  - ➡ **ADC resolution (10b > ~7b and 8b > ~6b)**
  - ➡ **trimming (3/4 of planned extended range)**

  thee have a workaround
  - ➡ **direct output locking in ToT, workaround TtP**
  - ➡ **acquisition reset on EN, workaround CS**
  - ➡ **5% high analog baseline, workaround STLC**
- **VMM3 solved all readout stability issues we found in VMM2, added many more features**
- VMM3 will be tested for SEU in Democritus Greece under Neutron irradiation in Spring 2017
- **Revision to fix residual issue recommended**, if schedule allows on May 2014 (Going to production for ATLAS) although the current version looks that it is enough good for trigger + readout (charge & timing measurements of high precision).

VMM

Clarification

From Vinnies summary slide @ Mini week in December

- No export license needed
  - CERN working for a universal license for all ASICs fabricated by Global Foundries, please check with P. Farthouat

Triggered fear/misunderstanding regarding availability of VMM for certain regions = export restrictions

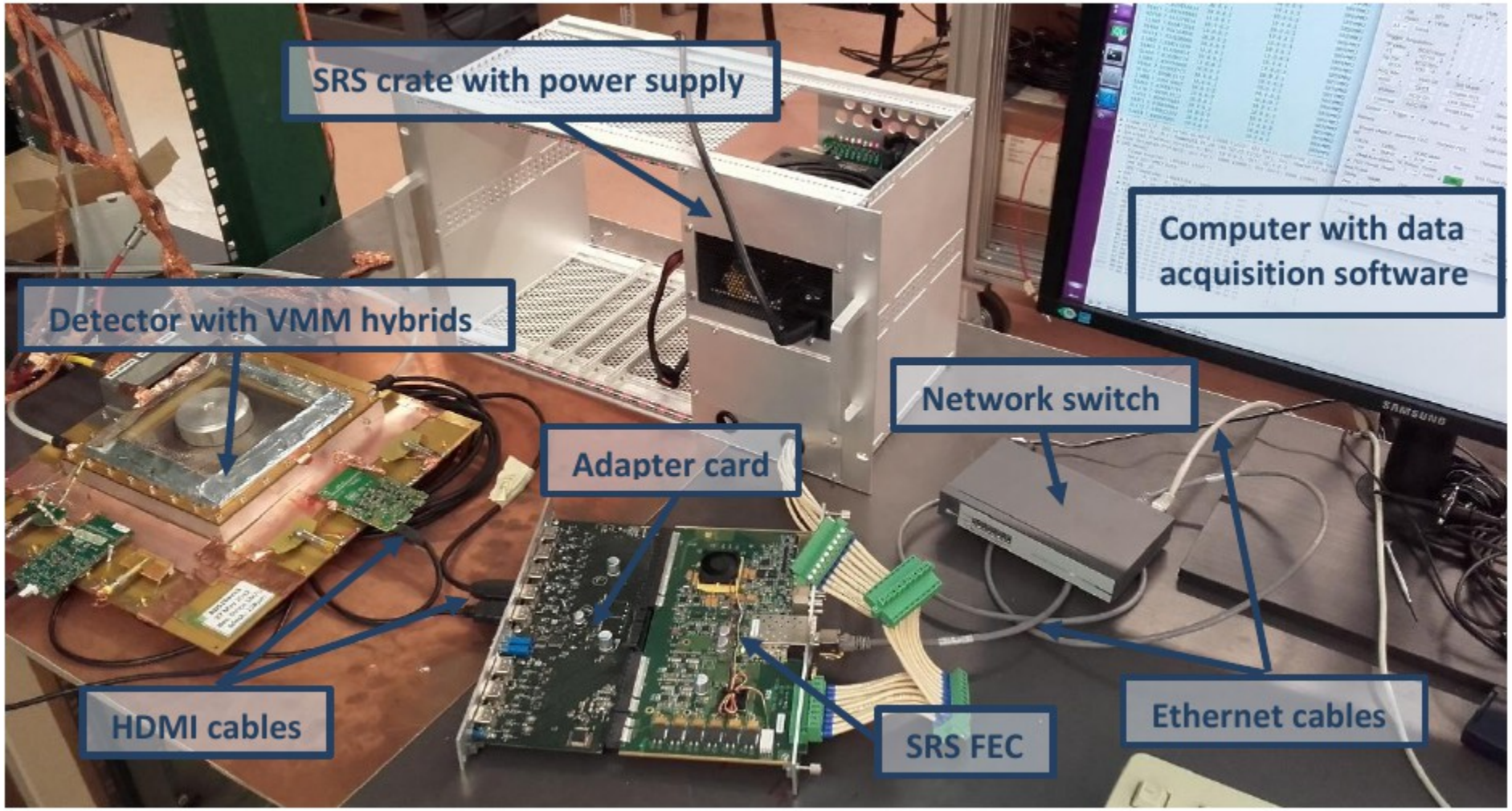
George and Vinnie solved this misunderstanding:

- CERN works on license for all Global foundries chips
- VMM might be included if this puts no limitations
- BNL works on license with goal: no export restrictions

VMM3 production: ATLAS is working on it

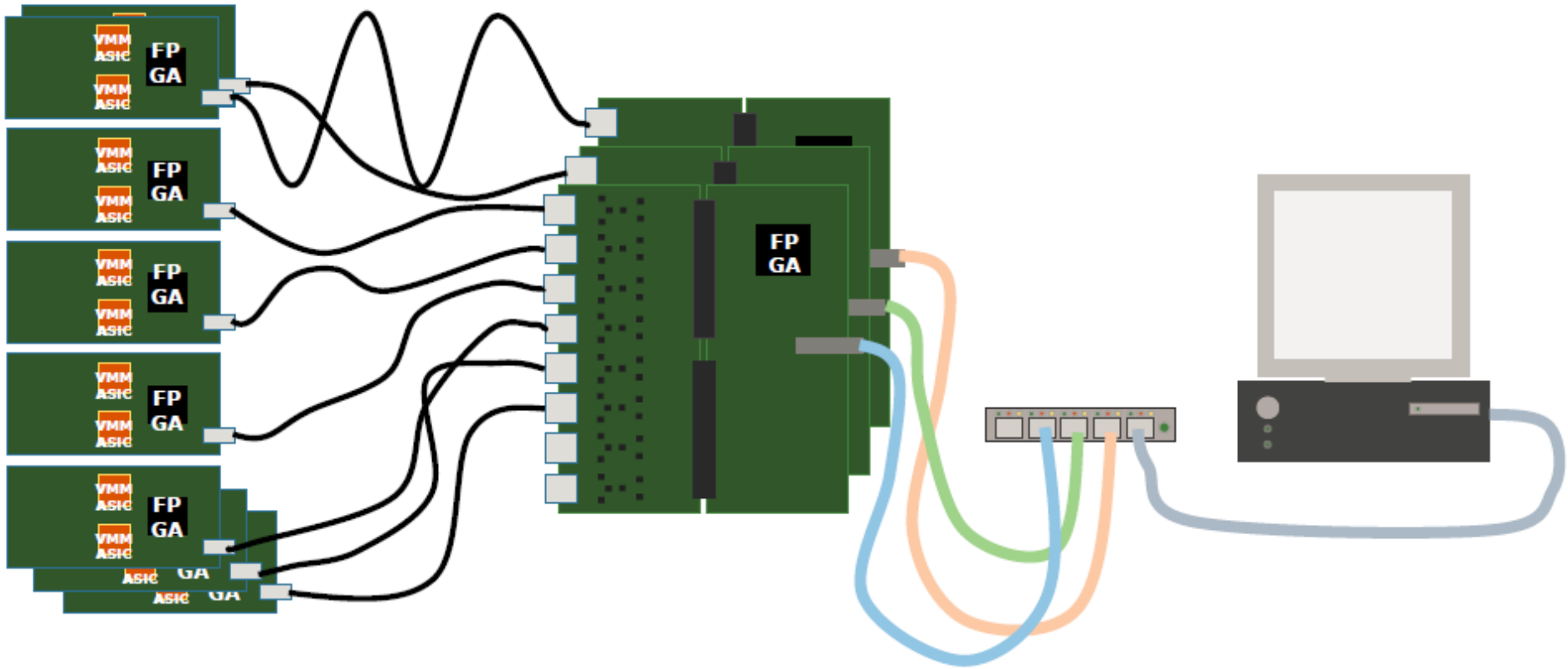
SRS + VMM

Detector electronics chain



SRS + VMM

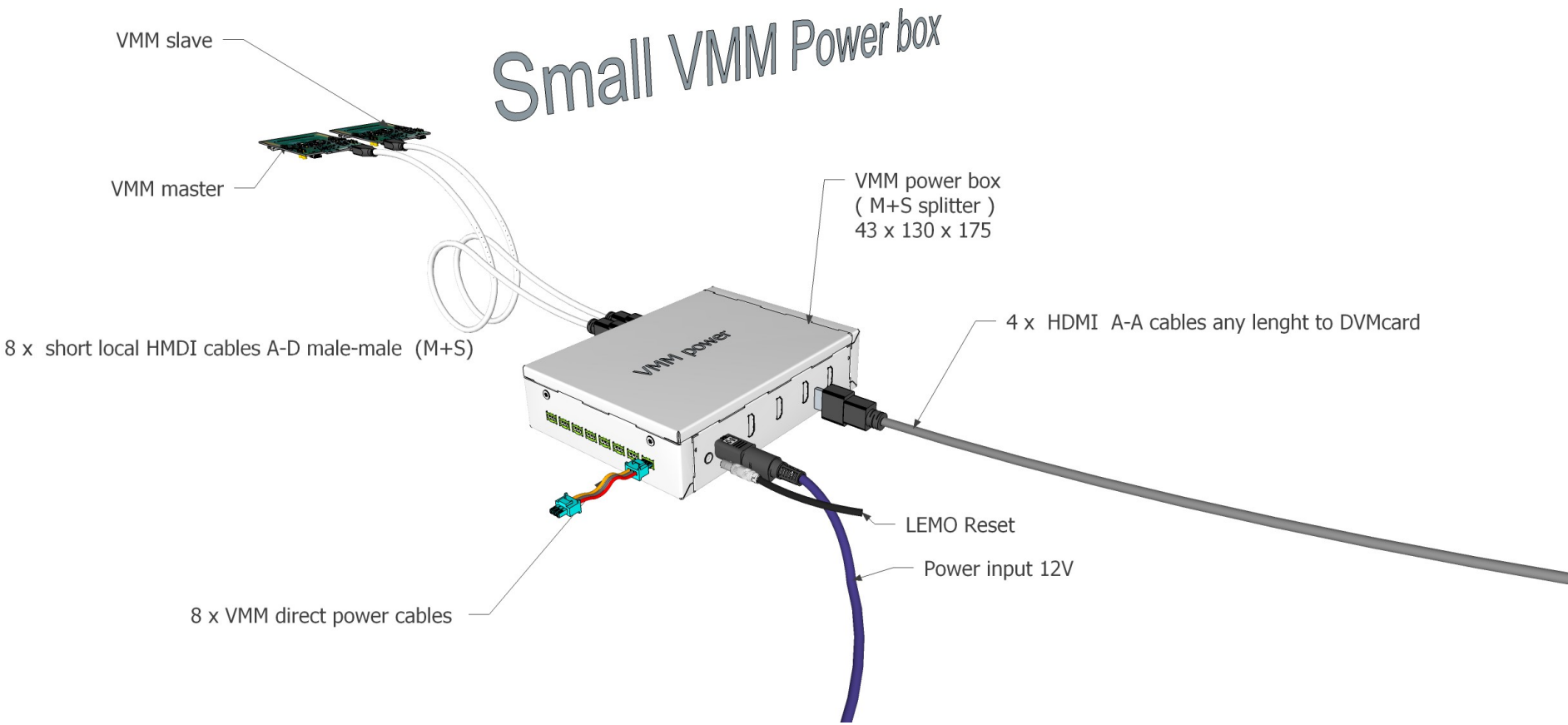
Detector electronics chain



VMM Hybrid → HDMI cable → Adapter card + FEC → Ethernet → Switch →Ethernet → PC

SRS + VMM

High VMM power consumption: Power Box



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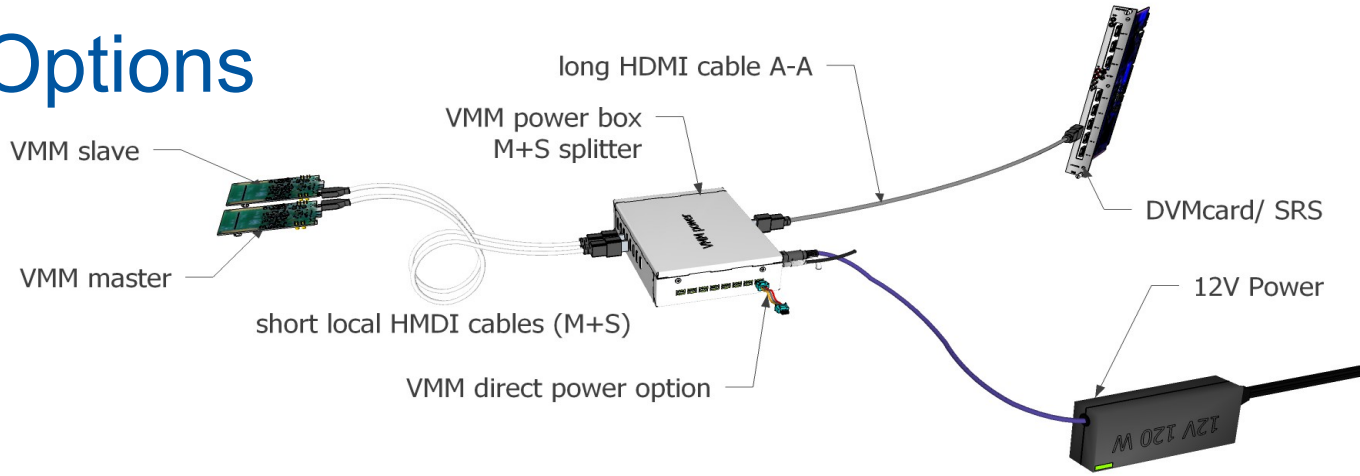
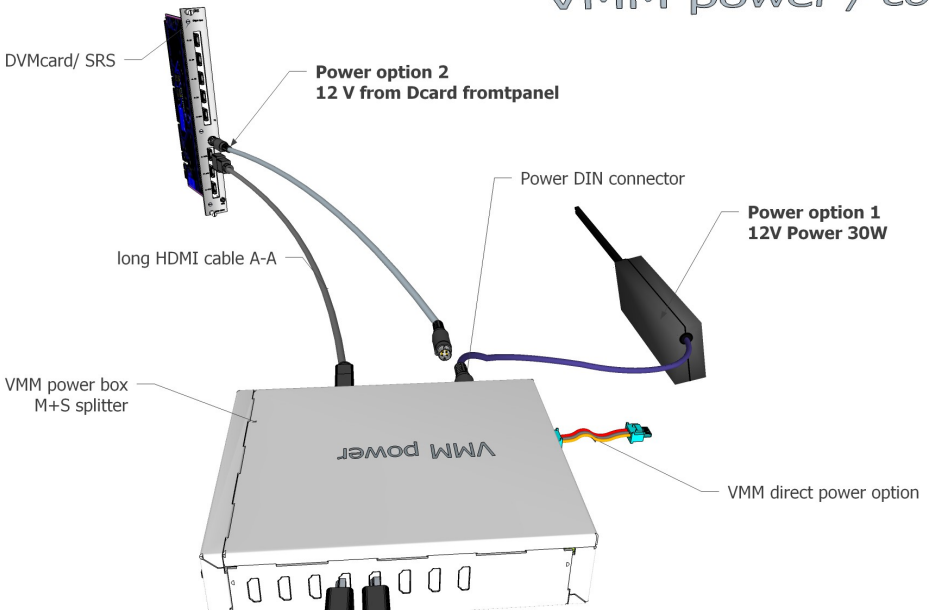
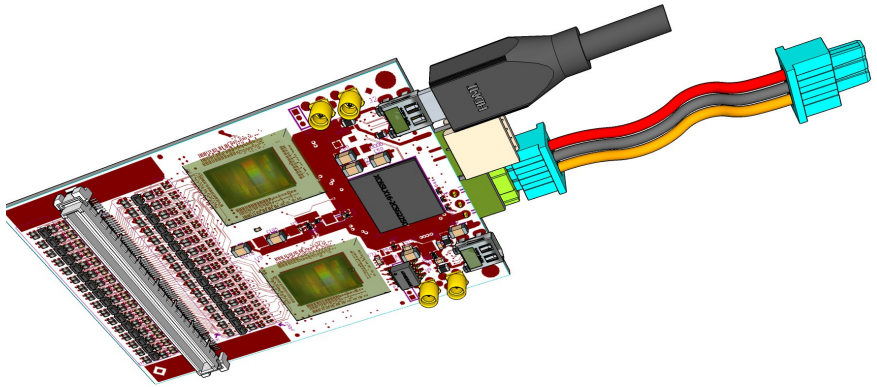
Power Box: Options



VMM power / connectivity plan

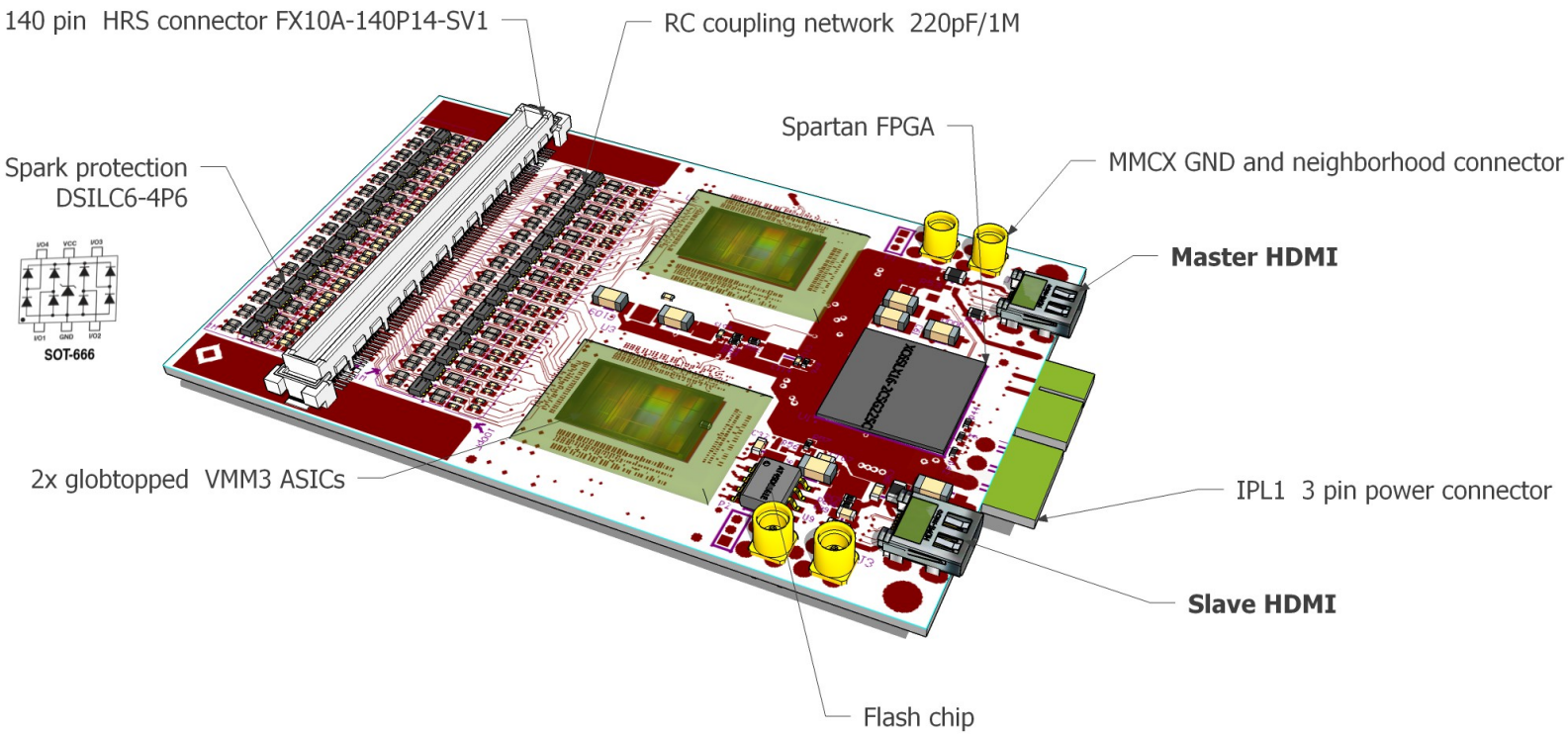
2k VMM channels =1 DVM/FEC
16 VMM hybrids
max 50 Watt





SRS + VMM

VMM3 hybrid with new connector



VMM

Availability

VMM3

- 4 hybrids at CERN
- ~32 VMM3 in stock, possibility to get 1-2 dozen more

  could build 16 up to 30 more hybrids (still on Panasonic)

more VMM3

- Low quantities: join next ATLAS production for prototypes
- Large quantities: join ATLAS NSW mass production

SRS + VMM

Availability

D-Card:

- 2 at CERN + 1 that needs to be fixed
- For final version: minor power routing and outline changes

FEC

- You will need the FECv_6
- Available at CERN store or directly from Samway also via SRStechnology.ch
- Power box: one prototype

SRS + VMM

Manpower at CERN GDD

- Alex Rusu: (VMM hybrid, Dcard) (25% for 3 month by ESS)
- Hans: (50% @ CERN GDD lab as unpaid member)
- Michael Lupberger: 100% @CERN GDD lab

very limited → need help from the community / possible users

Things to be done:

- Master/Slave option with boundary conditions: use with power box, master only when directly connected to D-Card, hybrids must be identical, (FPGA code must be identical)

  → upgrade VMM to M/S mode (FPGA code) make Dcard M/S capable (power routing)

- VMM Cooling, Panasinic-Hirose adapter, ...

SRS + VMM

VMM3 hybrid first price estimate by Alex

no guarantee

- ~ factor 2 more compared to APV25 when in production
- Depends on production quantities:
  - >500 hybrids → 250 chf/hybrid (~2x APV25)
  - 100 hybrids → 450 chf/hybrid
  - 50 hybrids → 680 chf/hybrid
  - 10 hybrids → 920 chf/hybrid (APV25 protos where about the same)
  - 1 hybrids → 4000 chf/hybrid

Need small quantity phase for prototyping before large production

SRS + VMM

VMM3 ASIC RD51 order

- Next production (small quantities)
- ATLAS mass production

Request received:	ASICs
- Lev Shekhtman (Novosibirsk):	4/20
- Dorothea Pfeiffer (ESS):	24/96