TDC in ACTEL FPGA continued

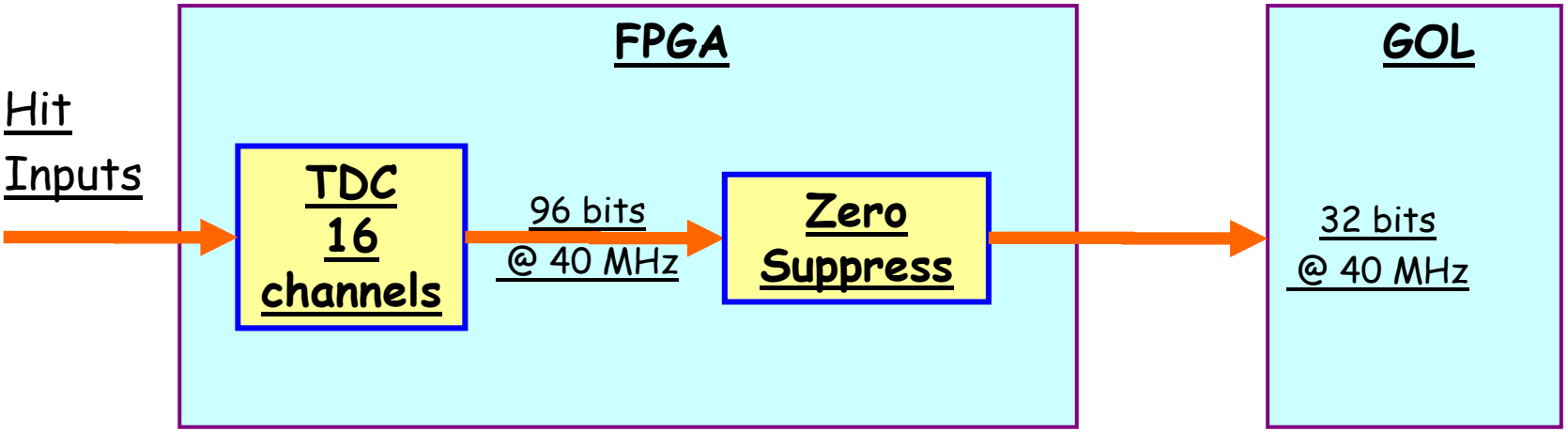
Preliminary

Tom Sluijk
Hans Verkooijen
Albert Zwart
Fabian Jansen

To be done

- Increase the number of channels to 16.
- Connect the TDC to a GOL to get better analyzing possibilities.
- Tests:
  - Linearity
  - DNL
  - Temperature

Test Setup


FPGA
GOL
Hit
Inputs
TDC
16
channels
96 bits
@ 40 MHz
Zero
Suppress
32 bits
@ 40 MHz

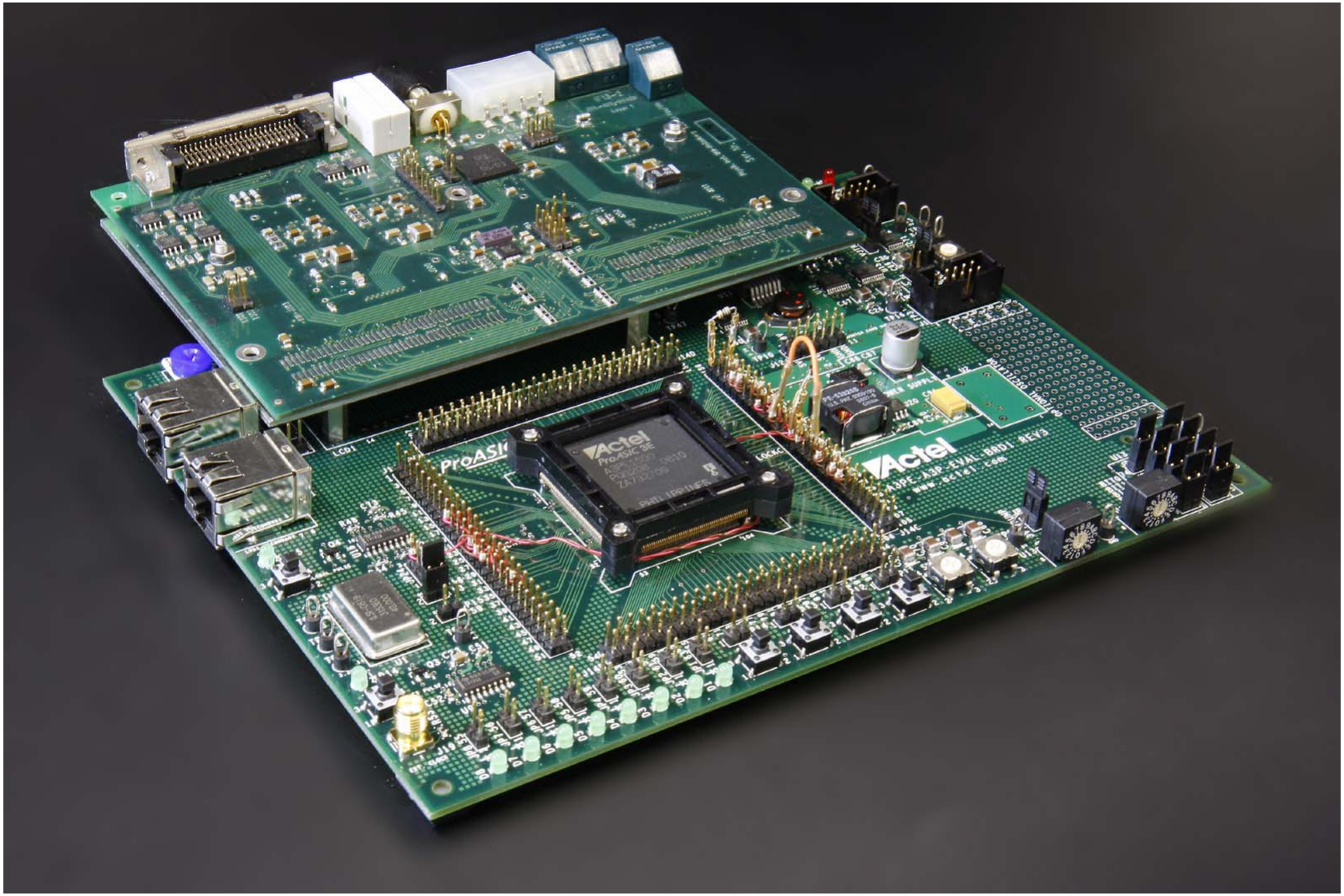
Zero Suppress

- Simple zero-suppress scheme implemented now
  - If one hit in a Bx is valid, the data of all 16 channels is sent to the GOL.
- The Event Data:
  - Header.
  - 64 bits Fine time (4 bits per channel).
- Header:
  - Hitpattern (16 bits).
  - Bx counter.
  - Status Flags

Compile Report

- CORE Used: 2239 Total: 38400 (5.83%)
- IO (W/ clocks) Used: 63 Total: 147 (42.86%)
- Differential IO Used: 0 Total: 65 (0.00%)
- GLOBAL (Chip+Quadrant) Used: 4 Total: 18 (22.22%)
- PLL Used: 1 Total: 2 (50.00%)
- RAM/FIFO Used: 48 Total: 60 (80.00%)
- Low Static ICC Used: 0 Total: 1 (0.00%)
- FlashROM Used: 0 Total: 1 (0.00%)
- User JTAG Used: 0 Total: 1 (0.00%)

Test Assembly



Results up to now

- Backannotated simulations are performed and it works fine.
- No data taken yet.