PLANS FOR FPGA IRRADIATION and TESTING

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OUTLINE:

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2. Plans @ Syracuse
3. Irradiation Facilities
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IRRADIATION LEVELS

Irradiation level for FPGAs near VELO

- Current best estimate of expected irradiation of VELO sensor for $100.fb^{-1}$
- Extrapolate from sensor to 1 m distance (approx. location of repeater cards)
- Get: 20–70 MRad / $100.fb^{-1}$

  or $(0.5–1.5)\times10^{15}$ neq/cm^2 / $100.fb^{-1}$

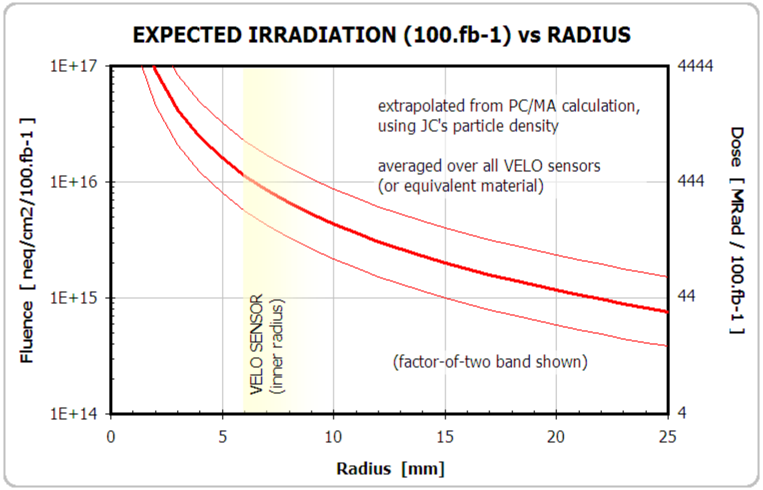
  (Range is envelope of different extrapolation methods)
- Large and problematic number

Irradiation level for FPGAs elsewhere

- In nearby corridor (requires some additional shielding), cable distance ~10 m
- At balcony, cable distance ~20 m
- Either location gives few kRad/10.yr, which scales up to: few 10 kRad / $100.fb^{-1}$
- More manageable level

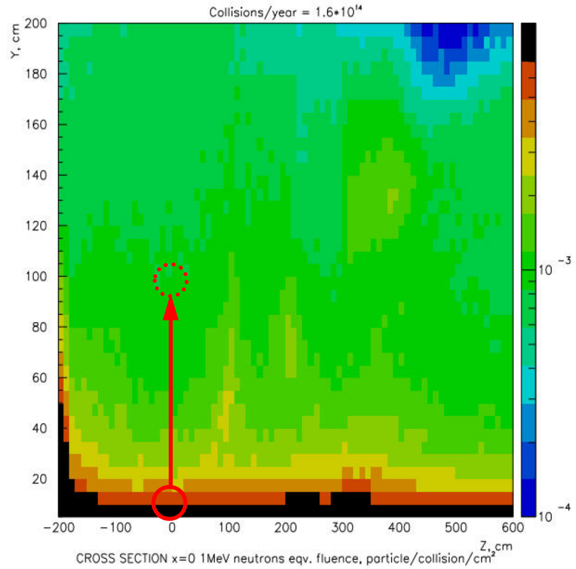
Intermediate FPGA for Multiplexing - van Beuzekom - velo.upg.081114

Sets scale of problem for VELO upgrade



VELO Upgrade News - Collins - velo.upg.090324

1 MeV neq fluence map in vertex region



(REF: $100\ fb^{-1} = 5$ yr @ 2×10^{33})

LHCB Radiation Background - Corti & Shekhtman - lhcb-2003-083

PLANS @ SYRACUSE

Just at the beginning of our program at Syracuse…

Purpose: To investigate likely FPGAs for use in VELO upgrade (specifically but not exclusively for pixel application)

Actel RTAX-S series (radiation tolerant)

RTAX-S/SL offers high performance at densities of up to 4 million equivalent system gates and 840 user I/Os for space-based applications. The RTAX-S/SL family, the leading Actel product offering for space applications, features SEU-hardened flip-flops implemented without any user intervention, and offers the benefits of user-implemented triple module redundancy (TMR) without the associated overhead.

Xilinx Virtex-4 QPro-V series (radiation tolerant)

Summary of Radiation-Tolerant Virtex-4 QPro-V Family Features

- Full V-Grade manufacturing and process flow
- Guaranteed operation over full military temperature range (–55°C to +125°C)
- Guaranteed 250 krad (Si) total ionizing dose per method 1019
- Guaranteed SEE latch-up Immunity to LET > 100 MeV/mg-cm^2 per method 1020
- Fully characterized for space radiation effects in heavy ion and proton environments
- SEU mitigation support with TMRTool software
- Fully tested configuration management IP cores available.
- High reliability ceramic flip-chip packaging technology
- Three device architectures: LX/SX/FX
  - XQR4VLX200:
    - High-density logic applications solution
    - Over 200,000 logic cells
  - XQR4VSX55:
    - High-performance solution for digital signal processing (DSP) applications
  - XQR4VFX60/140:
    - High-performance, full-featured solution for embedded processing platform applications
- Xesium clock technology
  - Digital clock manager (DCM) blocks
  - Additional phase-matched clock dividers (PMCD)
  - Differential global clocks
- XtremeDSP slice
  - 18 x 18, two's complement, signed multiplier
  - Optional pipeline stages
  - Built-in accumulator (48-bit) and adder/subtracter
- Smart RAM memory hierarchy
  - Distributed RAM
  - Dual-port 18-Kbit RAM blocks
  - Optional pipeline stages
  - Optional programmable FIFO logic automatically remaps RAM signals as FIFO signals
  - High-speed memory interface supports DDR and DDR2, SDRAM, QDR-II, and RLDRAM II.
- SelectIO™ technology
  - 1.5V to 3.3V I/O operation
  - Built-in ChipSync™ source-synchronous technology
  - Digitally controlled impedance (DCI) active termination
  - Fine-grained I/O banking (configuration in one bank)
- Secure chip AES bitstream encryption
- 90-nm copper CMOS process
- 1.2V core voltage
- IBM PowerPC RISC processor core (FX only)
  - PowerPC 405 (PPC405) core
  - Auxiliary processor unit interface (user coprocessor)
- Multiple Ethernet MACs (FX only)

Basic plan:

– Spec out a likely FPGA
  - Actel RTAX-S series
  - Xilinx Virtex-4 QPro-V series
– Construct a mini-daq with prototype board
– Develop coding to configure and exercise chip
  - Bench tests to validate procedures for measurements to be made (given below)
– Develop and test irradiation setup
  - Mechanical, cooling, power, etc.
– Move to irradiation facility (see next slide)
– Irradiate it
– Tests to be made:
  - Irradiate device with power on and
  - Configure / read back configuration file to determine probability of corruption of static registers
  - Write / read back dynamic registers to measure SEU rate (e.g. counting)
  - Measure SEE cross-sections for bit-flips, configuration loss, latch-up, transient effects, high-speed operation, etc.
– Establish mitigation strategies, etc.
– Iterate with other likely FPGAs as necessary

SUMMER

FALL

IRRADIATION FACILITIES

IRRADIATION FACILITIES							
Facility	Radiation Source	Irradiation Level	Exposure [MRad/hr]	Time (min) 50 MRad	Used by...	Ref.	Comments
HADRONS							
IUCF Indiana University Cyclotron Facility, Bloomington IN USA	30–200 MeV **p** (Cyclotron)	1e2–1e11 p/cm2.s (3.6e14 p/cm2.hr max)	9.6	5.2 hr $ 3,266	many	IEEE.REDW(08)21 www.iucf.indiana.edu/rerp/	DD tests, RERS-1,2 p beamlines, max p flux has 2 cm spot diam, beam available 0700-1900 (12 hr day), max 1e11 only available at night and sometimes on weekends, exposure durations: a few seconds upward routinely available
IUCF Indiana University Cyclotron Facility, Bloomington IN USA	**n** from 13 MeV p (PL-7 Linac)	4e8 neq/cm2.s (1.5e12 neq/cm2.hr)	0.07	750 hr $ 470,250	many	IEEE.REDW(08)21 www.iucf.indiana.edu/rerp/	DD, SEU (n), LENS/NREP, n-flux at max pwr 10 cm from moderator chamber >1e11 n/cm2.s (exp), dose for 1e10 n/cm2 fluence 10 cm from moderator chamber <3 rad (Si) (per sec?), prod Be(p,n)X cont E spectrum
CERN Irradiation Facility, PS, East Hall, CERN, Geneve CH	24 GeV/c **p** (CERN-PS IRRAD-1/3/5)	1–3e13 p/cm2.hr (~2–9e9 p/cm2.s CB)	0.80	62.5 hr ?	many	irradiation.web.cern.ch	irrad area ~ 2 x 2 cm2, min ~ 1.5e11 p/spill, CPS==> 14 or 18 cycles of 1.2 s, 1 EASTA or 1 EASTC = 2 cycles (2.4s), 1 slow extraction = 400-500 ms
CERN Irradiation Facility, PS, East Hall, CERN, Geneve CH	**n** from 25 GeV/c p (CERN-PS IRRAD-2/4/6)	0.3–1e12 neq/cm2.hr (~1–3e8 neq/cm2.s CB)	0.04	1125 hr ?	many	irradiation.web.cern.ch	max sample size is ~ 30 x 30 x 30 cm3, possibile to have electrical cabling, IRRAD-2: fast n ~1.MeV (down to 50 KeV?), IRRAD-4: slow n, IRRAD-6: mixed hadrons (p p+ p- n g) for TID, SEE, etc
Boeing Radiation Effects Laboratory (BREL), Space & Defense Sytems, Seattle WA USA	14 MeV **n** (Kaman A711 n-generator)	1e10 n/cm2.s monoenergetic 14 MeV			JPL	IEEE.REDW(08)21 www.boeing.com/assocproducts/radiationlab/	Target area (max) limited only by room and doorway
Sandia National Labs, Albuquerque NM USA	1 MeV eq **n** (SPR-III reactor)	8.9e12 n/cm2.s 1 MeV Si equiv	1424.0	0.04 hr $ 3,561	Boeing		
Ljubljana Neutron Irradiation Facility, Reactor Center, Jozef Stefan Institute, University of Ljubljana, Ljubljana SI	**n**, cont. E spectrum (TRIGA Mark II reactor)	< 5e12 n/cm2.s fast n	~9.2 ?	5 hr	LHCB, RD50		fast neutrons (E>100 keV), damage constant 0.9, thermal (E<0.5 eV), flux ratio thermal/fast ~ 2; irrad areas: circ r=2.2 cm, ellipse r = 5, 7 cm by 15 cm max len;
Louvain-la-Neuve, Université Catholique de Louvain, Centre de Recherche du Cyclotron (CRC), Institut de Physique Nucléaire, Louvain BE	**n** from 50 MeV d (isochronous cyclotron)	6.6e12 n/cm2.s typ 20.4 MeV ave (T2-line)	~12.2 ?	4 hr	RD50	www.fynu.ucl.ac.be/themes/he/RD50/	neutrons from 9Be(d,n)X using 50 MeV deuteron beam and subsequent induced activity foil interactions;

NOTES: - REDW = Radiation Effects Data Workshop

SOLICITATION

Would like to gather together a list of what people are interested in doing in terms of irradiation tests. Useful input:

- Which device(s) you want to irradiate
- Level of irradiation expected at the location of your FPGA
- What irradiation species (p,n) you prefer
- Specification of tests of interest to your group
  - List out details of what it is you want to test, and how to test it
  - Can we develop common algorithms to spec all devices? Establish common criteria for acceptable irradiated FPGA performance?
- Configuration files relevant to your application
- Rough schematic of system to be tested (dimensions, requirements in terms of services, etc.)
- Rough schedule of when you think it would be available for irradiation.
  - Syracuse plans are for irradiation in Fall 2009
- Assume apparatus self-contained and transportable to remote site
- Other issues of common interest?

⇨ will circulate an email request for this info