The CBM Silicon Tracking Station and CBM-related ASIC developments

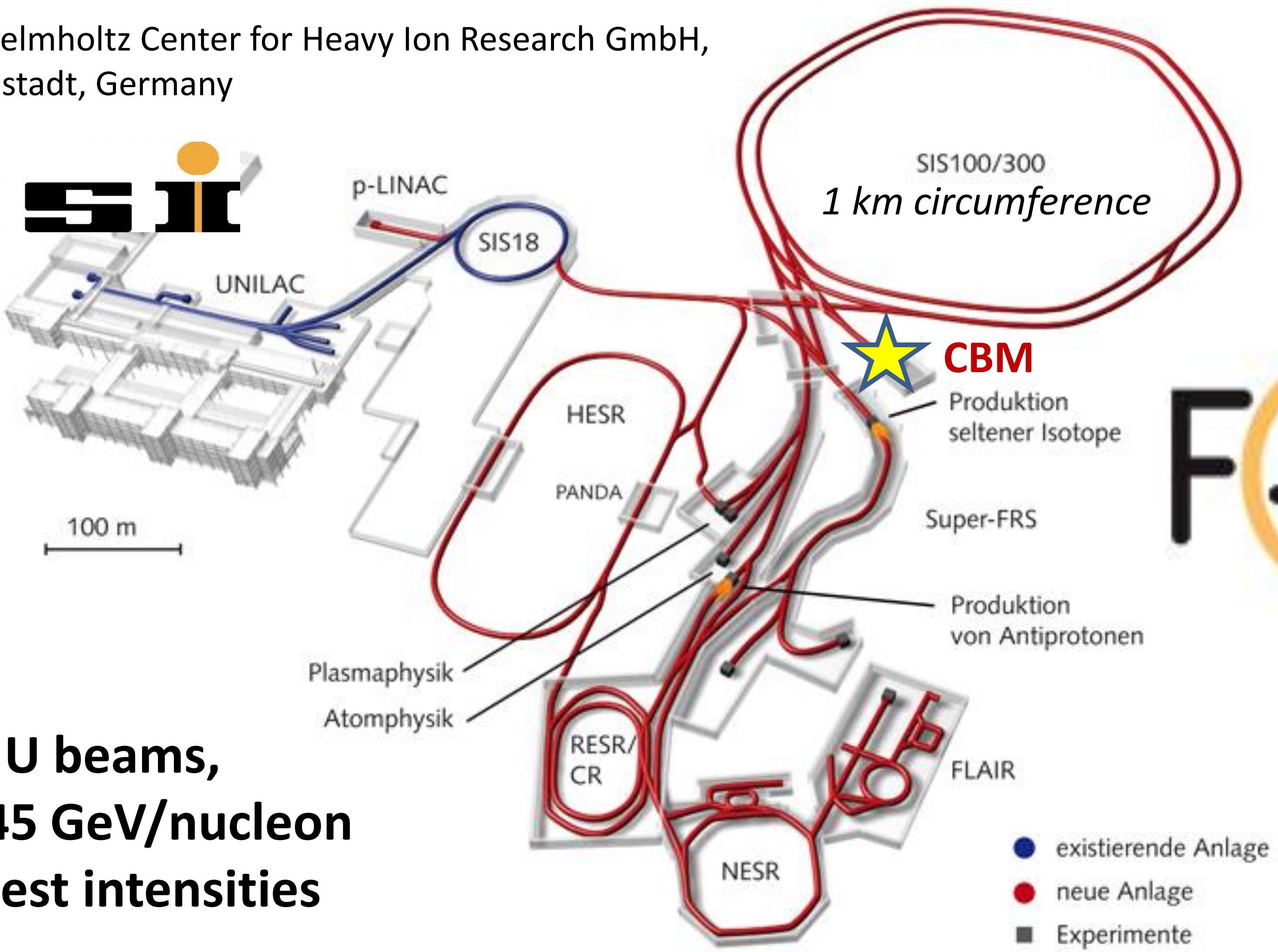
Christian J. Schmidt

3rd Annual MT Meeting

Jan. 31st to Feb. 2nd, 2017, GSI, Darmstadt, Germany

FAIR - Facility for Anti-Proton and Ion Research, Darmstadt

GSI Helmholtz Center for Heavy Ion Research GmbH,
Darmstadt, Germany



1 km circumference

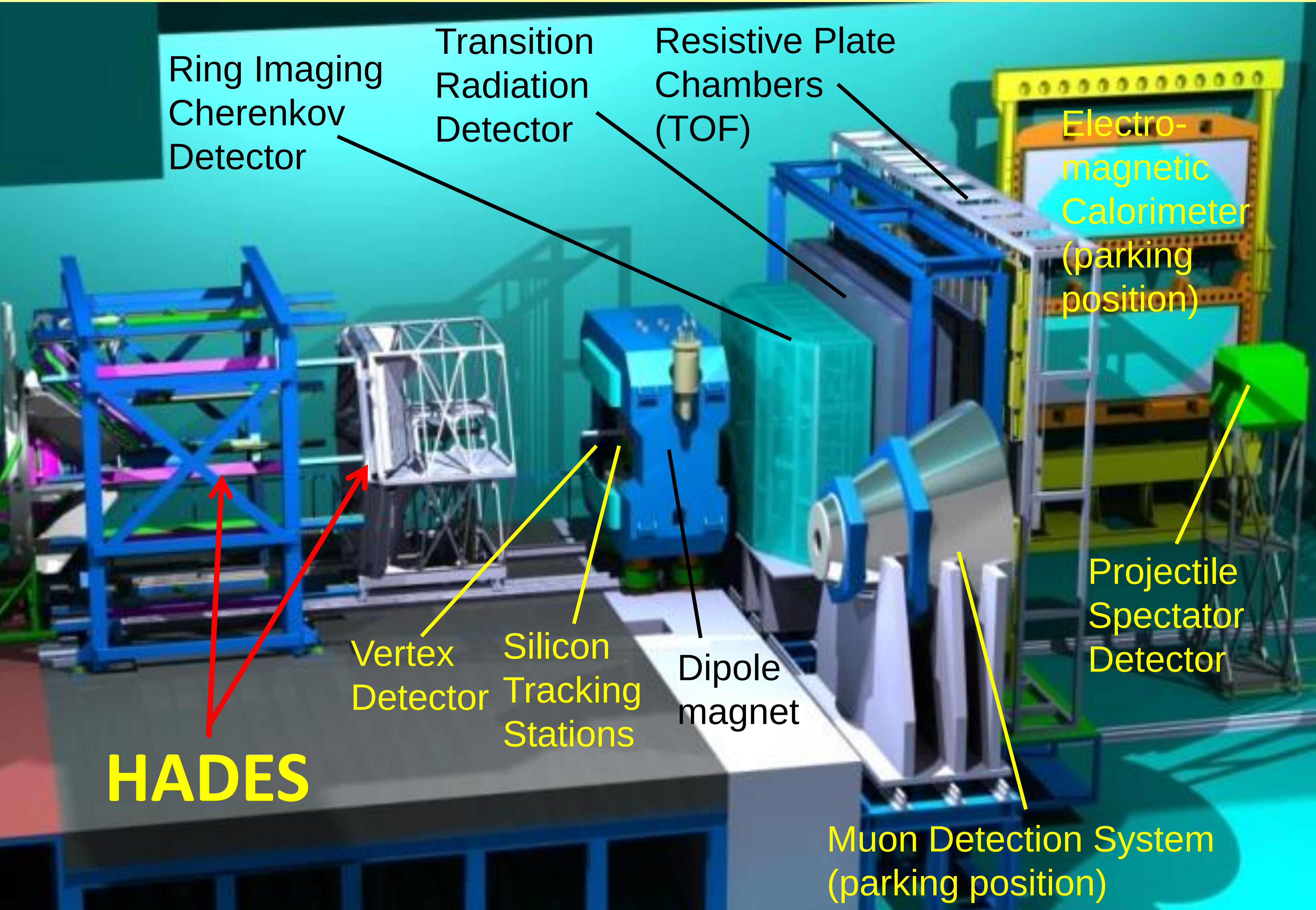
CBM

p to U beams,
2 – 45 GeV/nucleon
highest intensities

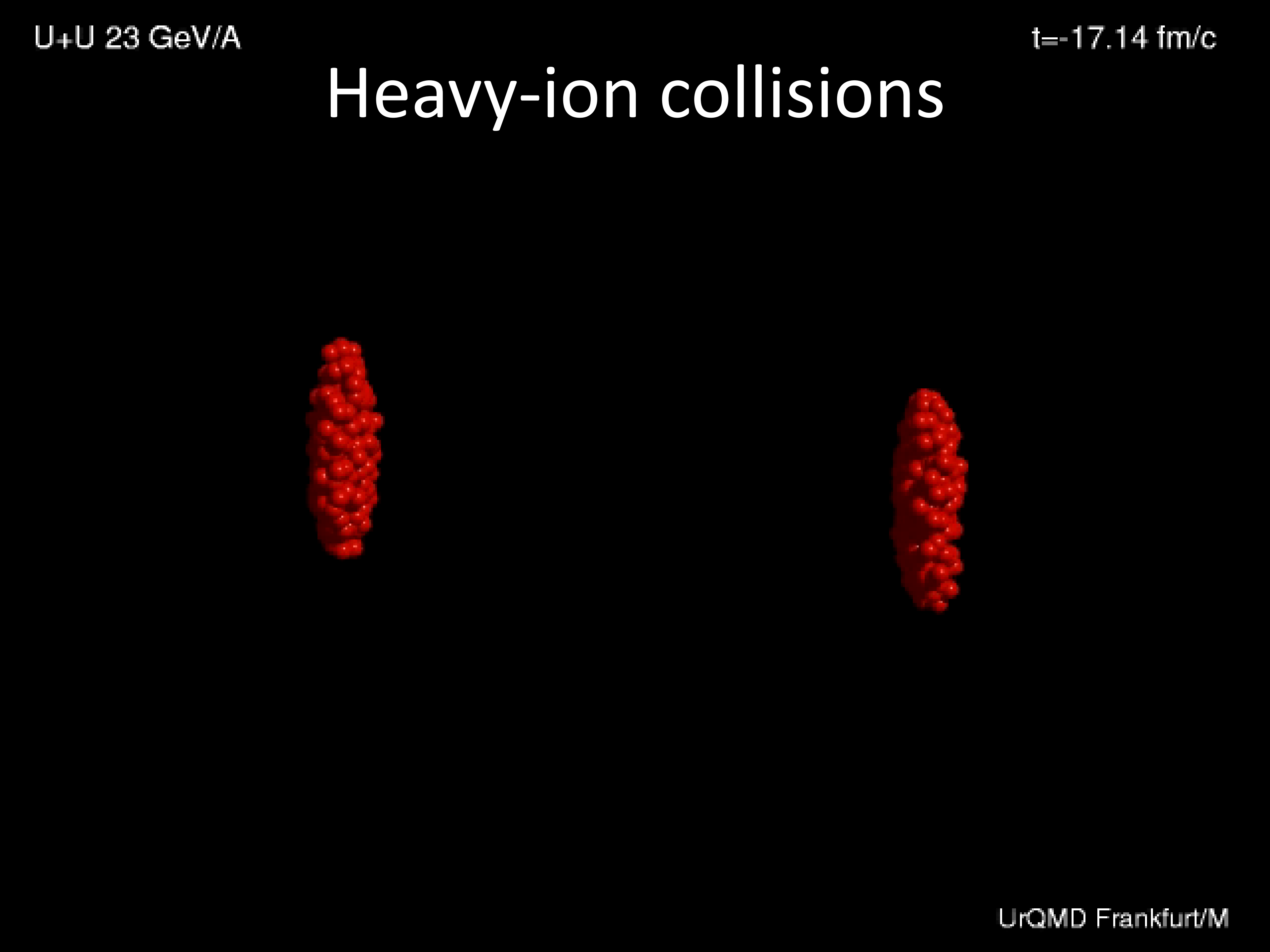
FAIR - Facility for Anti-Proton and Ion Research, Darmstadt

to of the construction site taken on July 27, 2013 (photo: Jan Schäfer for FAIR)

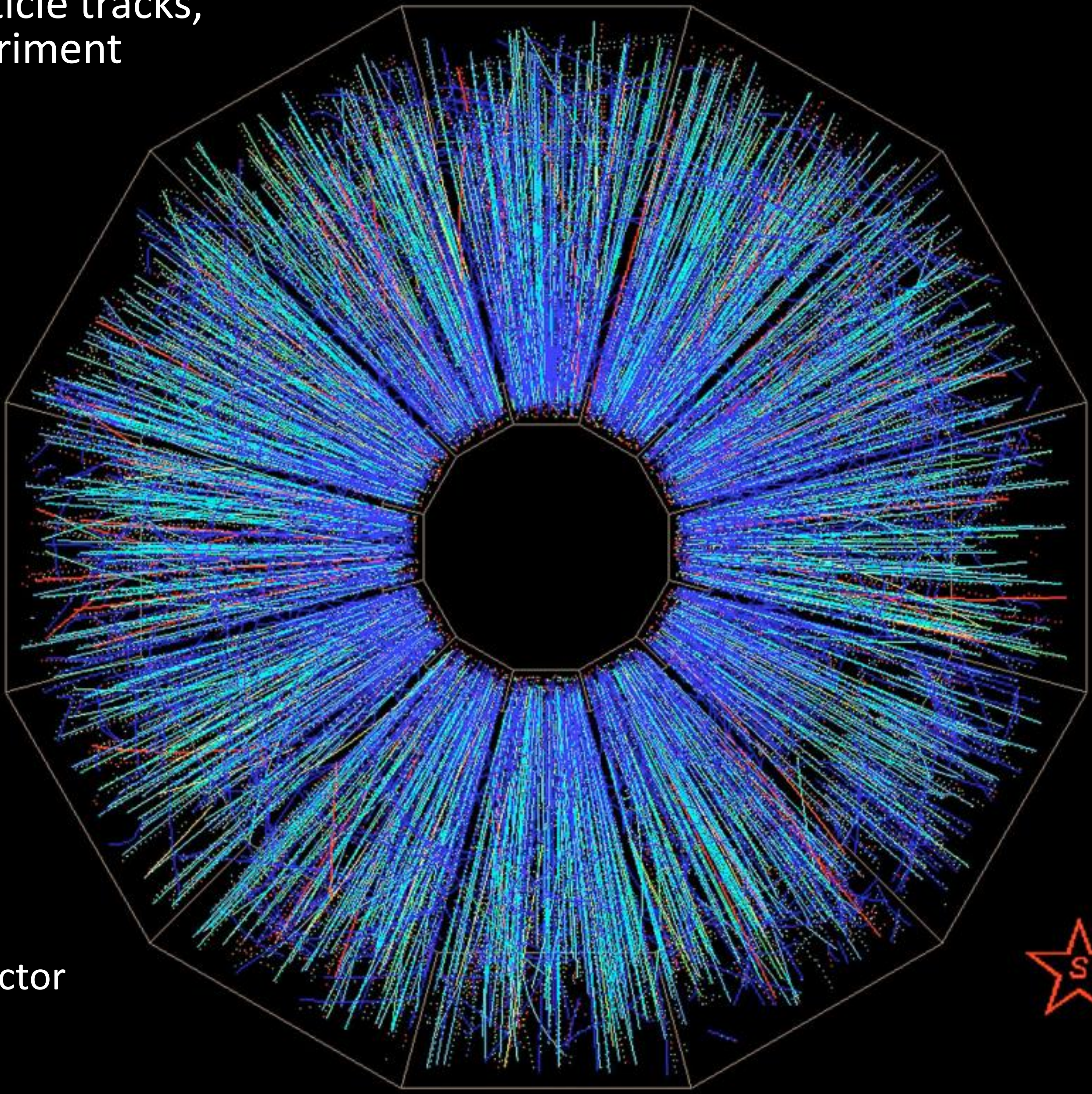
The Compressed Baryonic Matter Experiment



Heavy-ion collisions



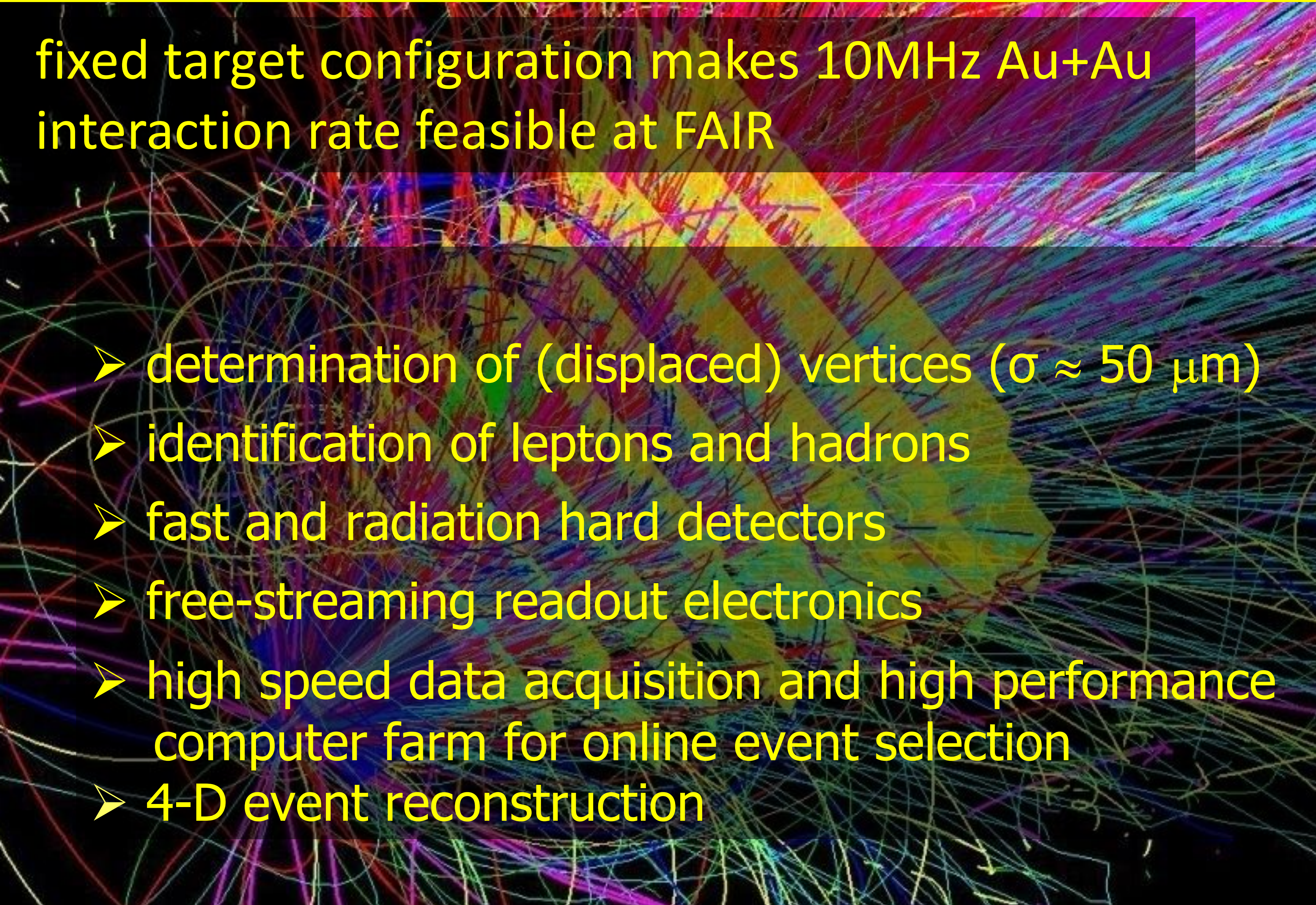
Charged-particle tracks, collider experiment



TPC detector

STAR

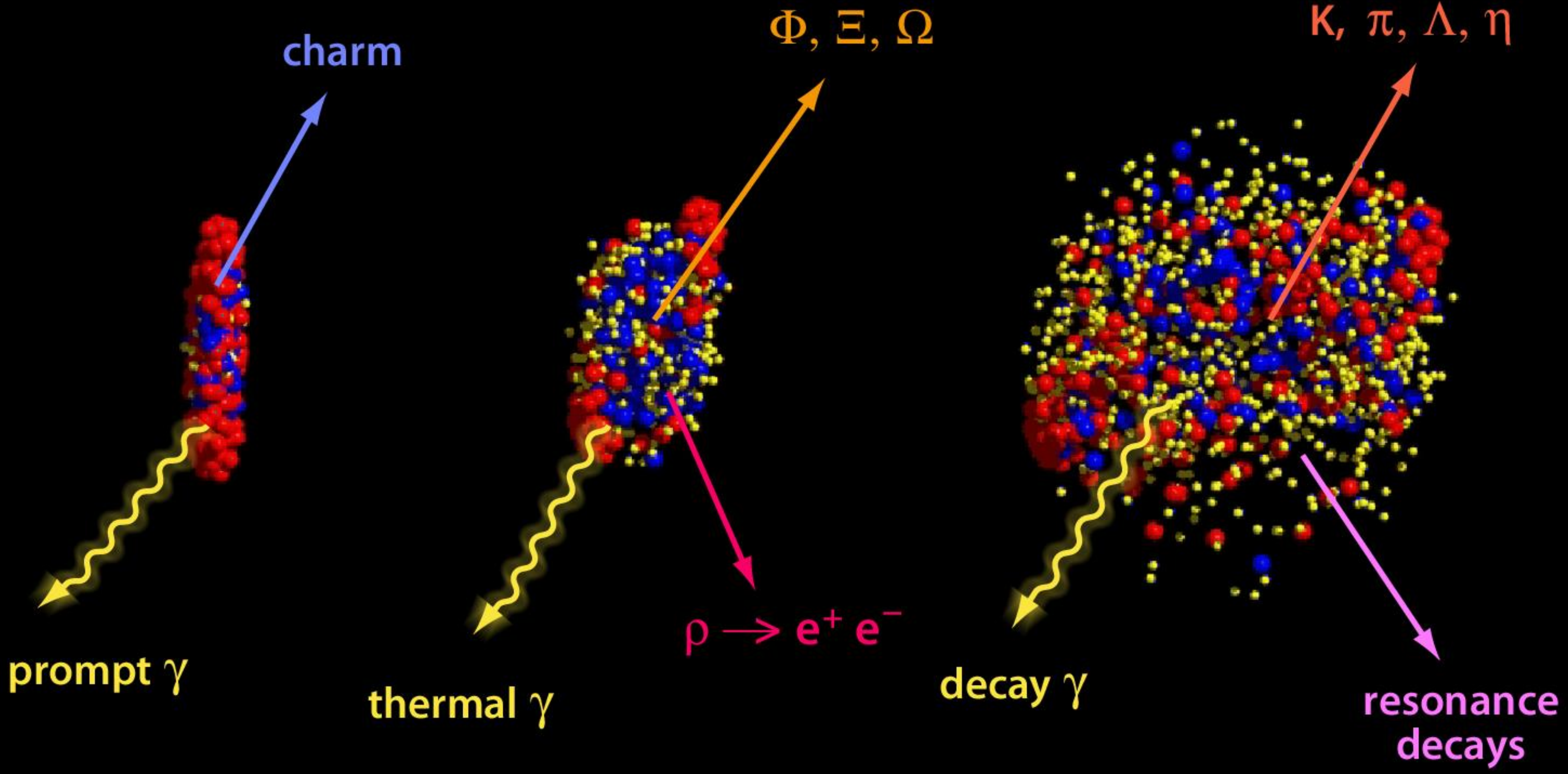
CBM technological challenges



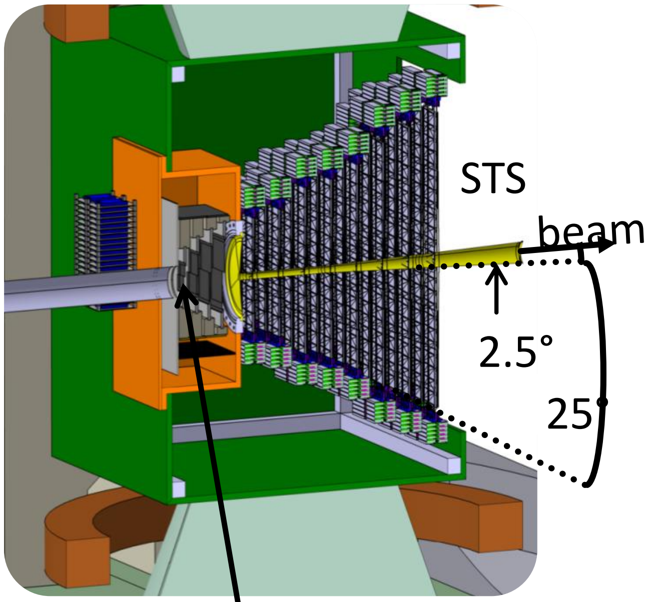
fixed target configuration makes 10MHz Au+Au interaction rate feasible at FAIR

- determination of (displaced) vertices ($\sigma \approx 50\ \mu m$)
- identification of leptons and hadrons
- fast and radiation hard detectors
- free-streaming readout electronics
- high speed data acquisition and high performance computer farm for online event selection
- 4-D event reconstruction

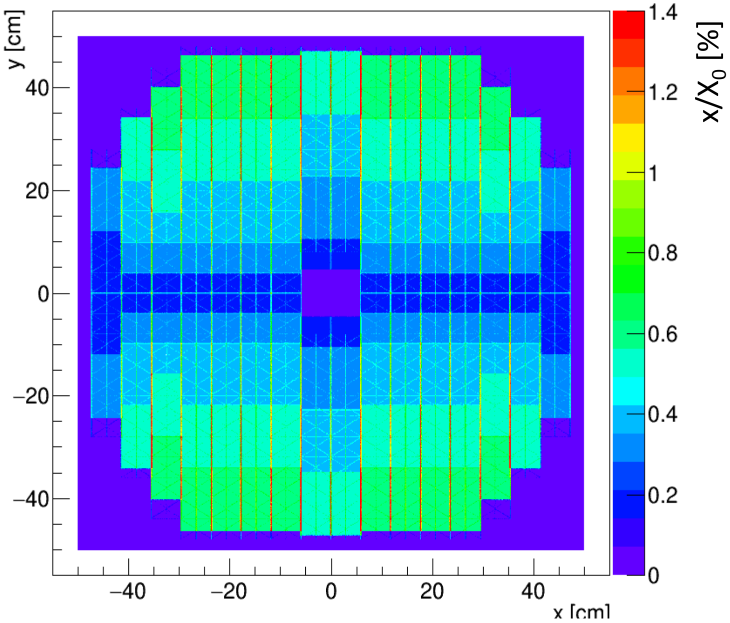
Diagnostic probes



CBM-STS

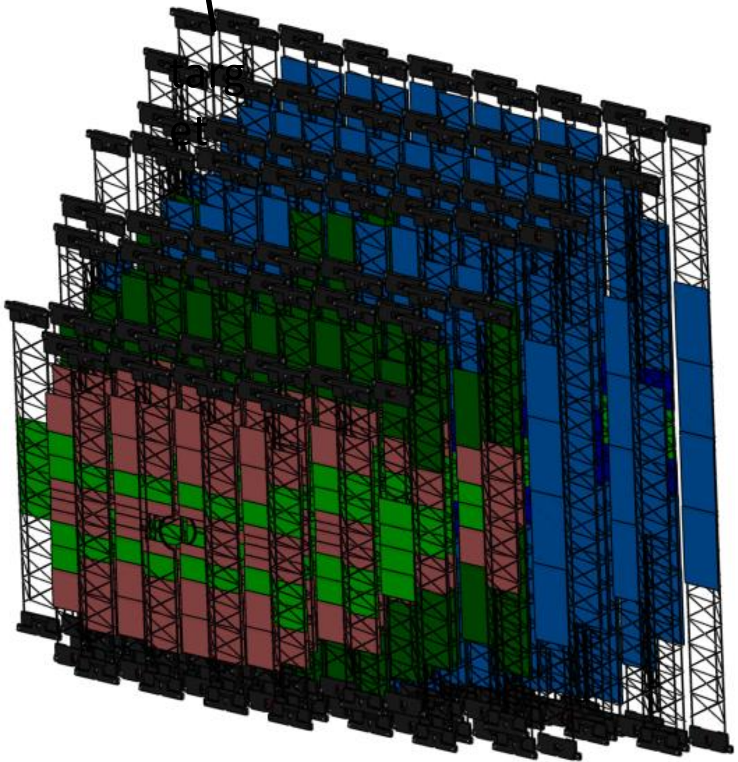


- ➢ Low-mass micro cables from sensor to FEE
- ➢ 1.8 Mio channels, cooling power ~ 40 kW
- ➢ selftriggering ASIC readout



material budget per station

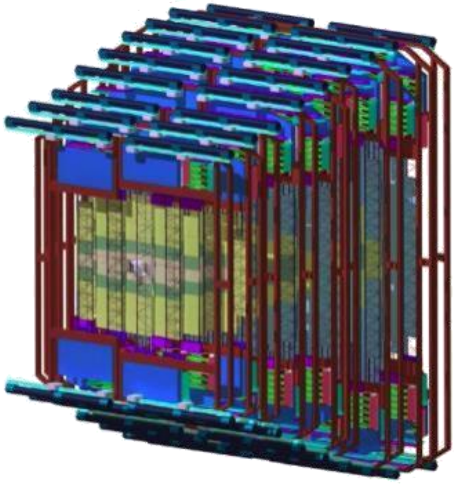
- ~ 3 sqm active sensor area
- double sided strips 7.5°, 58µm pitch
- 8 Stations,
- 106 ultra-light carbon ladders
- 896 Sensor modules



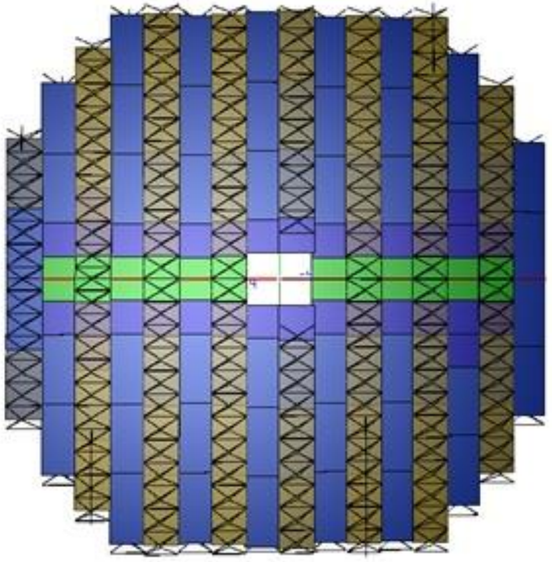
The CBM-

Silicon Tracking System STS

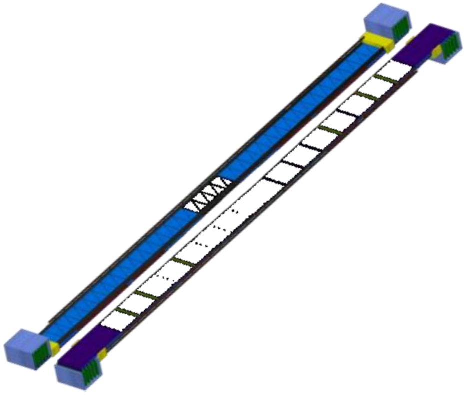
STS with 8 tracking stations



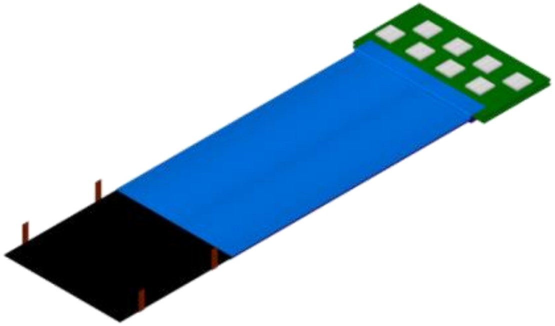
8 tracking stations



106 detector ladders



896 detector modules



Core CBM detector system:

- **to provide track reconstruction**
- **momentum determination of secondary particles.**

Assembly of double sided strip detector modules, a collaborative effort

- prototyping ongoing

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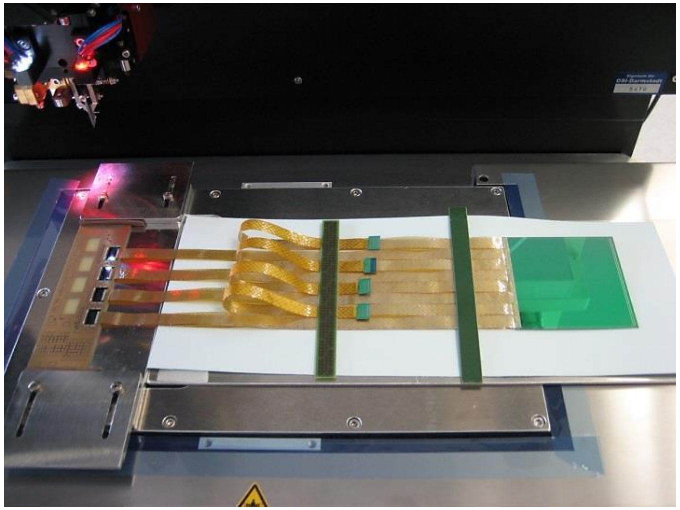
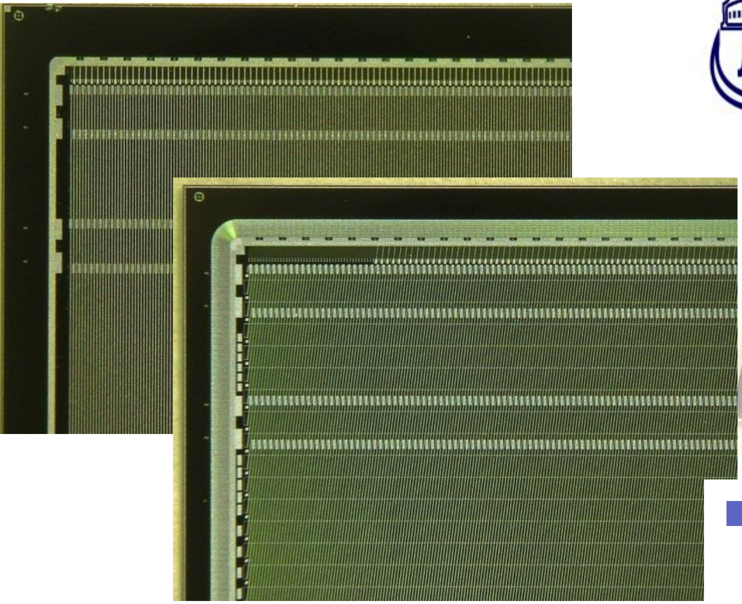
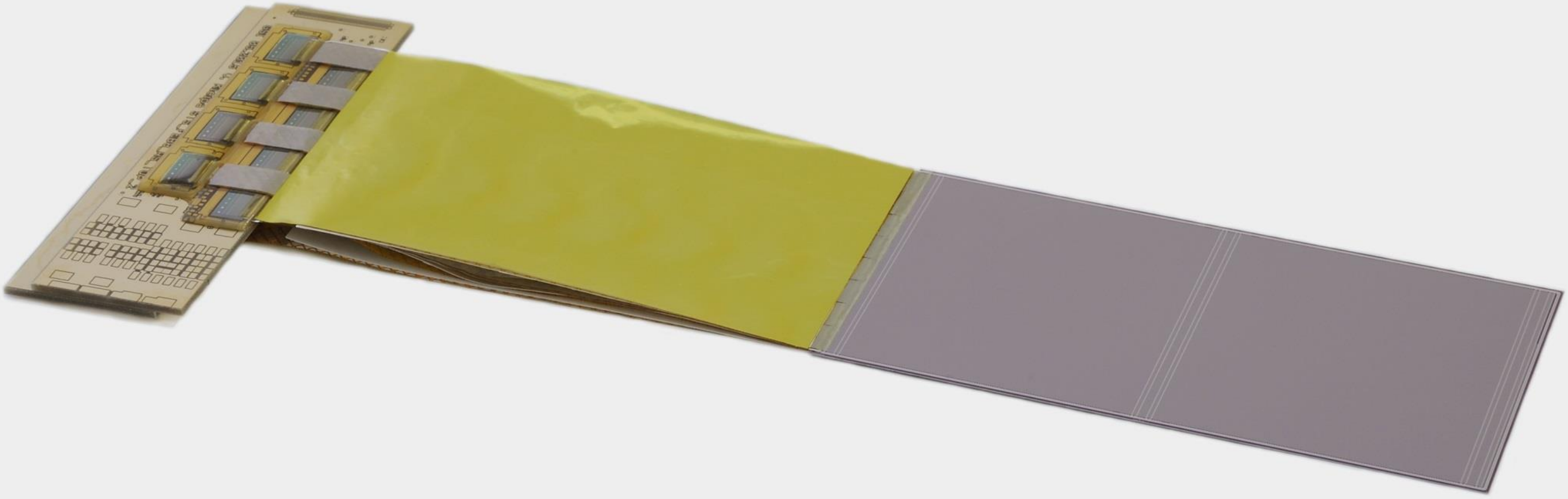




- Topical workshop on radiation induced surface effects in silicon detectors, Oct. 2016 at KIT

the Silicon-Sensor-Module



STS-module-components:

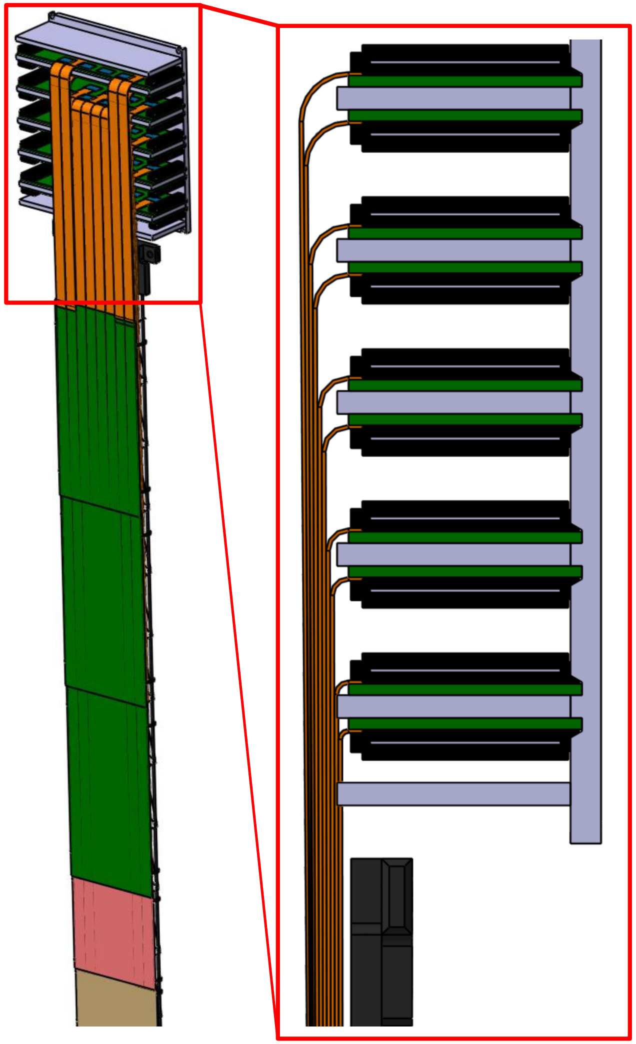
front-end-boards

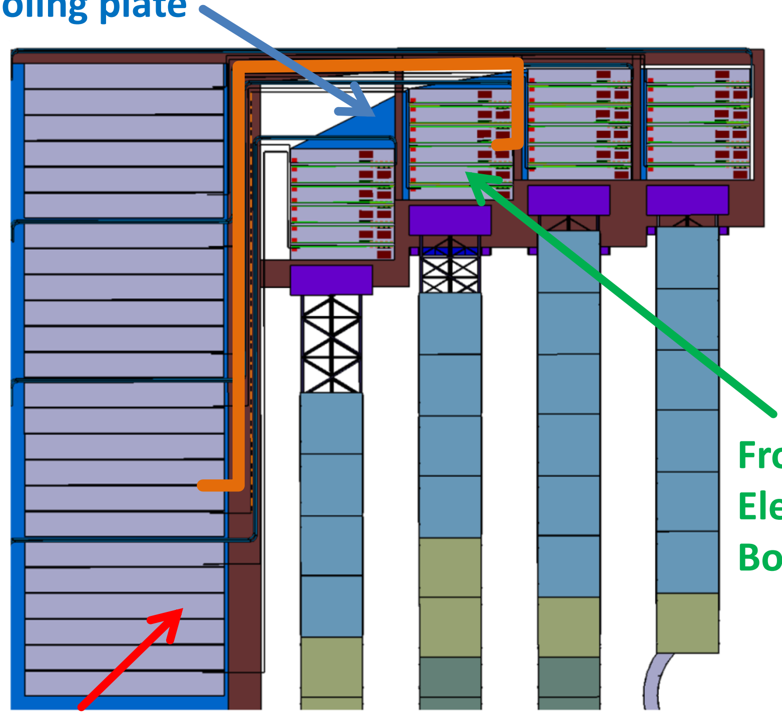
signal transmission cable

double-sided silicon microstrip sensor

C.J. Schmidt, GSI Detector Laboratory

Module Electronics Allocated on Cooling Shelves





Cooling plate

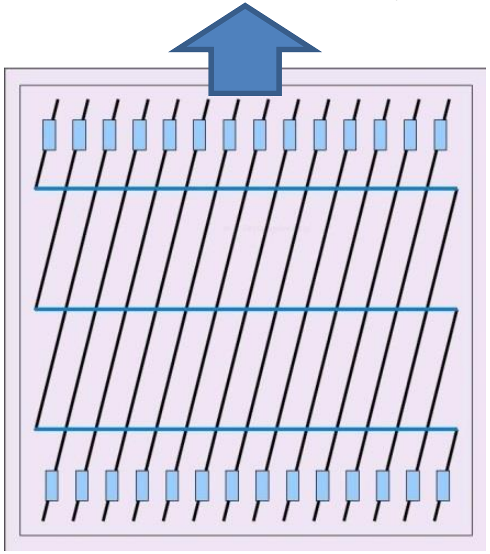
Front-end Electronics Boards

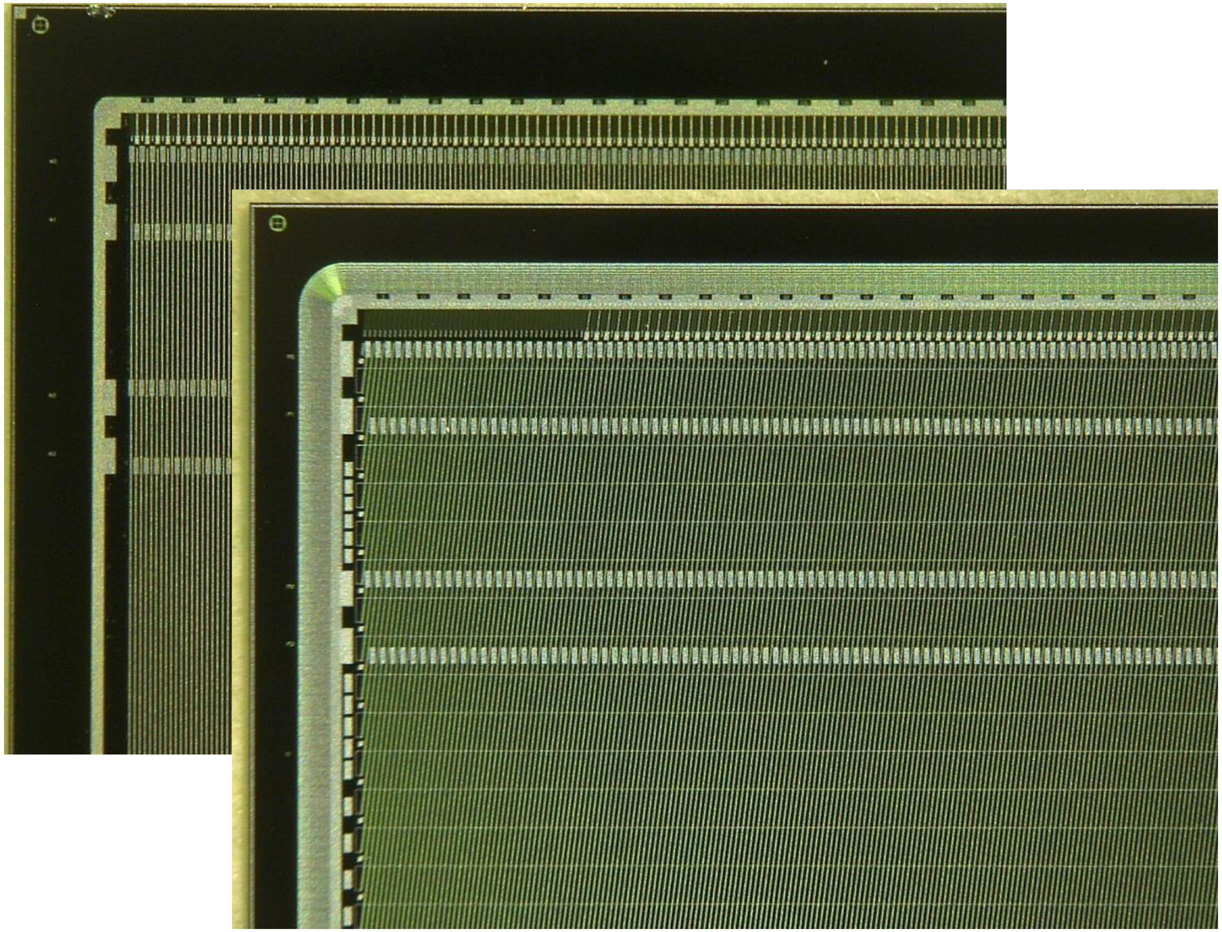
Read-out Boards, Power Boards

bi-phase CO_2 cooling system
STS electronics total: 42 kW

Silicon microstrip sensors

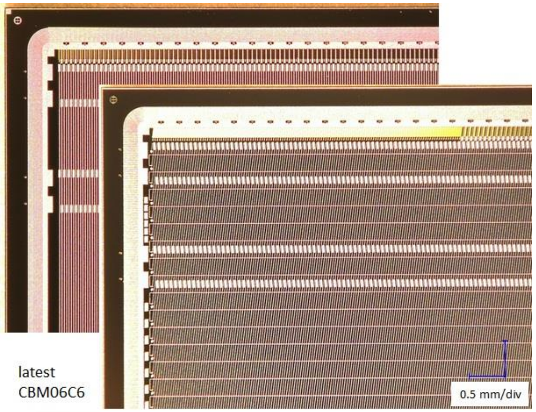
- 300 µm thick, n-type silicon
- double-sided segmentation
- 2nd metal routing lines
- 1024 strips of 58 µm pitch
- strip length 2/4/6/12 cm
- angle front/back: 7.5/0 deg
- read-out from top edge
- rad. tol. up to 10^{14} n_{eq}/cm^2





Module-Components:

silicon-microstrip-sensors



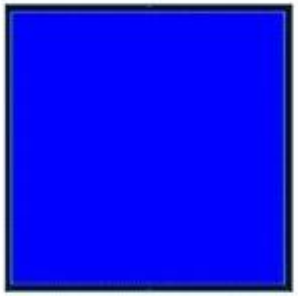
number of stripes: 1024
pitch of the stripes: 58 µm
pitch of the bond pads: 116 µm in two staggered rows

fill gaps at beam hole

few sizes, small numbers

62 mm x 22 mm

62 mm x 42 mm

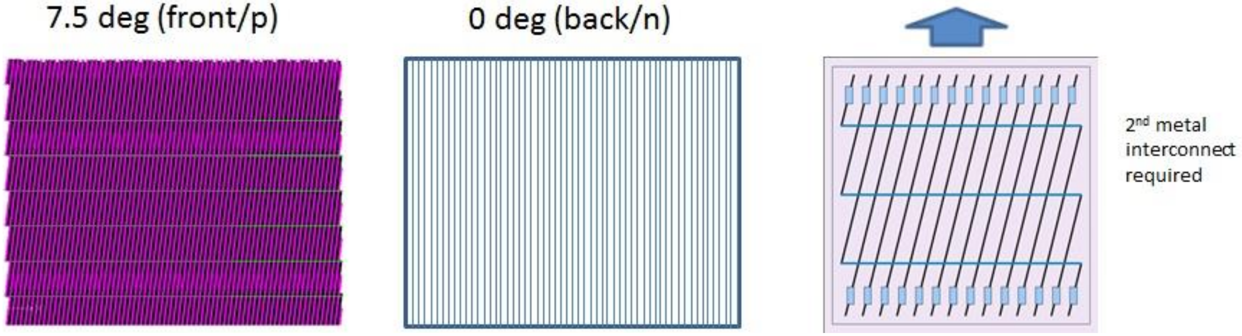


62 mm x 62 mm

62 mm x 124 mm

strip orientation at 58 µm pitch

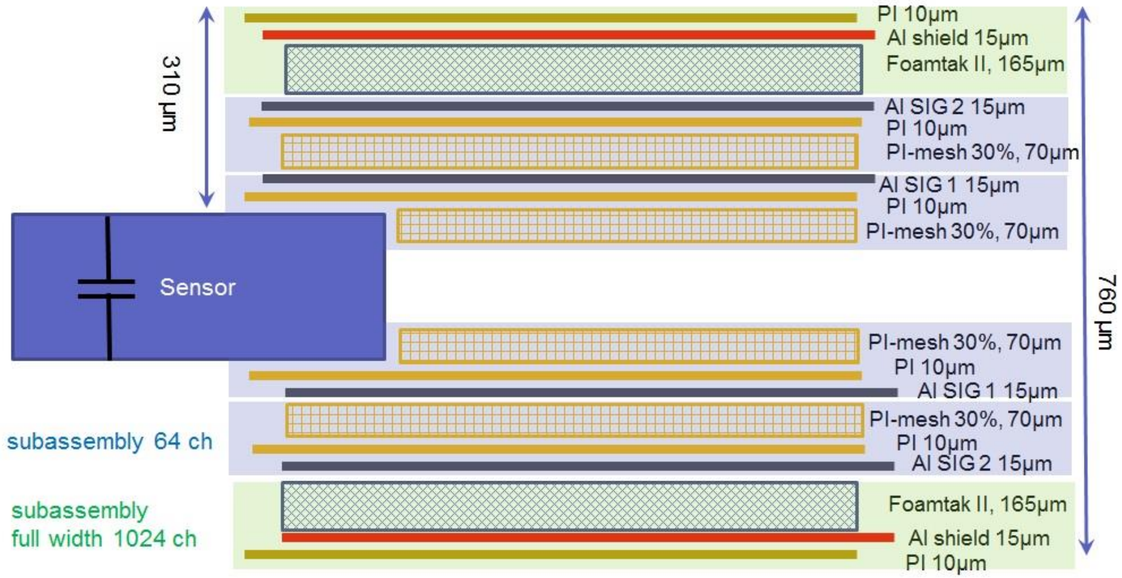
connectivity, r/o direction



module-components:

signal transmission cable, version 1

microcable stack-up of version 1:



ε_r Foamtak II = 1,5 ε_r PI-meshed 30% = 1,75 → strip capacitance < 0,5 pF/cm

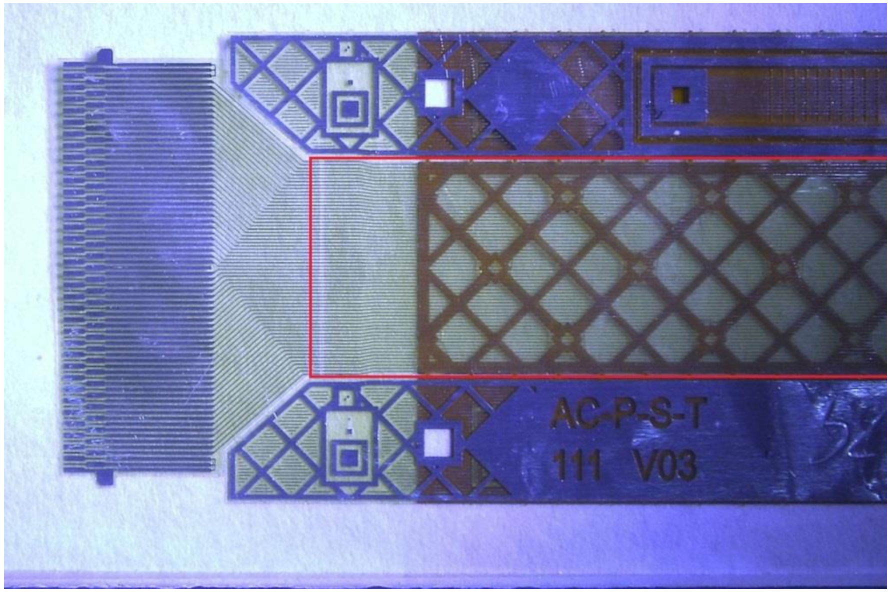
Additional spacers (PI-mesh) are placed between two signal layers to reduce the capacitance contributions from the adjacent connecting layers.
Shielding layers reduce the noise level and prevent shorting between the stacks of cables.

module-components:

signal transmission cable, version 1

version 1: Aluminum on Polyimide-cable from LTU/ Kharkiv, Ukraine

signal layer: *64 Al lines of 116 µm pitch, 10 µm thick on 14 µm polyimide, lengths up to 55 cm*

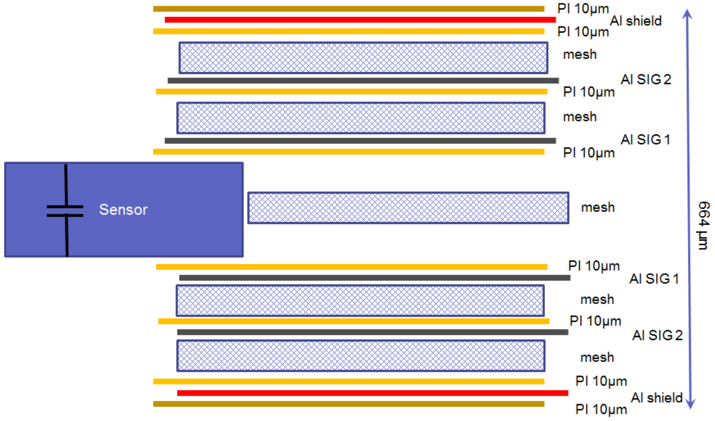


A set of 32 microcables with different cable types is needed for one module!

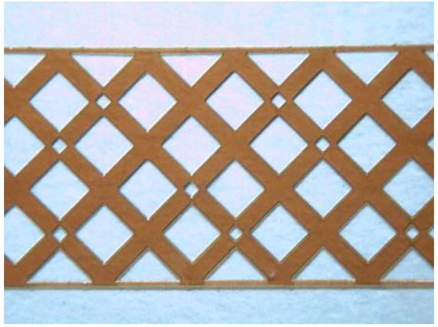
Read-out cables

32000 analogue cables of 64ch needed

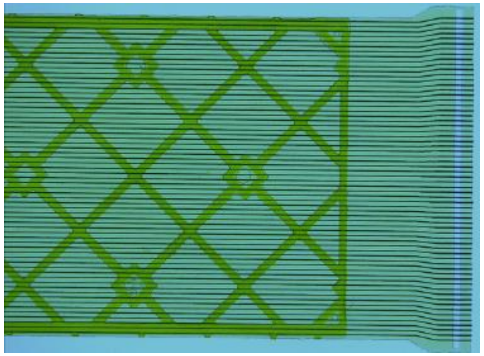
cable stack: *thickness 0.230 % X_0*



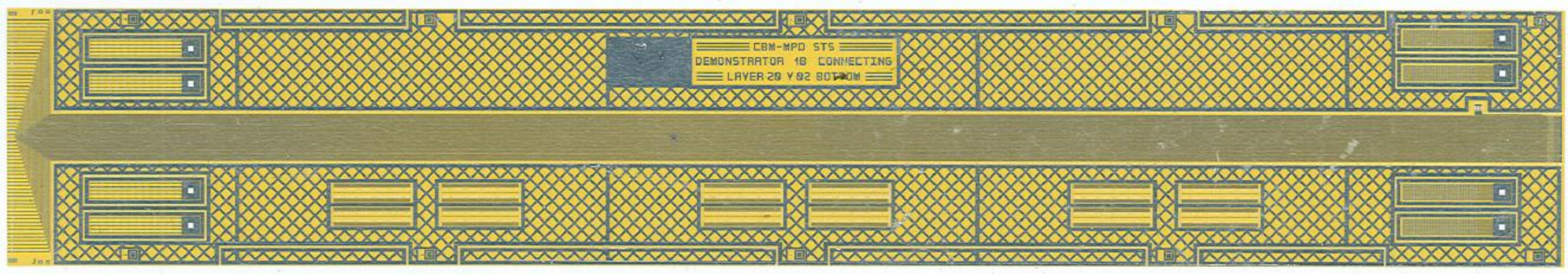
spacer layer



64 traces per cable

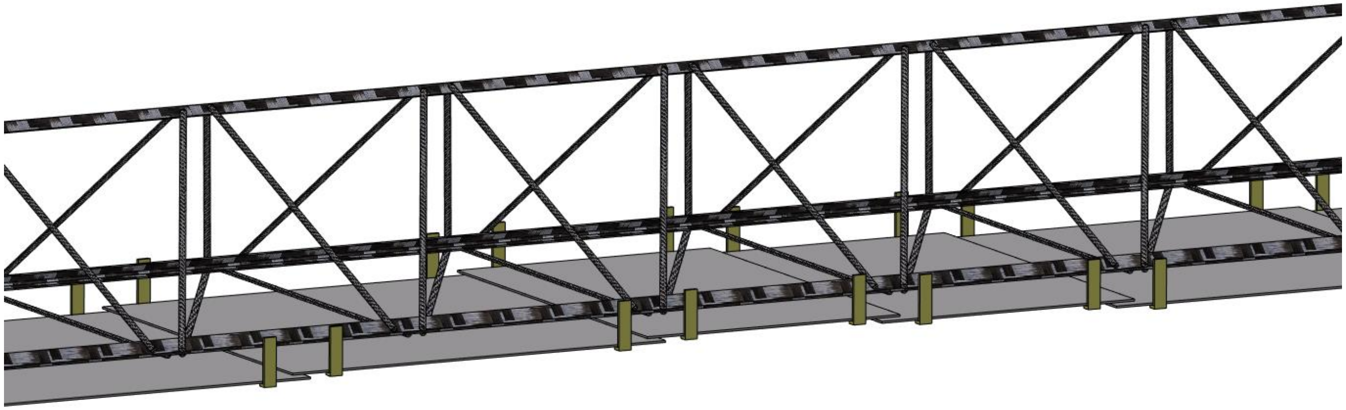


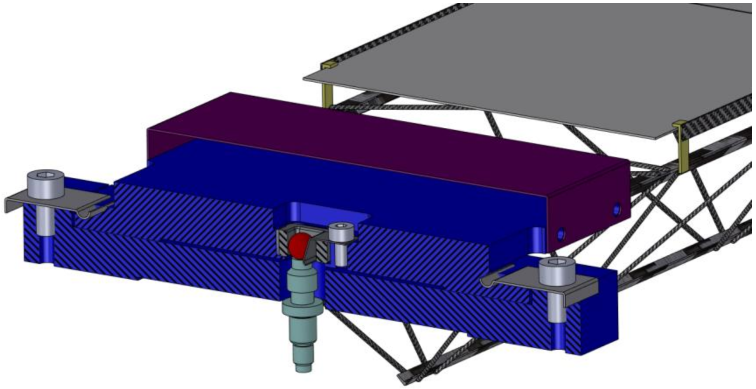
signal layer: *64 Al lines of 116 µm pitch, 10 µm thick on 14 µm polyimide, lengths up to 55 cm*

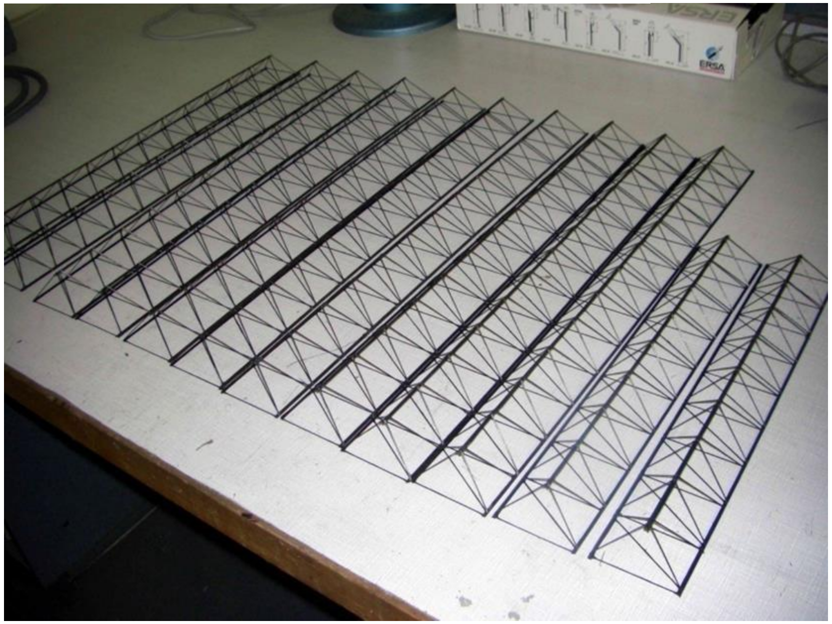


challenge: production yield of upto 50cm long cables → low yield = uncalculable project duration

Carbon fiber ladders

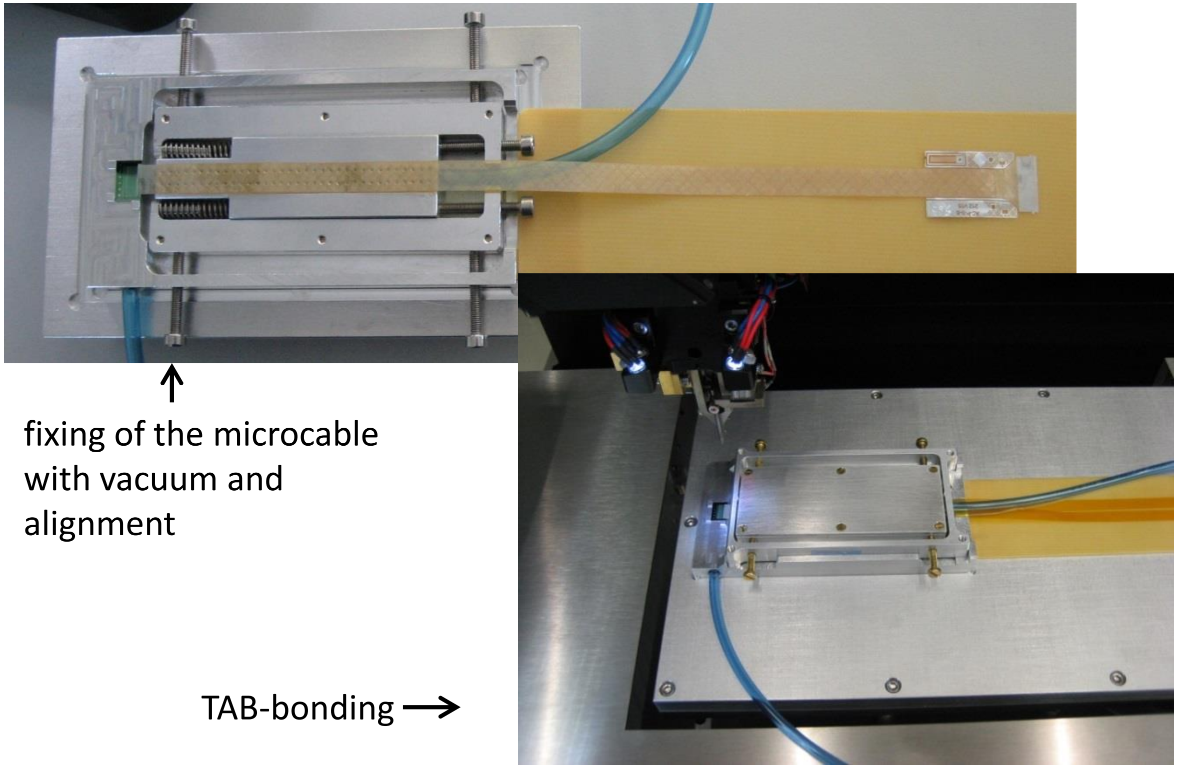






11g for 1m long ladder

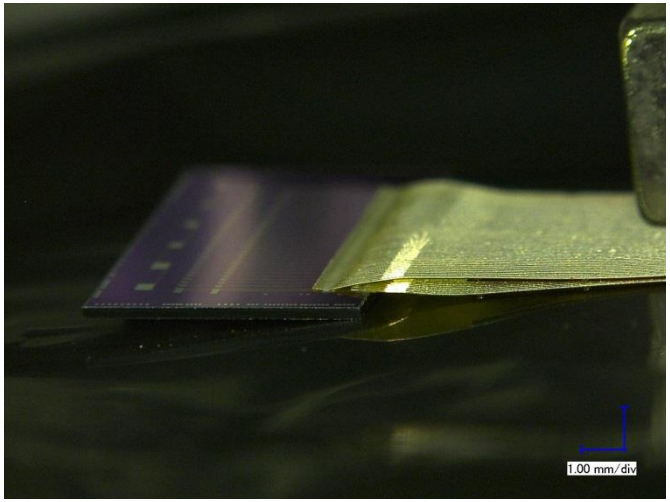
<u>assembly-step 1:</u> Chip cables: TAB-bonding of microcables to the readout chip



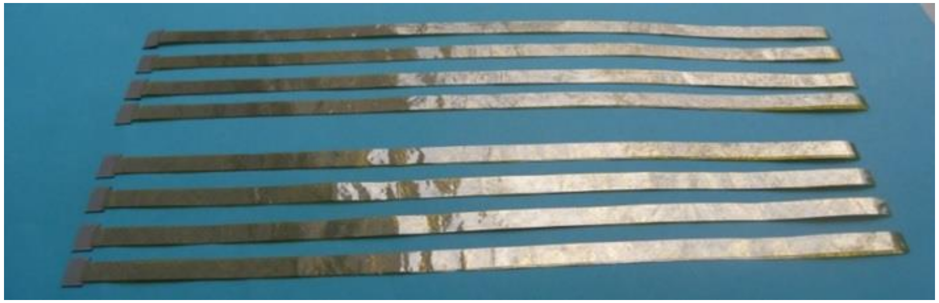
↑ fixing of the microcable with vacuum and alignment

TAB-bonding →

two layers of microcables, TAB-bonded to a dummy-ASIC and protected with Globtop after QA-measurements ↓

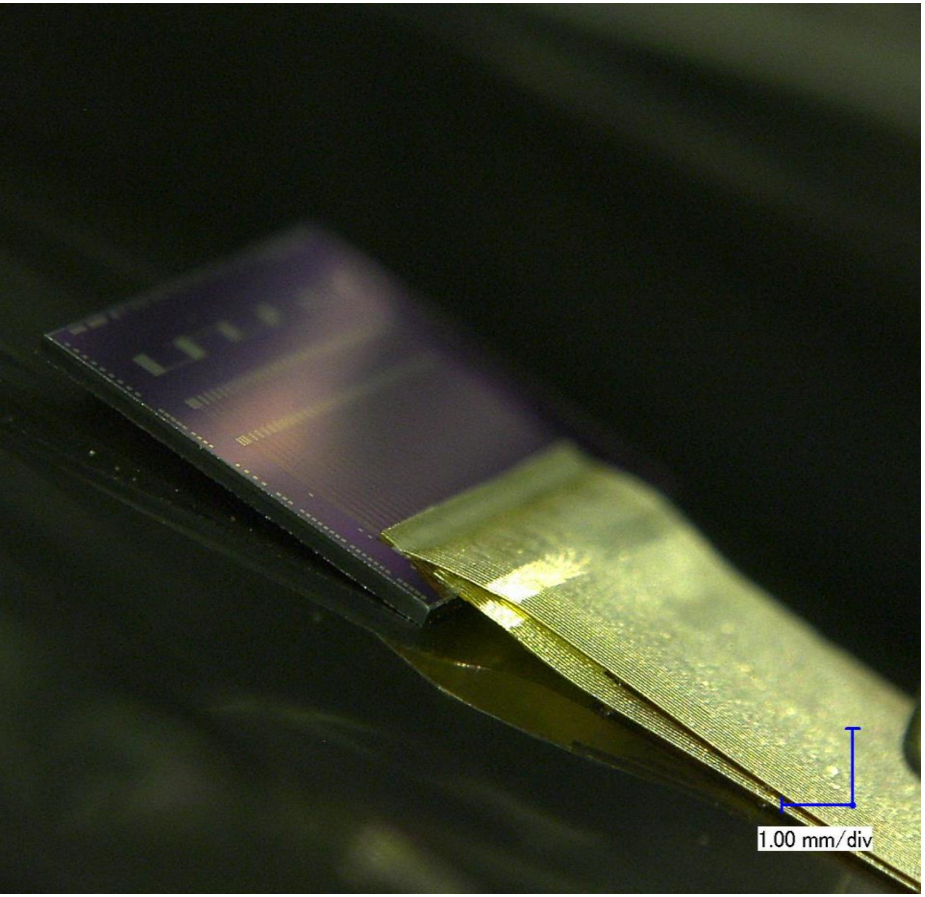


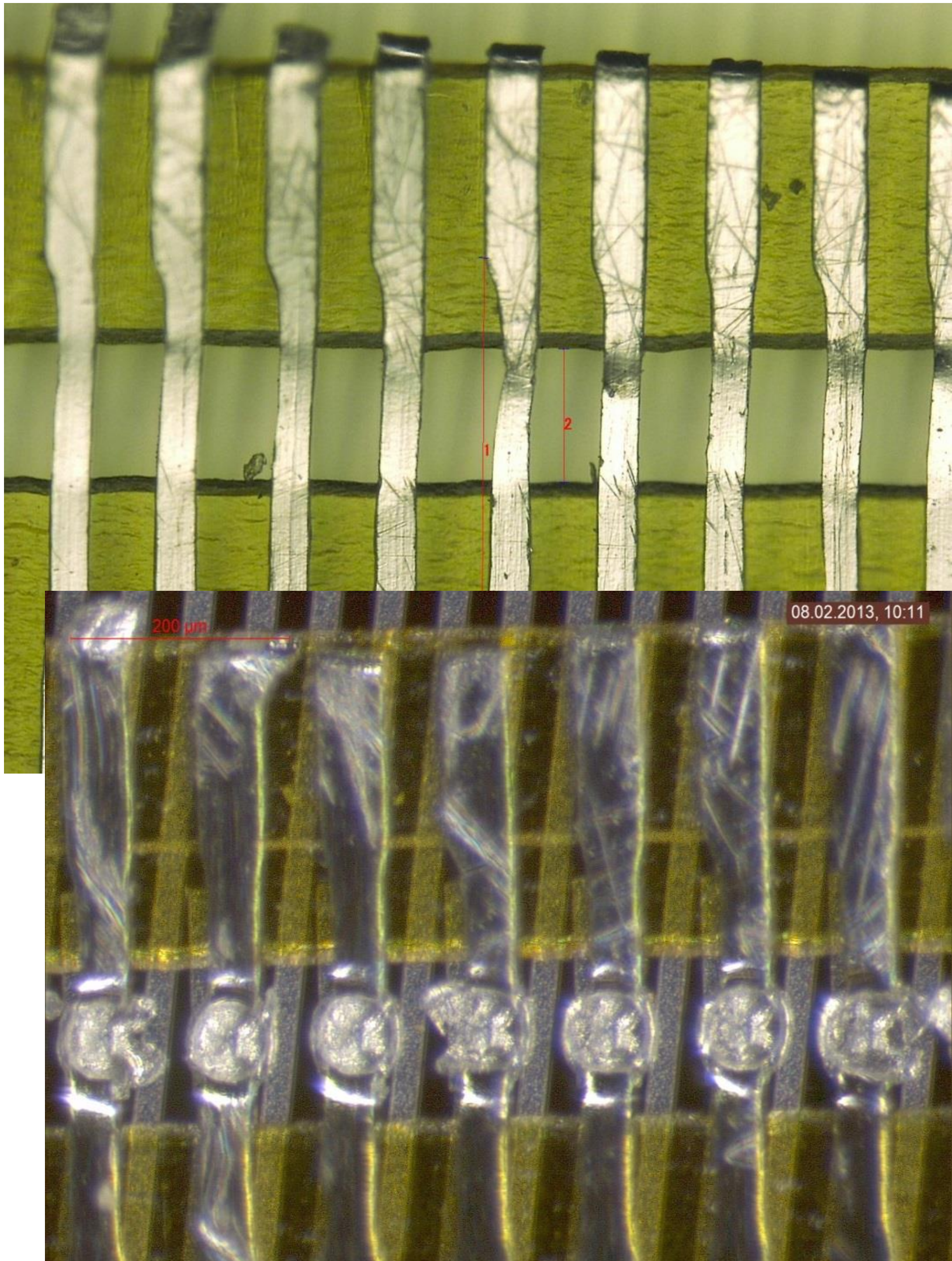
bottom and top layer of the microcables,
TAB-bonded to the 8 STS-ASICs for one sensor side →



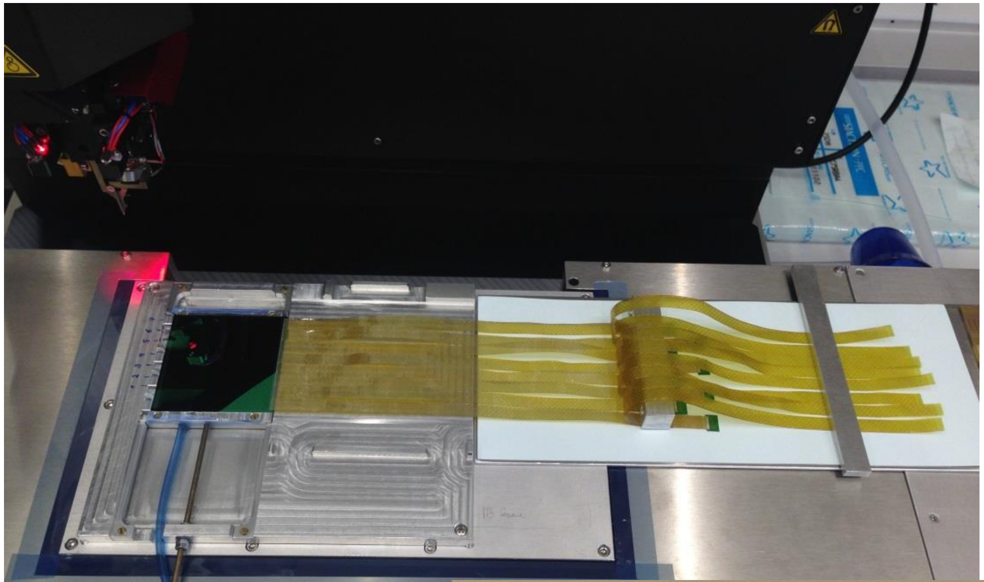
Micro Cable Technology with TAP-Bonding

- double cable layer bonded onto chip



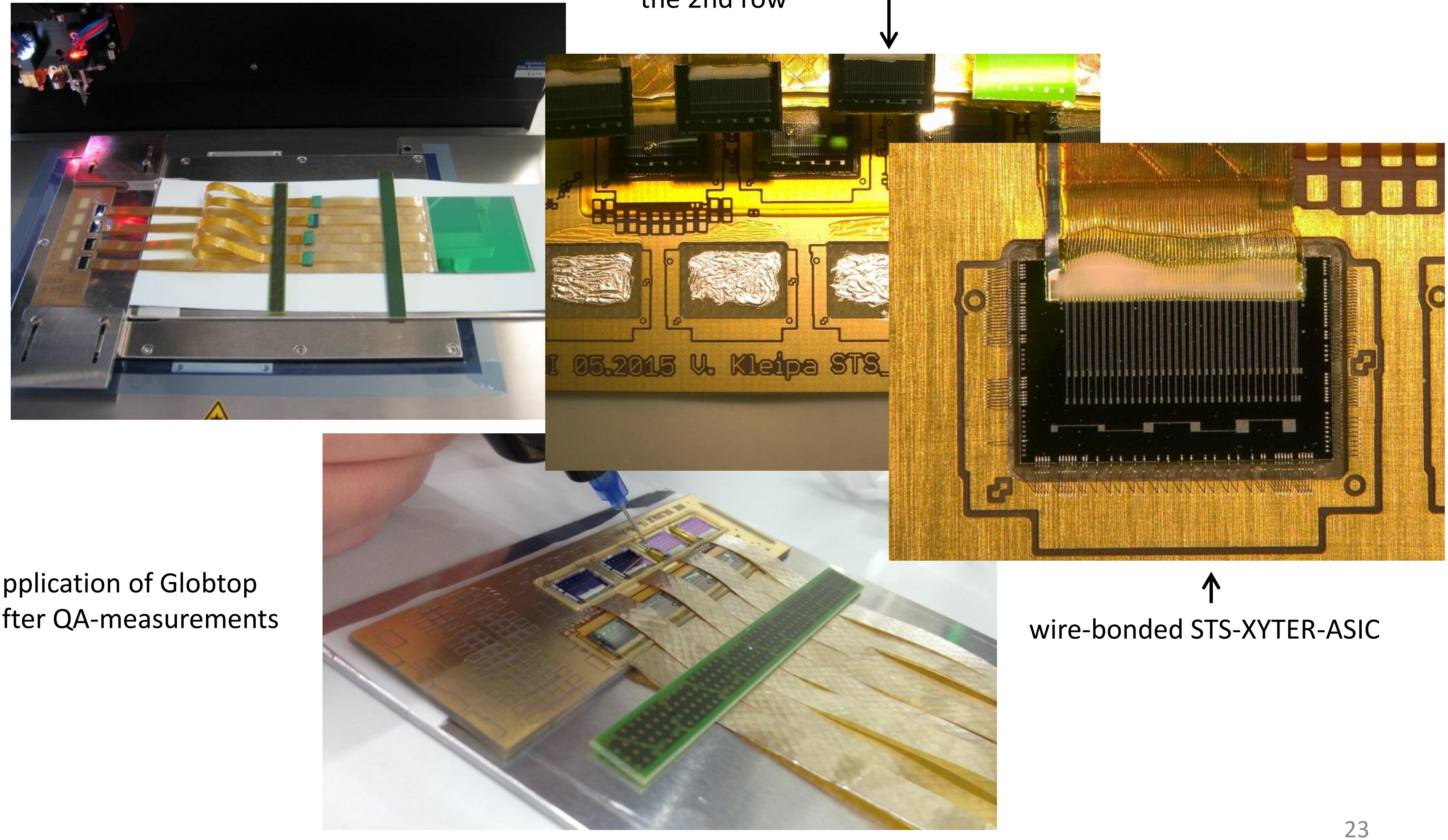


<u>assembly-step 2:</u> TAB-bonding of chip cables to the silicon sensor



- fixing of the microcables with vacuum and alignment
- TAB-bonding of 16 microcables to the sensor (two rows at 8 microcables)
- protection of the TAB-bonds with Globtop after QA-measurements

assembly-step 3: die- and wirebonding of readout chips to the PCB-rows



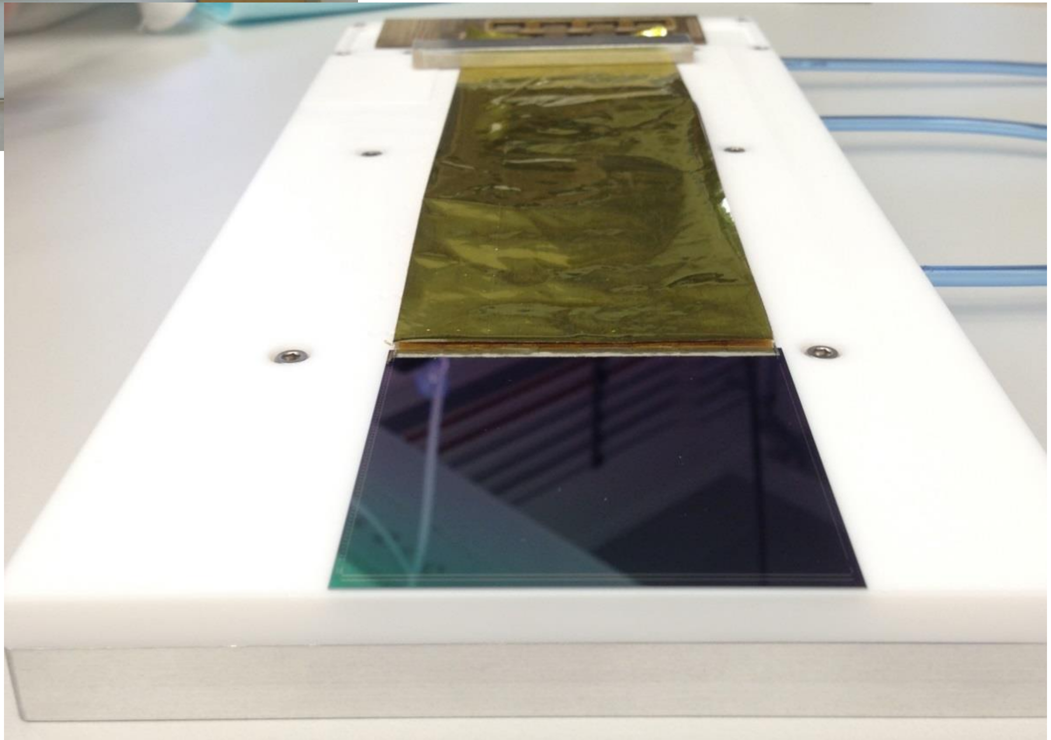
wire-bonding of the STS-YTER-ASIC´s ↓

die-bonding of four ASIC´s for the 2nd row ↓

↑ wire-bonded STS-XYTER-ASIC

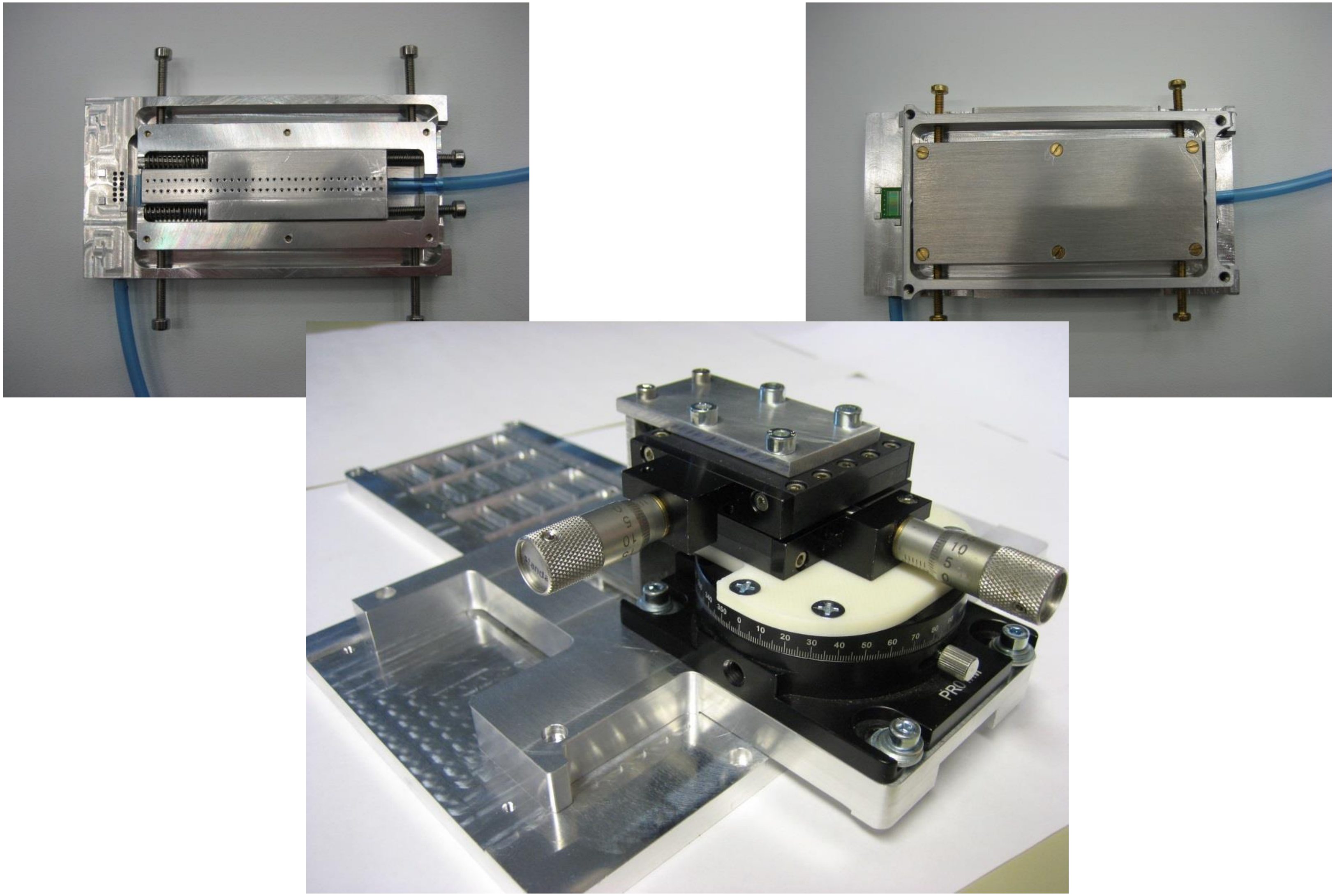
application of Globtop after QA-measurements

assembly-step 4: glueing of shielding- layers and spacers



This semi-module then turned over to the n-side of the sensor and steps 1 to 4 are repeated!

optimization of alignment jigs

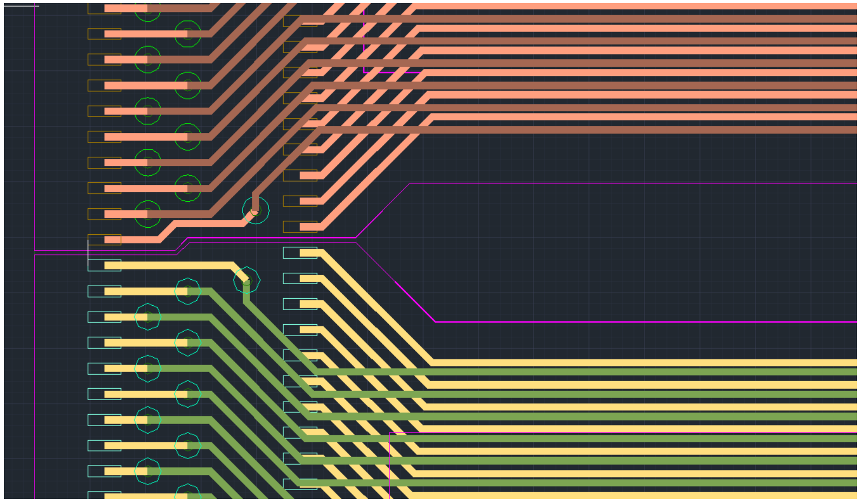


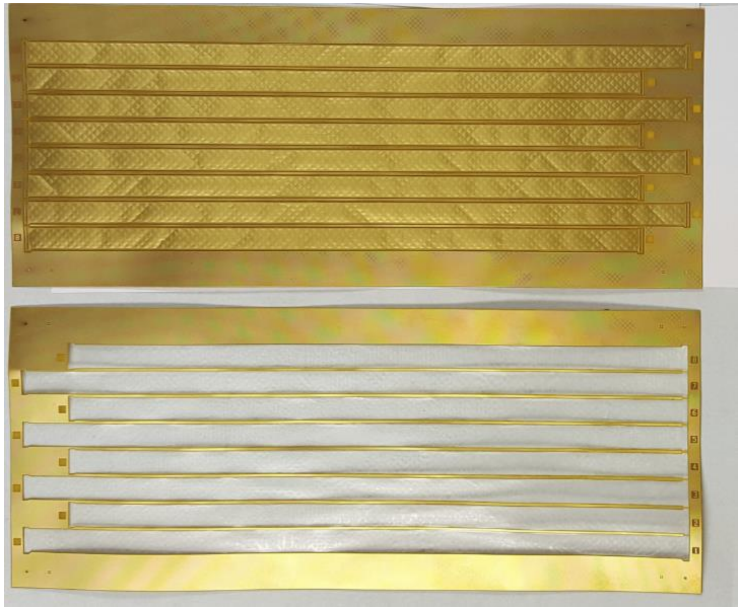
Module-Components:

signal transmission cable, version 2

version 2: Copper-based microcables/
KIT-IPE (Dr. Thomas Blank & team)

As an alternative to the Aluminum-microcables a R&D-project has been started that investigates Copper-based cables.





Benefits of Copper:

- well known in PCB-Flexboard technology
- offers interconnected multilayer solutions
  - ⟹ one cable with two layers (bottom & top) and vias instead of two single Al-cables

Module-Components:

signal transmission cable, alternative version 2

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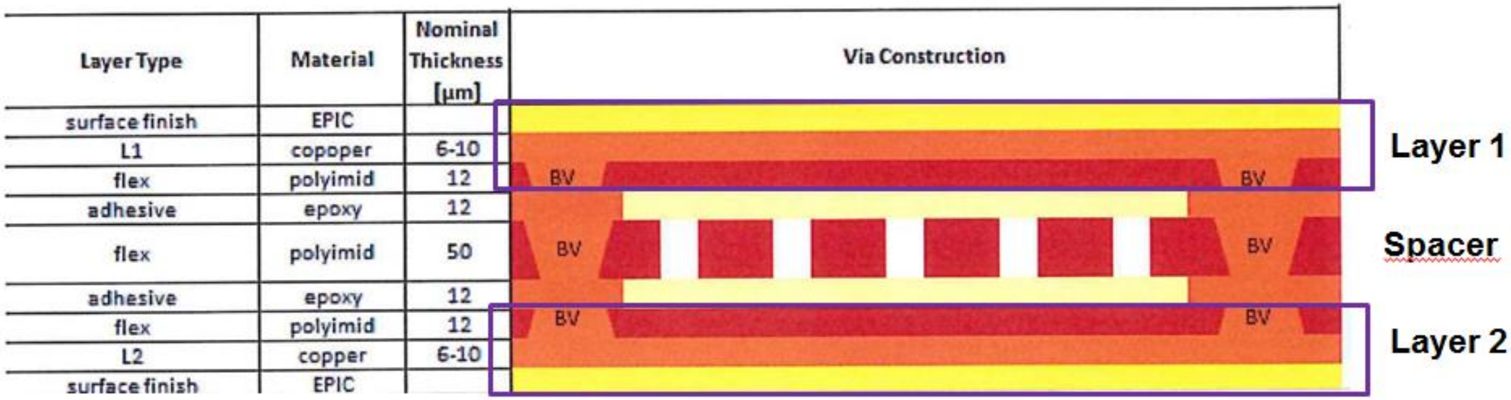
build-up of micro-copper-cable of version 2:



Layer Type	Material	Nominal Thickness [µm]
surface finish	EPIC	
L1	copoper	6-10
flex	polyimid	12
adhesive	epoxy	12
flex	polyimid	50
adhesive	epoxy	12
flex	polyimid	12
L2	copper	6-10
surface finish	EPIC	

surface finish:
EPIG (Electroless Palladium, Immersion Gold**),**
thin (300 nm) noble surface for soldering and bonding in contrast to standard ENIG (5..7µm) (-> Pitch), Palladium serves as a highly efficient diffusion barrier

Resulting capacitances

- 0,82 pF/cm with 50 µm meshed spacer
- 0,67 pF/cm with 150 µm meshed spacer

the module-components:

signal transmission cable, version 2

interconnection technology for version 2: Au-stud bumps + flip-chip

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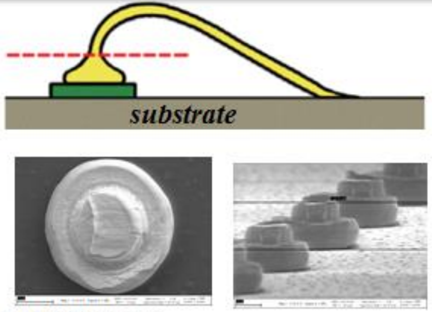
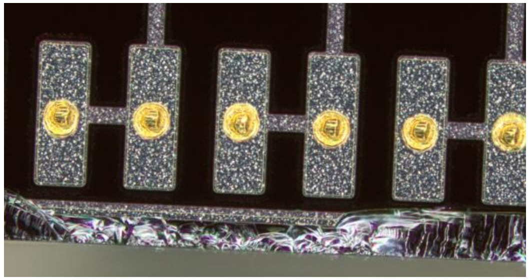
Ball - wedge gold wire bonding



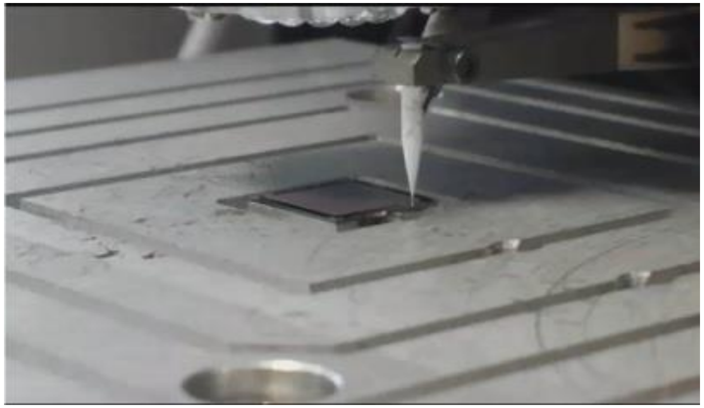
Gold-Stud bumps

Source: J. Jordan – Gold-Stud bumps in flip-chip applications

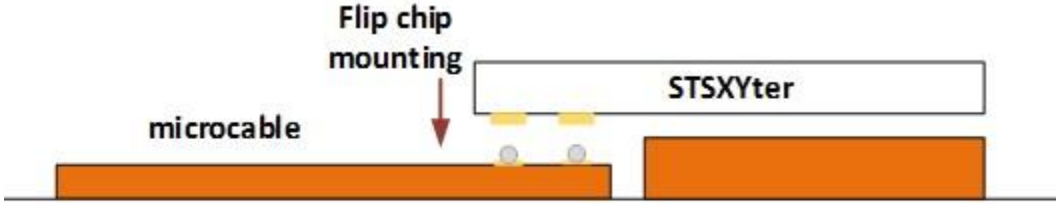


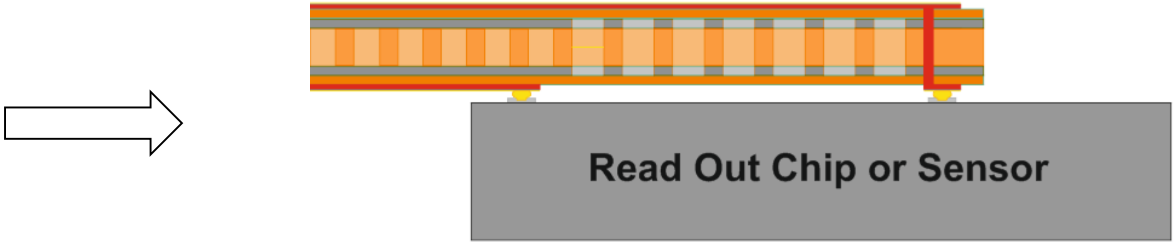
Au-Stud bumps on STSXter-Testchip

- *reliable and fast process*



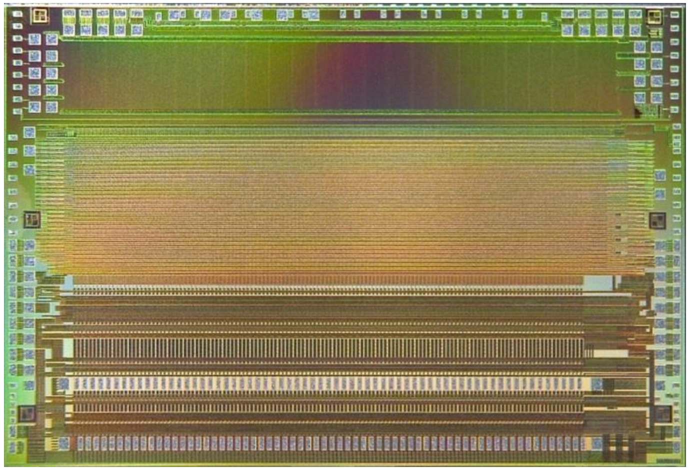
Ball-Wedge-Bonder



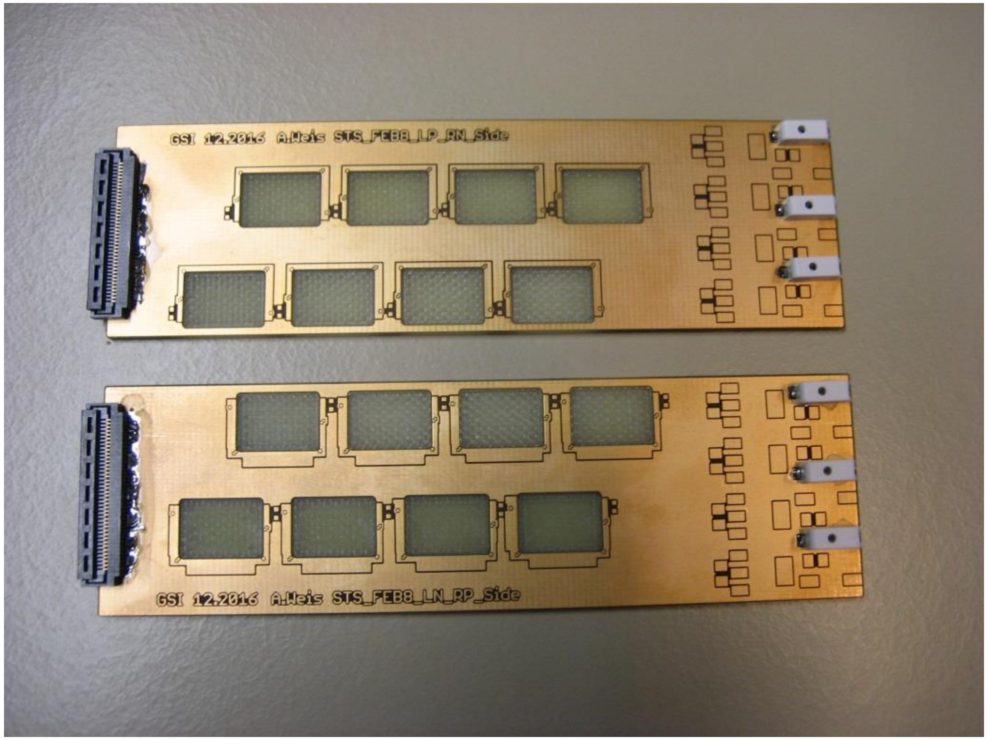


Module-Components:

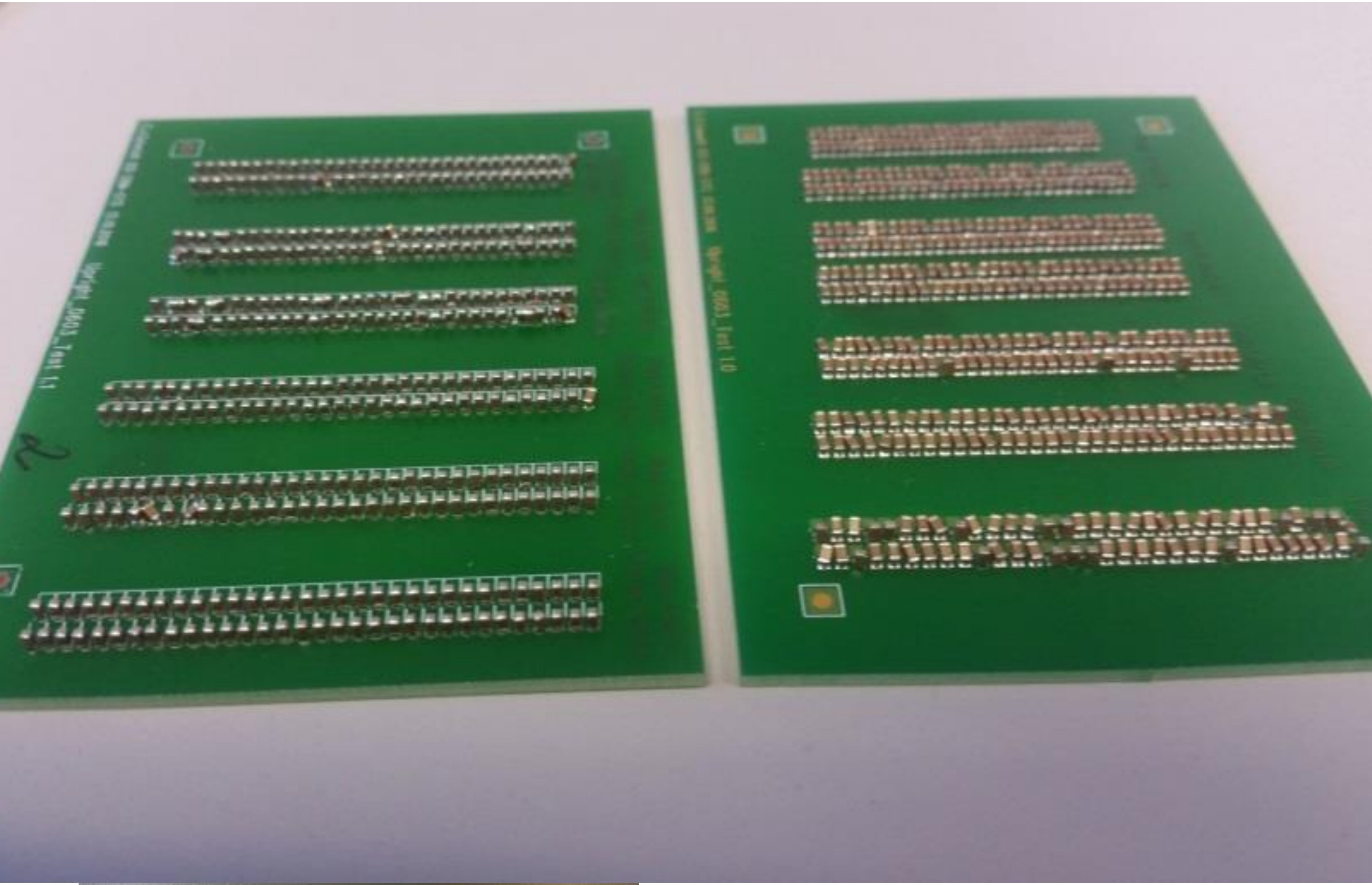
front-end-boards



STS-XYTER-ASIC
with 128 channels and pitch of 116 µm
(same as the sensor bond pad pitch)

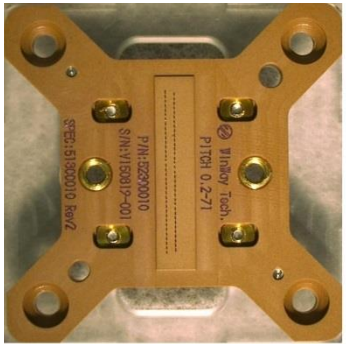


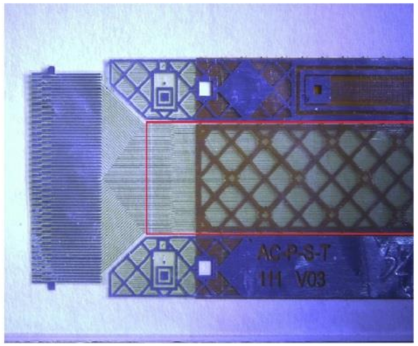
8-STS-XYTER-board
(dummy-PCB with power and signal connectors)

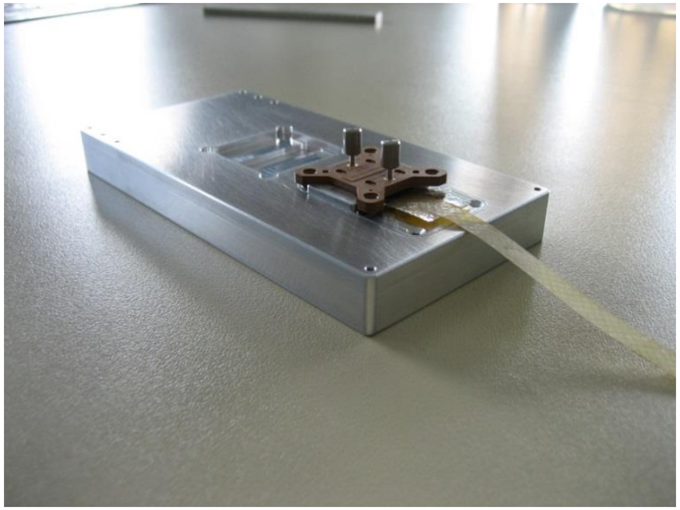

Upright_0603_Test 1.1
2
Upright_0603_Test 1.0

QA-measurements tools: Pogo-Pin Sockets

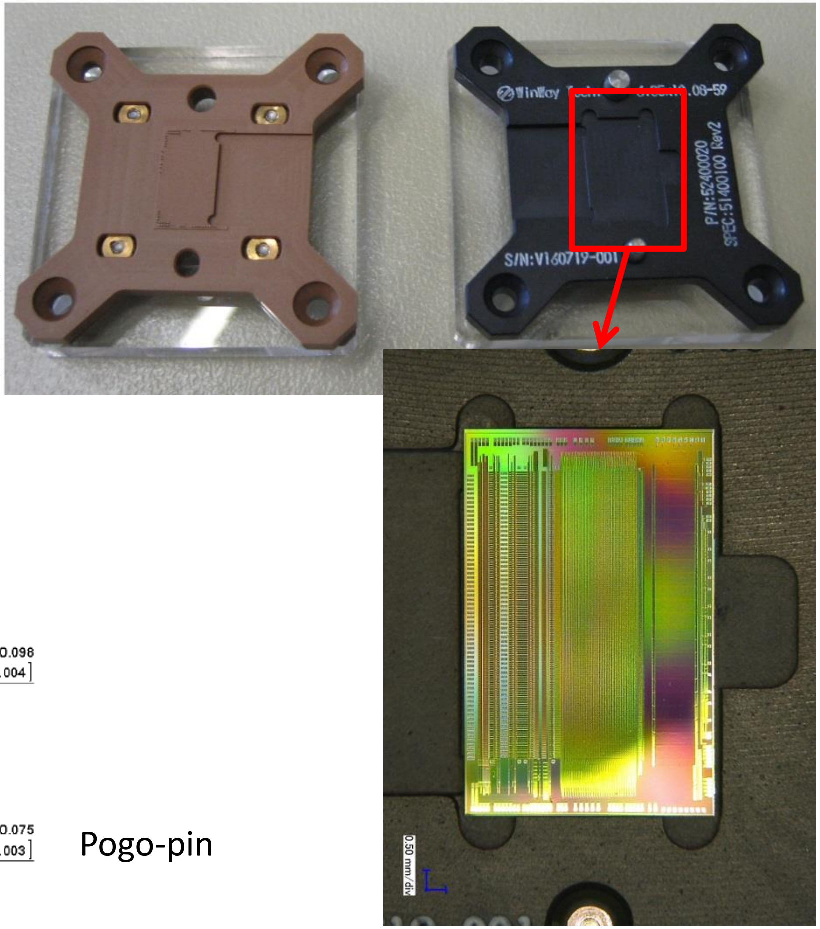
testsocket for the ASIC-TAB-bonds

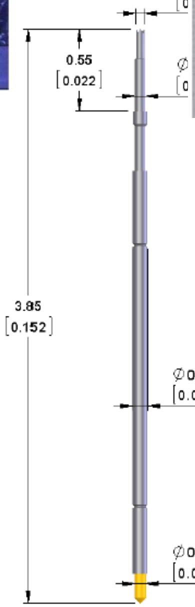






testsocket for the sensor-TAB-bonds



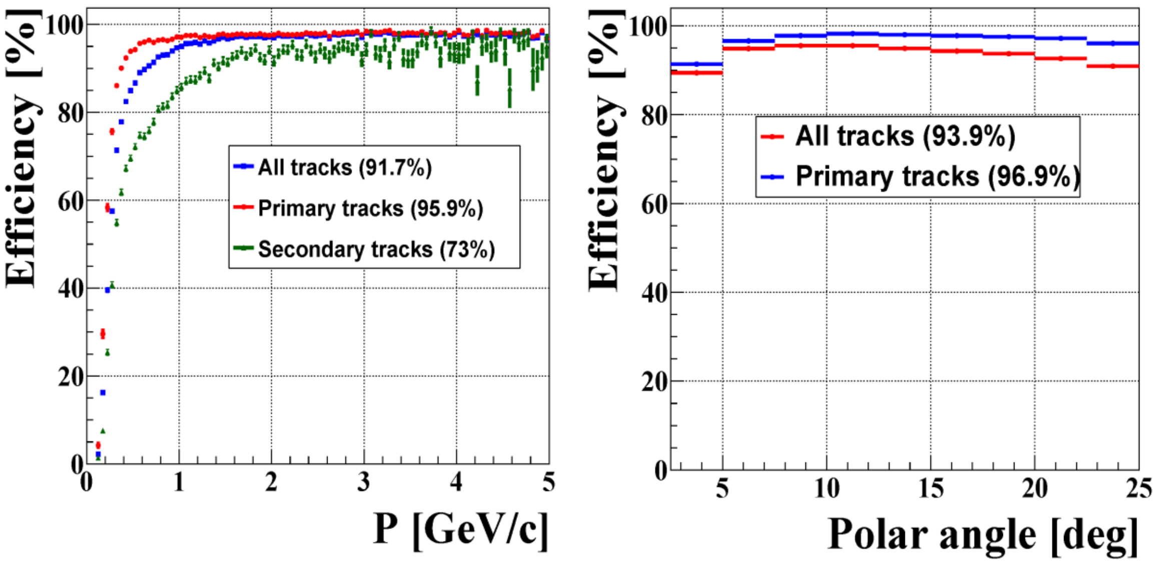


Pogo-pin

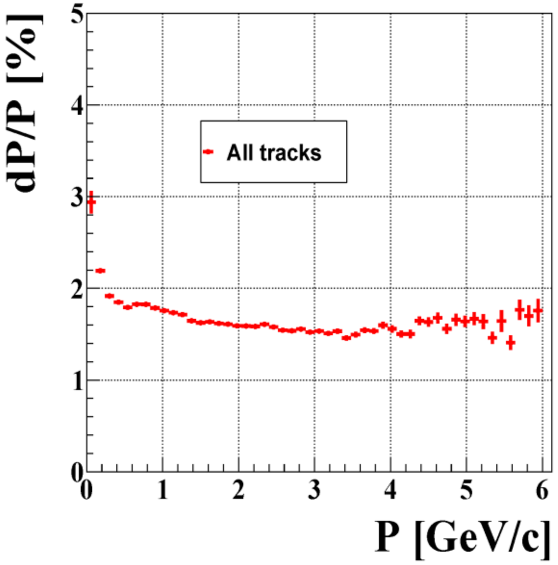
STS performance simulation

- detailed, realistic detector model based on tested prototype components
- CbmRoot simulation framework
- using Cellular Automaton / Kalman Filter algorithms

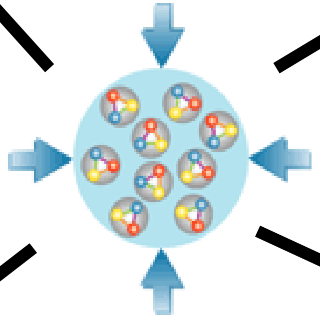
track reconstruction efficiency



momentum resolution



CBM-related Chip Developments and Options



PADI for Diamond
M. Ciobanu, ISS

PADI for TOF
M. Ciobanu, ISS
Bucharest

GET-4 TDC (TOF)
H. Flemming, H. Deppe, GSI

CBM MuCH XYTER
E. Atkin et al, MEPhI

CBM STS-XYTER/MuCH-XYTER
AGH Krakow, R. Szczygiel et al

SPADIC for TRD
ZiTi Heidelberg, P. Fischer et al

SPADIC 2.0 with e-link interface

CBM-GBTx
Chipset ordered from CERN

GBTx
FPGA emulation for
VECC and JINR

Rad tolerant LDOs
SCL Chandigarh, India

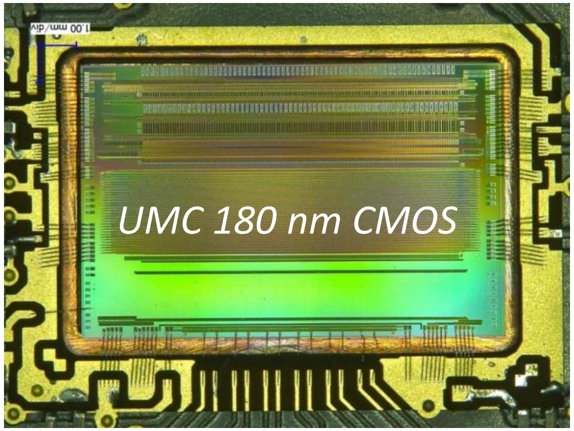
Fully digital Read-out ASIC “STS-XYTER”

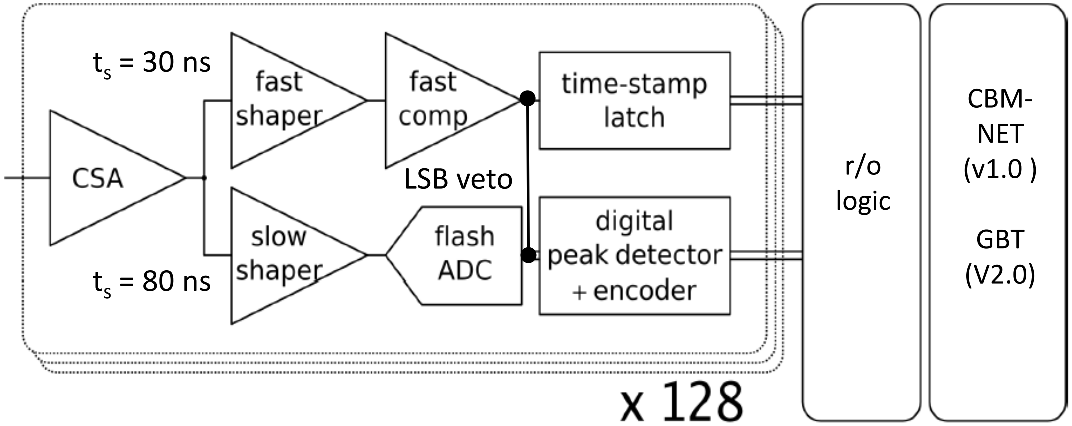
- *purely data driven read-out*
- *time-stamped data elements*
- *250kHz per channel*

for every channel:

- fast branch: time-stamp
- slow branch: signal height digitization (energy)

STS-XYTER ASIC





channels	128, polarity +/-
noise	< 1000 e^- under load
ADC range	16 fC, 5 bit
clock	160 MHz
power	< 10 mW/channel
timestamp	< 5 ns resolution
out interface	5 × 320 Mbit/s LVDS

noise minimization in self-triggering system:

effective two-level discrimination

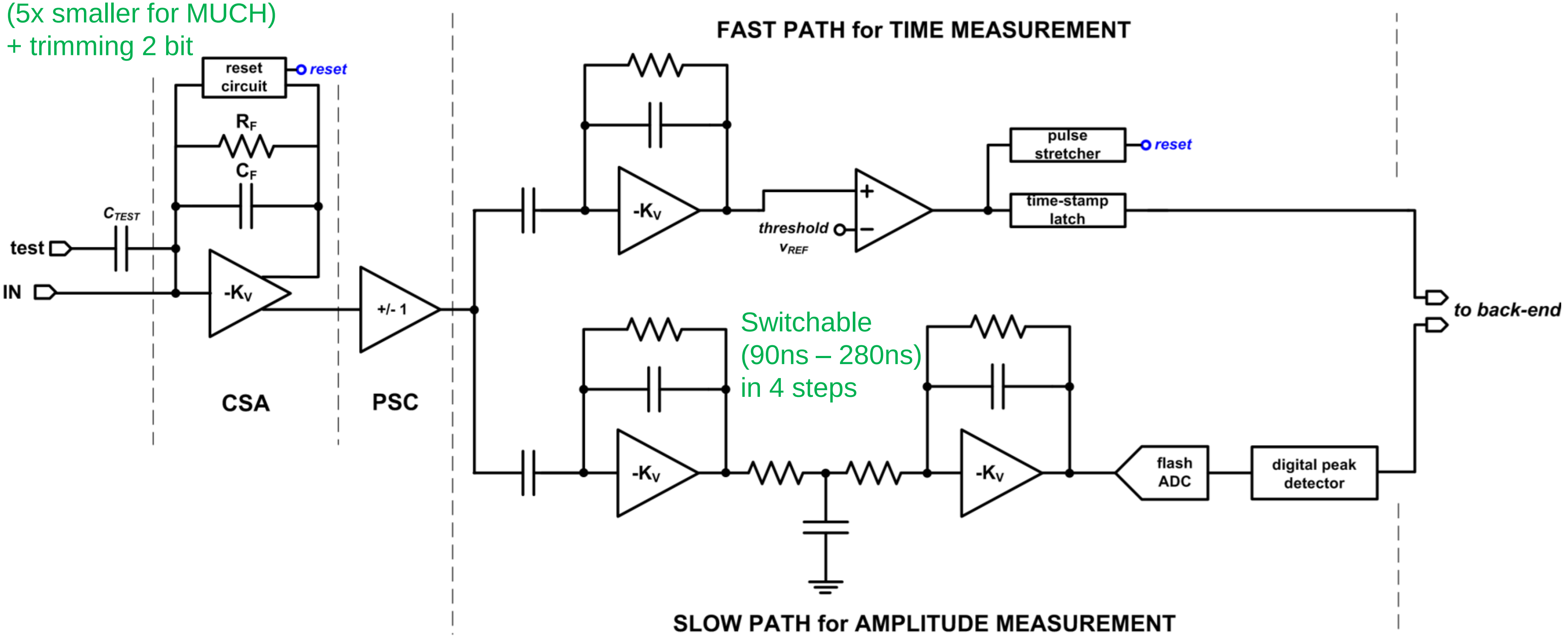
- trigger to the timestamp latch vetoed if ADC-LSB generated no signal

Design Team:
R. Szczygiel et al. at AGH Krakow/Poland

Analog Front End - overview

Switchable gain
(5x smaller for MUCH)
+ trimming 2 bit

Switchable
(90ns – 280ns)
in 4 steps



STS-XYTER

R. Szczygiel et al. AGH Krakow

STS-XYTER turns into MuCH-XYTER via Gain Switch

- Submission Review in Feb. 2015: Noise is an issue →

system issue, optimization with complete system perspective,

extensive architectural studies → goal < 1000 ENC

- Submission Review in Oct. 2015 → full go for submission

- STS-XYTER 2.0: adaptation to GBTx-eLink-readout, STS-r/o protocol

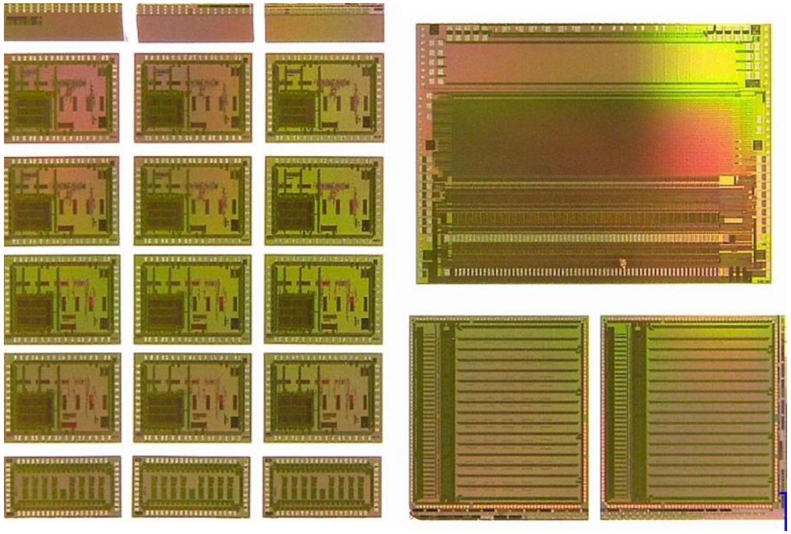
→ intensive collaboration AGH-WUT (W. Zabolotny (DPB)) on design and verification

  - STS-XYTER defines critical path for STS!
  - → all architectural elements included!

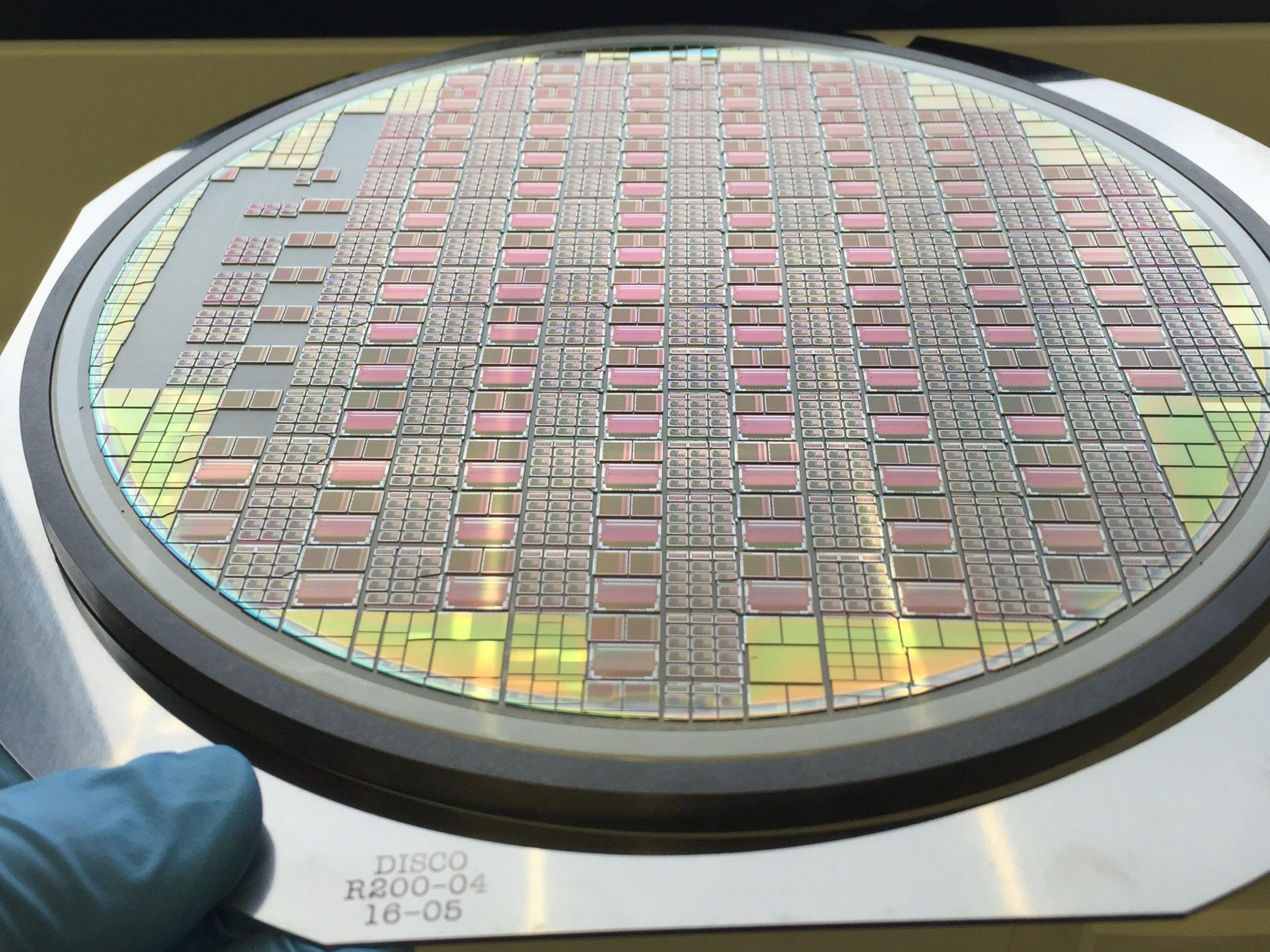
Long awaited STS-XYTER 2.0 Submission Mai 2016

...evolved to a grand CBM-Joined 6-Chip Submission

- STS-XYTER 2.0 → yield 930 chips for STS- and MUCH-prototyping
- TOF readout ASICs, Volume production for operation at STAR
  - Get4-TDC in two versions:
    - Bug-fix version
    - Version for robust operation at 40MHz
  - PADI – fast 8-channel TOF pre-amp



- SPADIC V2 → prototype run with CBM compatible e-link interface


DISCO
R200-04
16-05

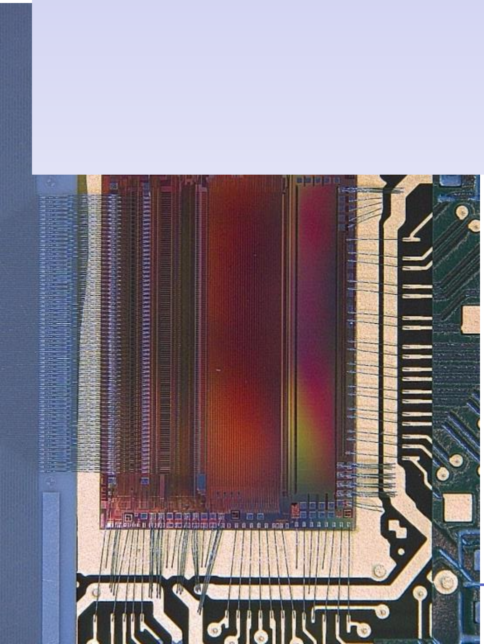
The Readout-ASIC STS-XYTER

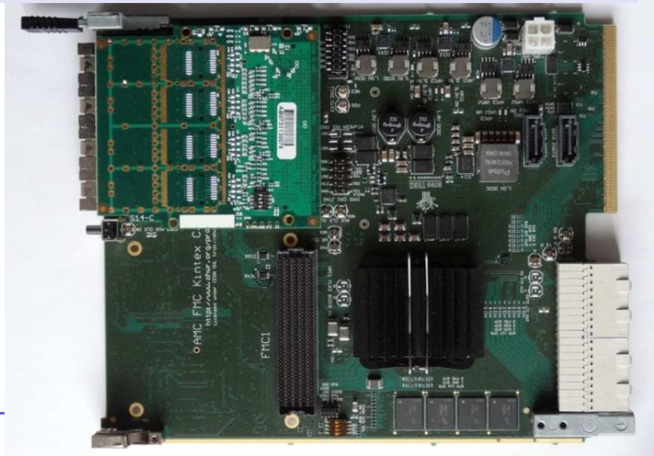
- The moment of truth:

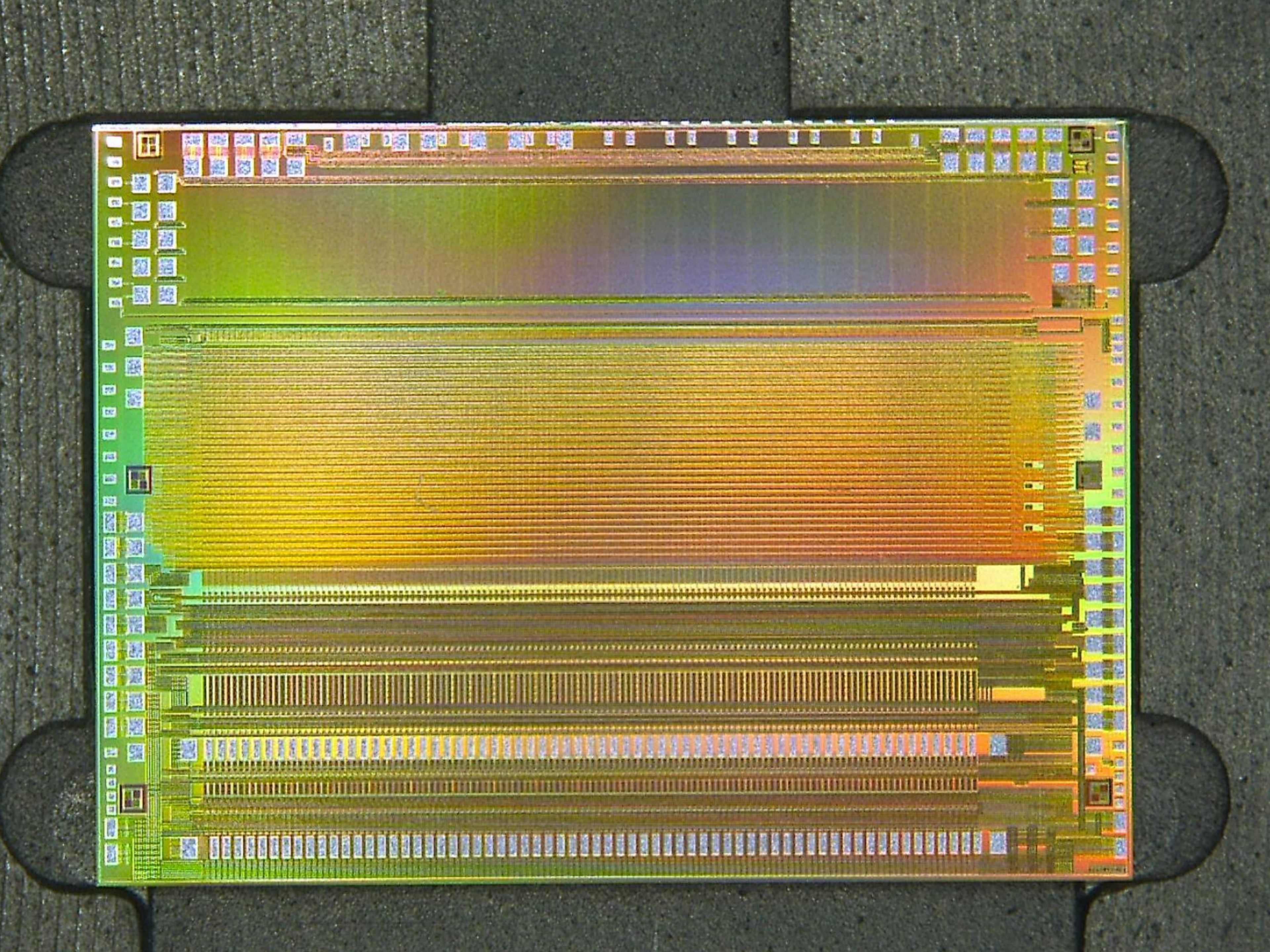
  Testing is a joined AGH, WUT, VECC and GSI effort

  → workshop on STS-XYTER testing Feb. 2017 in India

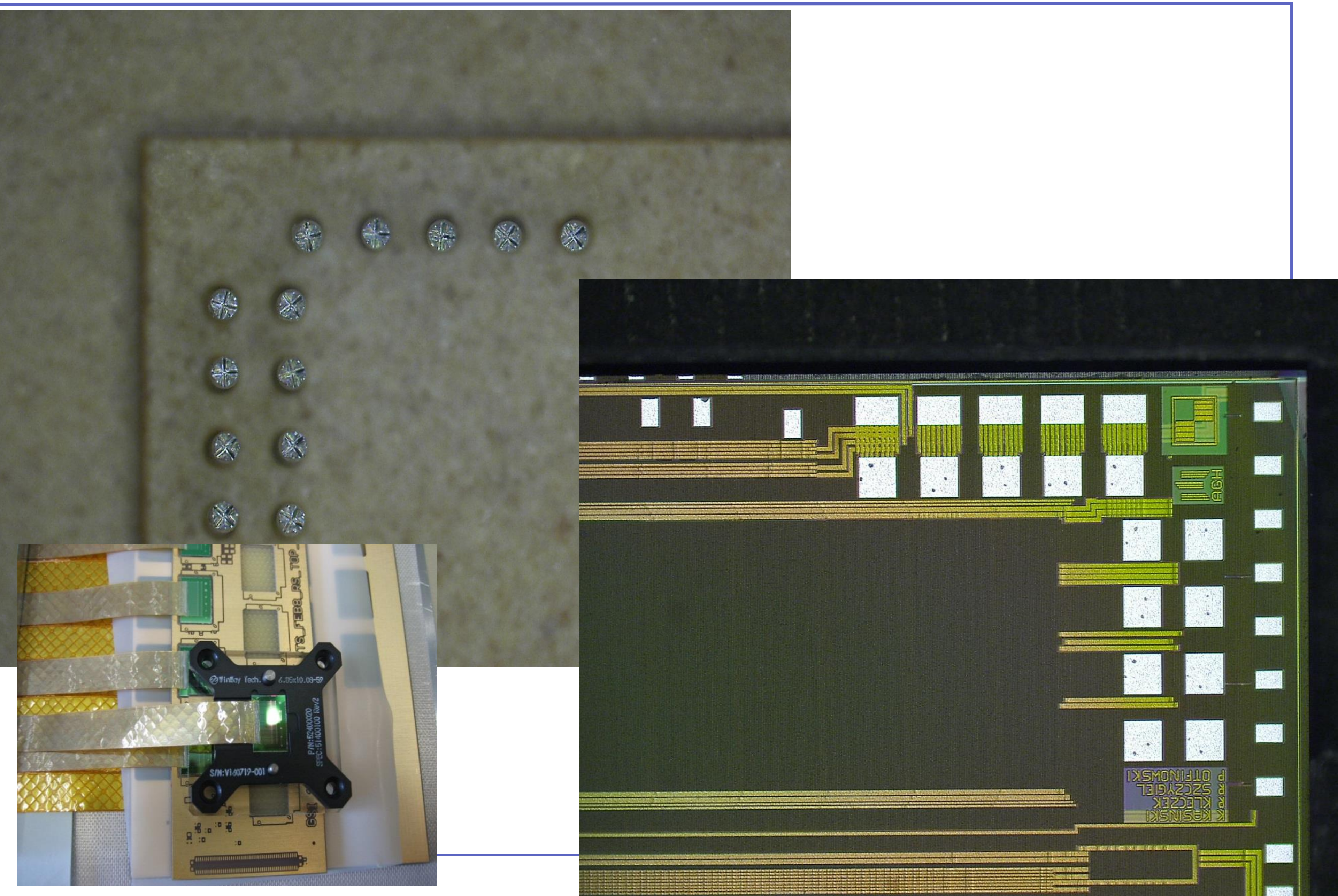
- Beam-time Feb. 2017 at Helmholtz FZ-J COSY: Rad. tests





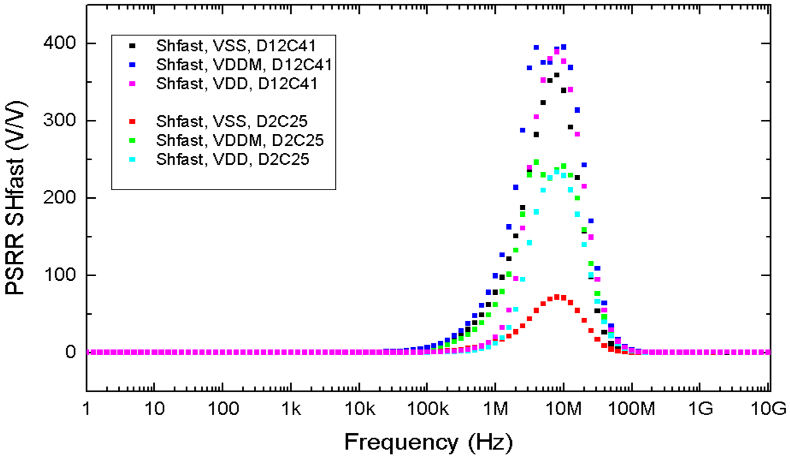


Dicing precision successful: 100µm Pogo-Pins match!

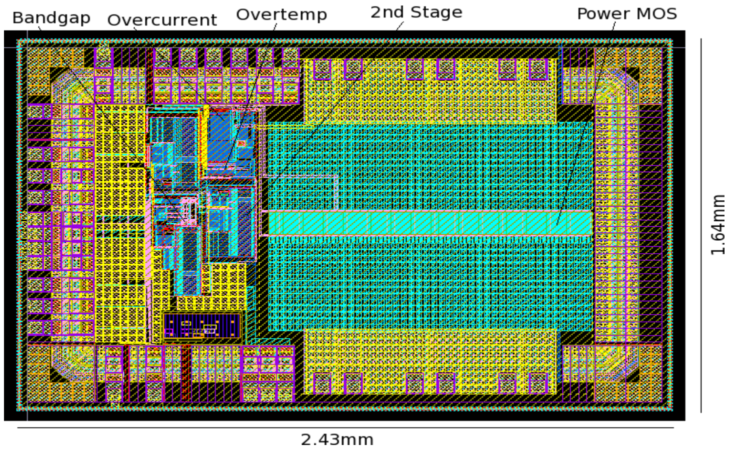


SCL realizes radiation tolerant LDOs for CBM

- Sensitivity to Total Ionizing Dose evaluated by VECC Kolkata → OK for CBM
- Sensitivity to Single Event Upset evaluated by GSI at COSY, FZJ → OK for CBM



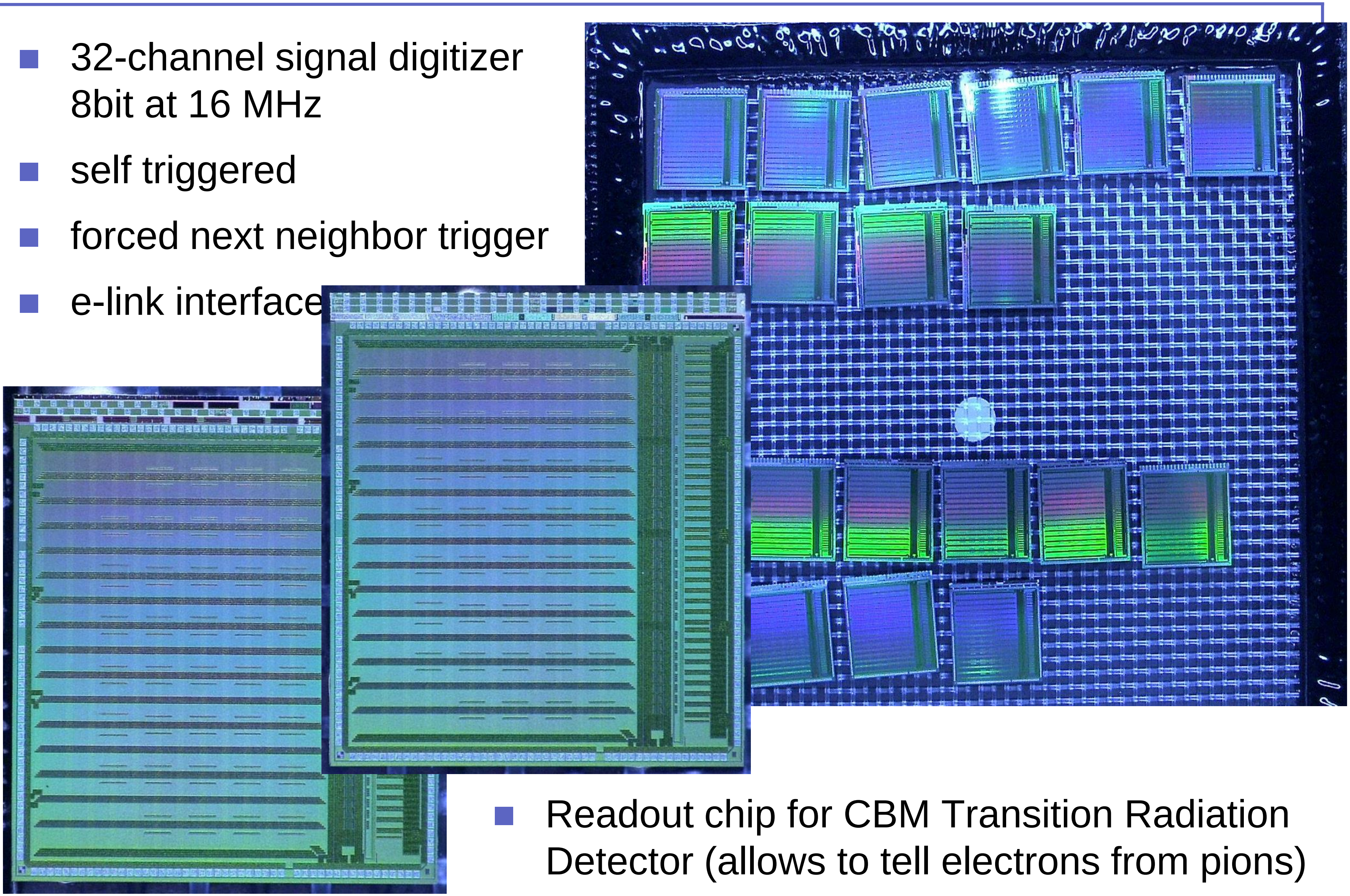
STS-XYTER single ended cascode very sensitive to supply noise



180nm Tower Jazz Process

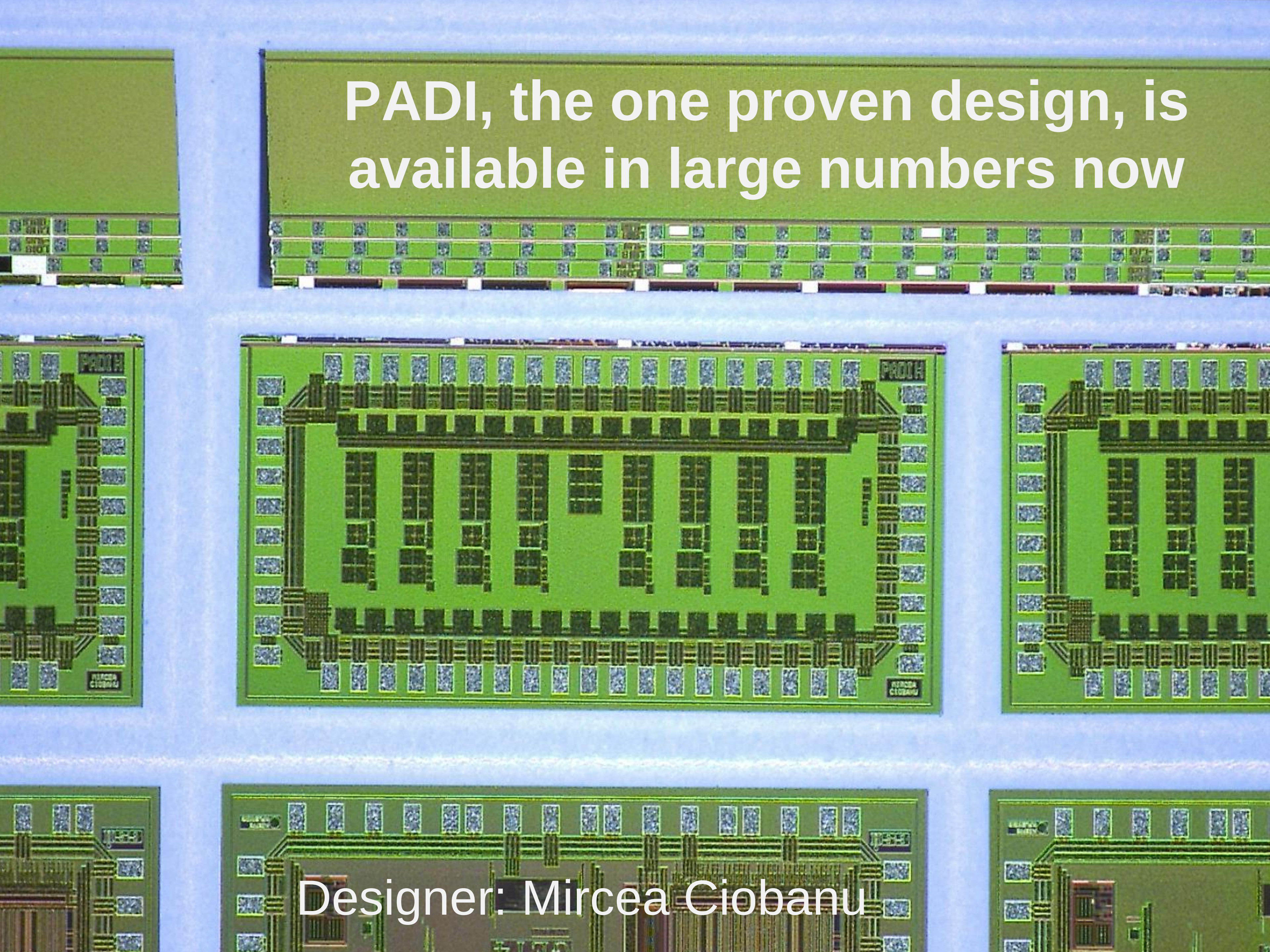
CBM-TRD: Spadic 2.0 in two versions being tested

- 32-channel signal digitizer 8bit at 16 MHz
- self triggered
- forced next neighbor trigger
- e-link interface



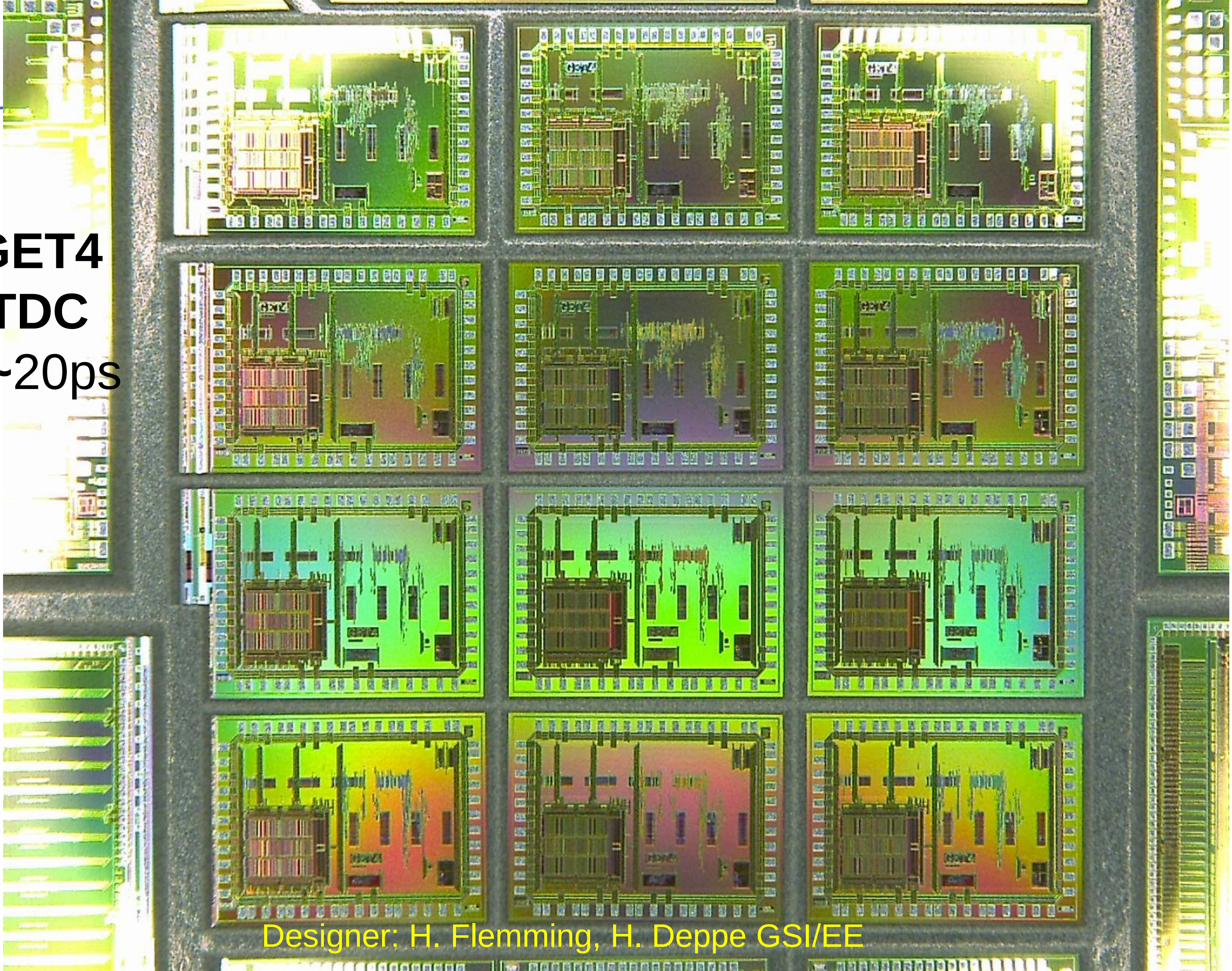
- Readout chip for CBM Transition Radiation Detector (allows to tell electrons from pions)

PADI, the one proven design, is available in large numbers now



Designer: Mircea Ciobanu

GET4
TDC
σ~20ps

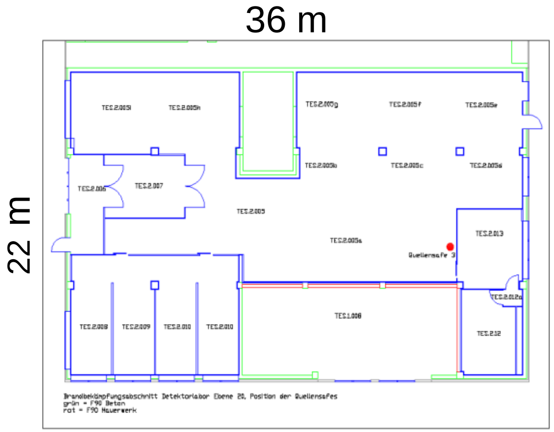


Designer: H. Flemming, H. Deppe GSI/EE

Summary

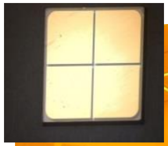
- Heavy-ion physics → nucleus-nucleus collision physics
  - investigation of the properties of nuclear matter in collisions of nuclear beams
  - high charged particle multiplicities, embedded in those: “rare probes”
    - challenge: charged-particle tracking, decay topology recognition,
    - additionally: micro vertex detection
- Silicon detectors can meet the tracking requirements:
  - fine segmentation, low material budget, read-out, radiation tolerance
  - challenge: keep the sensor benefits in a realistic detector system
- Careful full system design needed
  → also several dedicated specialized microchips (ASICs)
- Outlook: We will be diving into our production phase now...

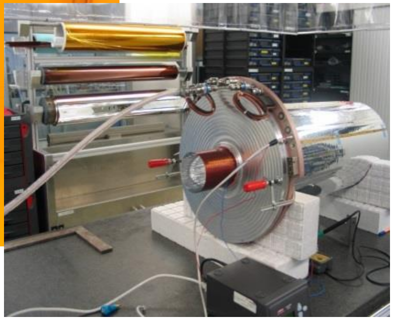
Detector Laboratory at GSI: 600 m² Clean-Room



Competences:

- Micro Patterned Gaseous Detector Technology, GEMs
- Silicon Strip Detector Integration
- ASIC Handling and Integration
- Diamond Detectors





Machinery:

- Laser Lithography
- PVD
- Bonding Automates
- Probestation and Chip Handling
- Automated Wire Winding
- Digital Microscope
- Thin Foils Handling and Processing
- Detector Ageing Teststands
- Large Prototyping CNC Milling Machine