Implementation and evaluation of custom logic for various configuration schemes based on I2C and HDLC protocol for ALICE Common Readout Unit(CRU)

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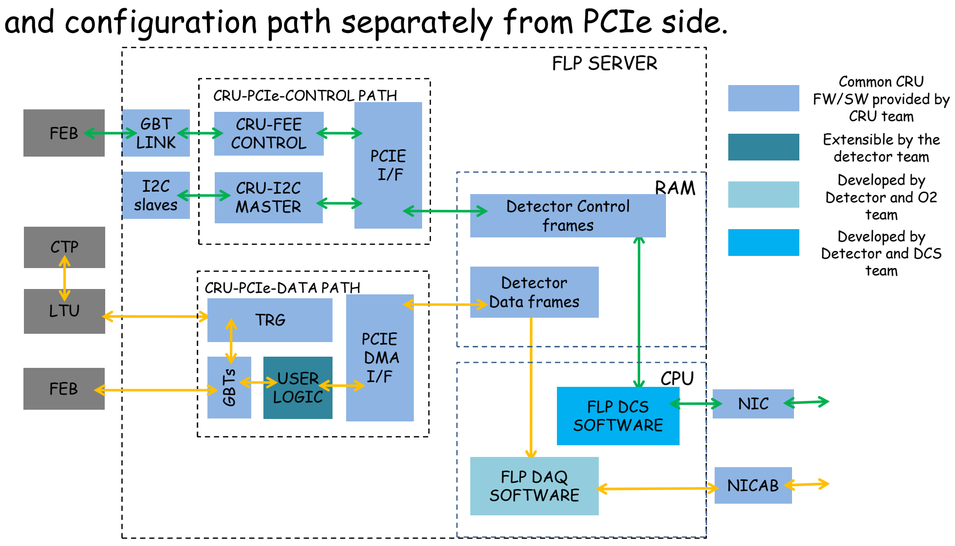
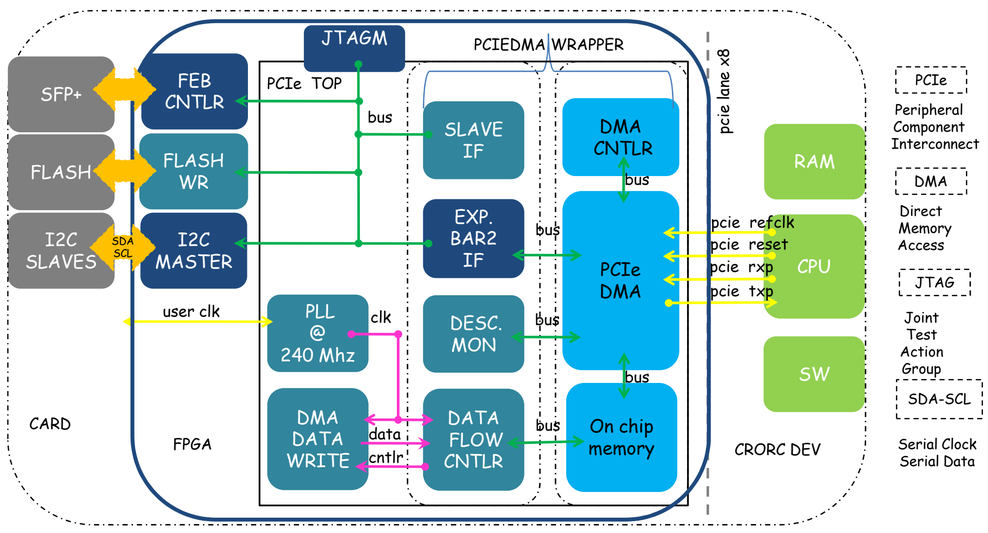
CRU is FPGA based architecture to set up bi-directional communication path between most of the ALICE sub detector system and online-offline system (O2). The figure below shows two flow paths i.e. data and configuration path separately from PCIe side.



The major roles of configuration schemes in CRU are the following:

A. Upload configuration data associated with on board components via PCIe-CRU control interface from DCS servers into CRU

B. Upload detector control information associated with various FEB boards from different detectors via PCIe-FEE control interface from DCS server into CRU



The evaluation PCIe based configuration interface includes FW as well as SW:

A. VHDL based user logic development to interact with open core I2C master and HDLC protocol

B. VHDL based Avalon slave interface to pass data through PCIe BAR master or JTAG master to I2C master or FEB controller

C. VHDL/Verilog based user logic validation using simulation as well as in real time.

D. Software script for scan and configure available slaves on board and loop back test of internal/external control (IC-GBTX/EC-SCA) module.

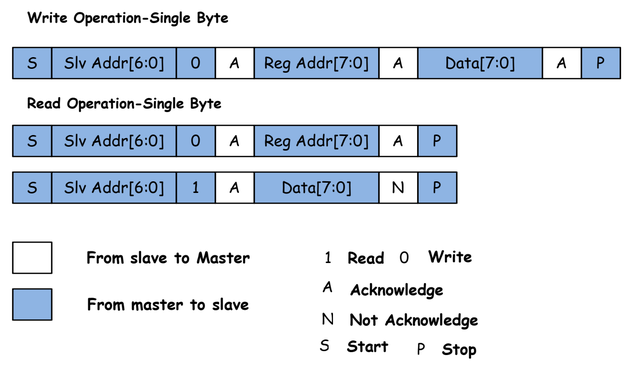
E. Interact with GBTX and GBT SCA on VLDB board from inside CRU via GBT frame.

We are using ALTERA DEV KIT having ARRIA 10 FPGA as hardware platform and CERN Cent OS 7 (CC7) as software platform.

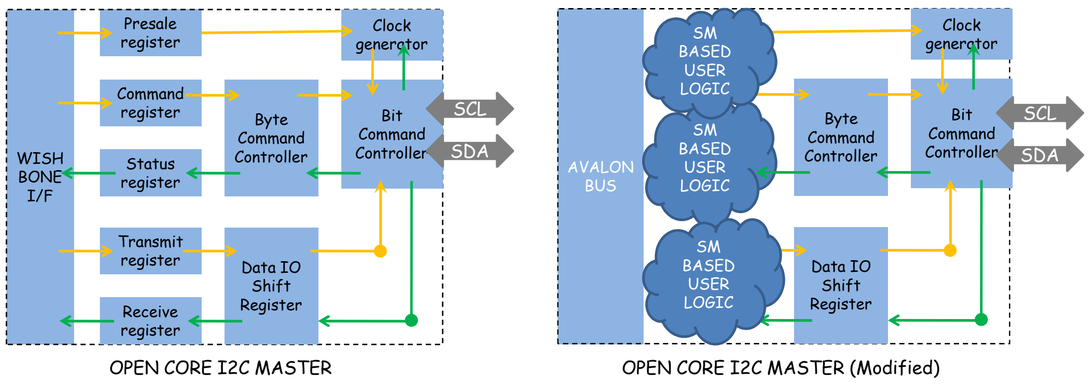
I2C(Inter-integrated circuit) protocol features:

1. Two-wire, bi-directional multi-master serial bus.
2. Suitable for low speed communication over short distance.
3. Two output lines. One is SCL used as clock signal for SDA.
4. Supports three clock speeds (100 khz/400 Khz/3.5 Mbps) .
5. SCL/SDA pin of slave devices must have open-drain/collector outputs.
6 .The SCL and SDA pins should be defined as tri-state buffer.

In principle,I2C slave has multiple 8 bit registers for configuration. I2C master interact with slave having 7bit/10 bit address to read or write those configuration registers. There is pre-defined way for each slave to write and read slave register as shown below. The user logic should be written in the same way mentioned in slave datasheet for register configuration

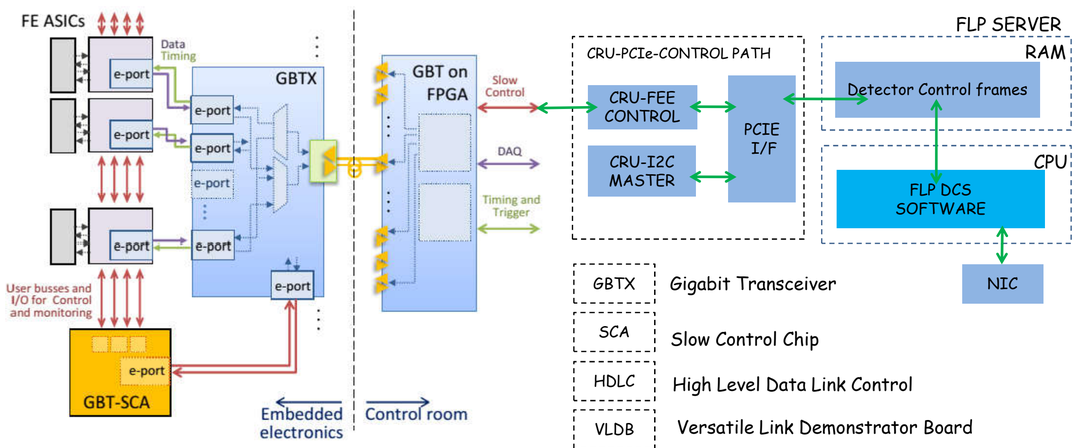


Open core I2C master has multiple command registers which are to be configured by the user using wishbone bus to pass data/control info to the I2C master core. Wishbone bus is not compatible with Altera. The bus has been replaced by Avalon bus supported by Altera to pass data/control for configuration. A bridge like state machine(SM) based user logic has been placed in between Avalon bus and open core I2C to take 32 bit data as input and generate command for I2C mater. The debug and monitoring logic has also been added to detect loss of arbitration and get back the state of the SM while debugging. The figure below shows the difference of open core I2C master and the one custom made for ALICE -CRU.



OPEN CORE I2C MASTER — OPEN CORE I2C MASTER (Modified)

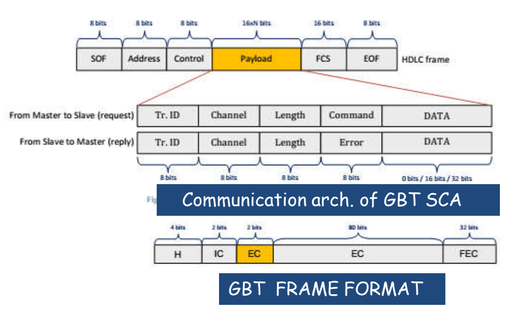
There are front end electronic board (FEB) related ASICs like GBTx and GBT-SCA used to configure detector specific ASIC of different sub-detectors and monitor temperature, voltage. VLDB board has one GBTX and GBT-SCA ASIC. Using that board, a loop back test has been done upto GBT-SCA. The figure below shows general architecture of FEB board.



GBT-SCA can only be accessed through GBTX. So, configure the GBTX ASIC first and then interact with GBT-SCA chip when the GBTx is up. The configuration data to be sent is wrapped up in HDLC frame format as per HDLC protocol. As HDLC protocol only defines data link layer. We must add physical layer on top of it. So, HDLC frame is put into GBT frame format and send optically using Gigabit Transceiver(GBT) protocol developed at CERN.

Three types of information slow control, data and timing & trigger can be sent over GBT. Here, we are interested only in slow control data. There are mainly 4 bits dedicated for IC/EC communication in GBT frame. However, in case of large configuration, the payload field of GBT can be used to send detector specific data. The CRU-FEE logic mainly deals with making of HDLC frame from data. The figure below shows HDLC frame format and various sub-field of field.

Script is being written in TCL and Python to scan available I2C slaves on board and configure slaves like PLL, optical modules. The TCL script is using JTAG master and python script is using PCIe.



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