An efficient approach to manage DMA descriptors and evaluate PCIe based DMA performance for ALICE Common Readout Unit (CRU)

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Agenda

- Overall view of CRU
- PCIe-DMA
  - Basics
  - Architecture (FPGA based)
- DMA descriptor management
- User logic internal architecture (Block Diagram)
- Features of user logic
- Result
• **PCIe (Peripheral Component Interconnect)**:
  1. Protocol implemented in FPGA as per PCIe-SIG standard
  2. Can handle input BW (avg ~96 Gbps) as PCIe offers large BW (User BW ~114 Gbps in Gen3 ×16 mode)
  3. Consume no FPGA resource as it is available as Hard IP from Altera.

• **DMA (Direct Memory Access)**:
  1. Protocol to push data through PCIe interface.
  2. DMA evaluation goal: Use as much possible the PCIe- BW.
  3. Mainly based on Look Up table approach known as descriptor table.
DMA PROFILE:

Throughput:

1. Old: ~51 Gbps

2. New:
   A. With clean FW: ~53 Gbps
   B. With clean FW and SW: ~55 Gbps

PCIe DMA idle time:

MAX: ~3 us
AVG: ~160 ns
FW WR FULL ON CHIP MEM & PULL FOUR DESCRIPTORS

FW WR FULL ON CHIP MEM & PULL NXT FOUR DESCRIPTORS

DMA TRANSFER GOING ON

ALL STATUS RXD BY DAQ SW

ACK BY DAQ SW

CARD FIFO

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SW FIFO
NON PIPELINED DMA

WR FULL ON
CHIPMEM &
PULL FOUR
DESC.

DMA
TRANSFER
GOING ON

ALL STATUS
RXD BY
DAQ SW

ACK BY
DAQ SW

WR FULL ON
CHIPMEM &
PULL FOUR
DESC.

PG(0-3) WR P

PG 0-3 DMA MV

PG 0-3 DMA MV

PG 0-3 DMA MV

PG 0-3 WR P

idle Time

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FW WR FULL ON CHIP MEM & PULL FOUR DESCRIPTORS

1. MEM WR
2. PULL GEN DESC

DAQ SW
1. STS RX
2. ACK = 1

DMA TRANSFER GOING ON

CARD FIFO

SW FIFO
DMA TRANSFER GOING ON

1. MEM WR
2. PULL GEN DESC

WAIT FOR NEXT STATUS

PG(0-3) WR

PG0 DMA MV

PG1 DMA MV

PG2 DMA MV

PG3 DMA MV

PG0 DMA MV

current

pending

pending

new

STS = 1

ACK = 1
<table>
<thead>
<tr>
<th>OLD DMA IF LOGIC</th>
<th>NEW DMA IF LOGIC</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. No handshaking signal from FW side to SW side to trigger the DMA</td>
<td>Ready signal from FW side to SW side to fetch the data</td>
</tr>
<tr>
<td>2. DMA reg. programming was done by SW</td>
<td>Later ready signal is used internally by FW for DMA programming</td>
</tr>
<tr>
<td>3. Status memory has been used for ack. generation</td>
<td>Status memory has been used for ack. generation</td>
</tr>
<tr>
<td>4. No monitoring signal for debugging</td>
<td>Added several monitoring processes to debug the current status of DMA transfer</td>
</tr>
<tr>
<td>5. Good for DMA performance evaluation.</td>
<td>Good for DMA evaluation plus data consistency.</td>
</tr>
</tbody>
</table>

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Run time:
5 Mins =>

Run time:
30 Mins =>

Run time:
60 Mins =>

Run time:
120 Mins =>

DMA PERFORMANCE

Run time:
5 Mins =>

Run time:
30 Mins =>

Run time:
60 Mins =>

Run time:
120 Mins =>

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2/16/2017
THANK YOU