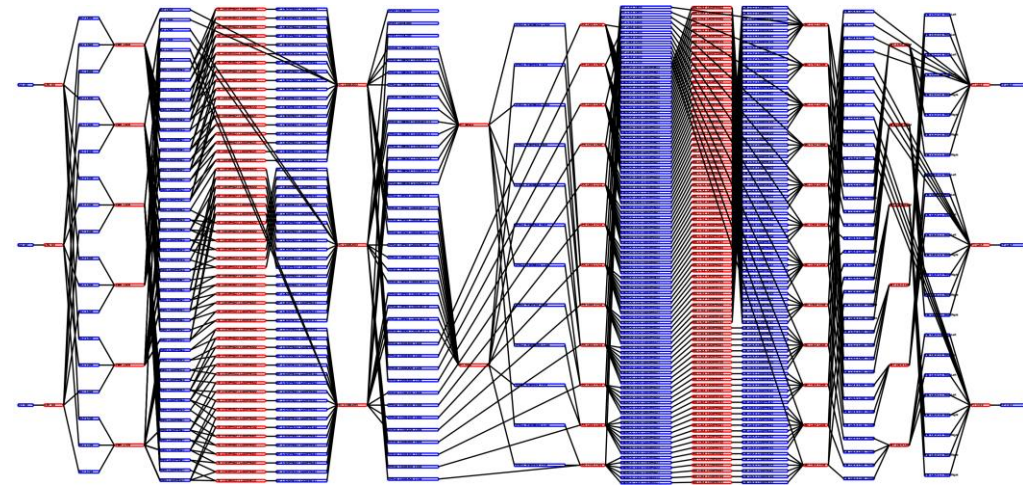
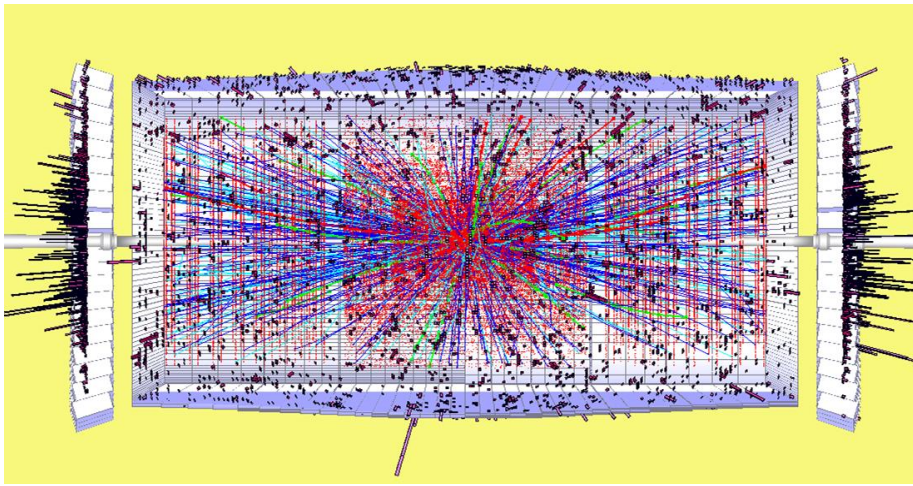


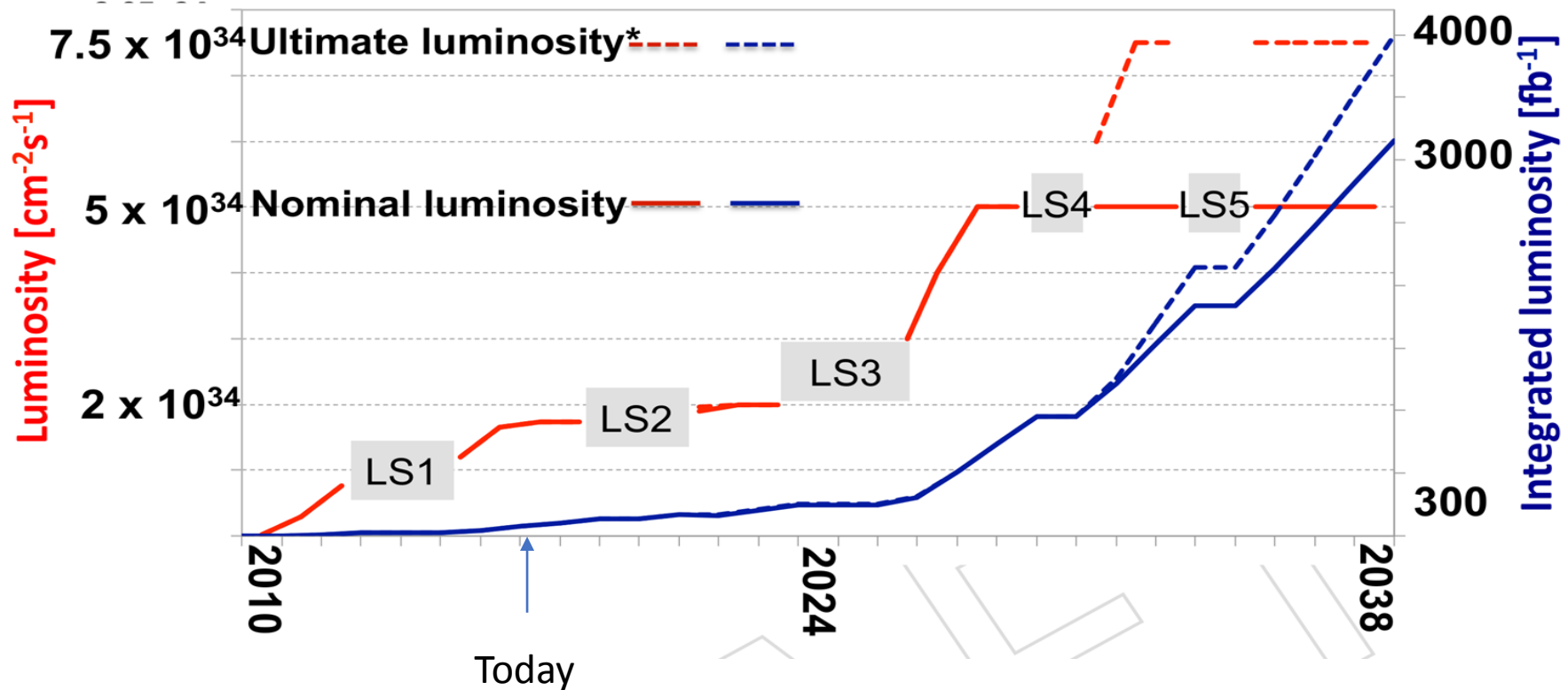
# HL-LHC Upgrades and the Track Trigger

Anders Ryd  
Cornell  
Dec. 13, 2016



# Upgrades to the LHC

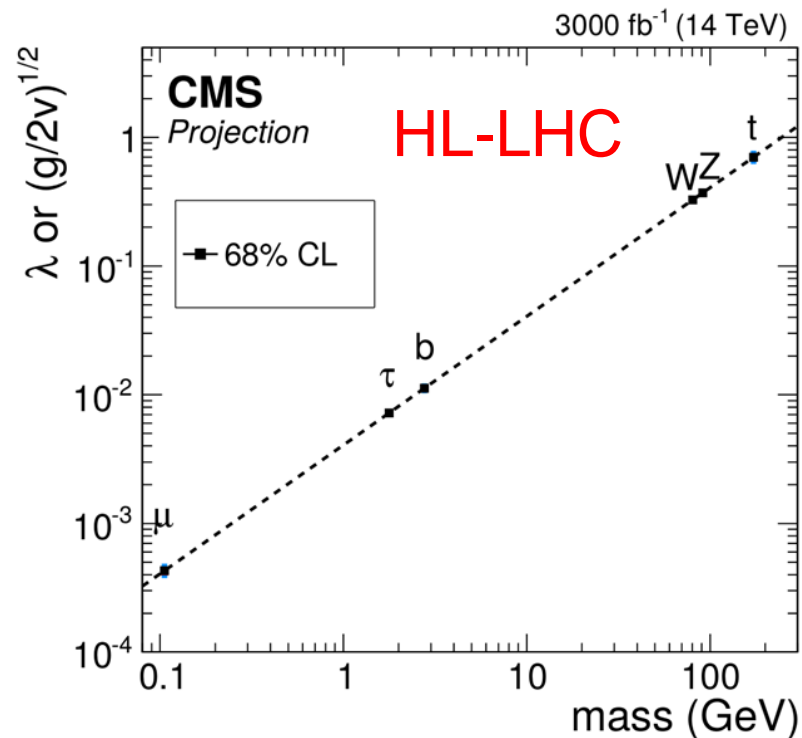
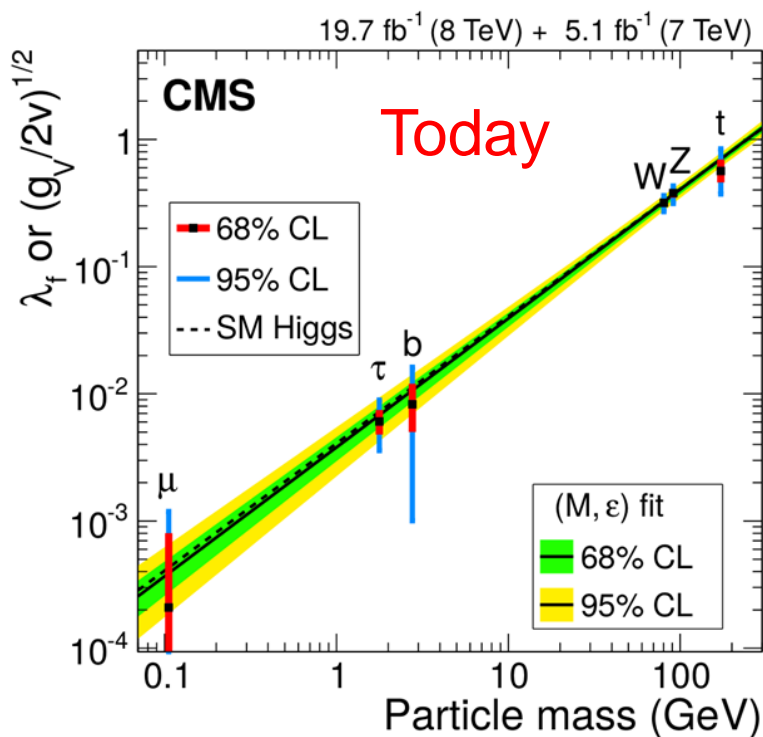
- High Luminosity LHC: 200 proton-proton interactions every 25



While taking data now we are also preparing for the future

# Higgs Studies @ HL-LHC

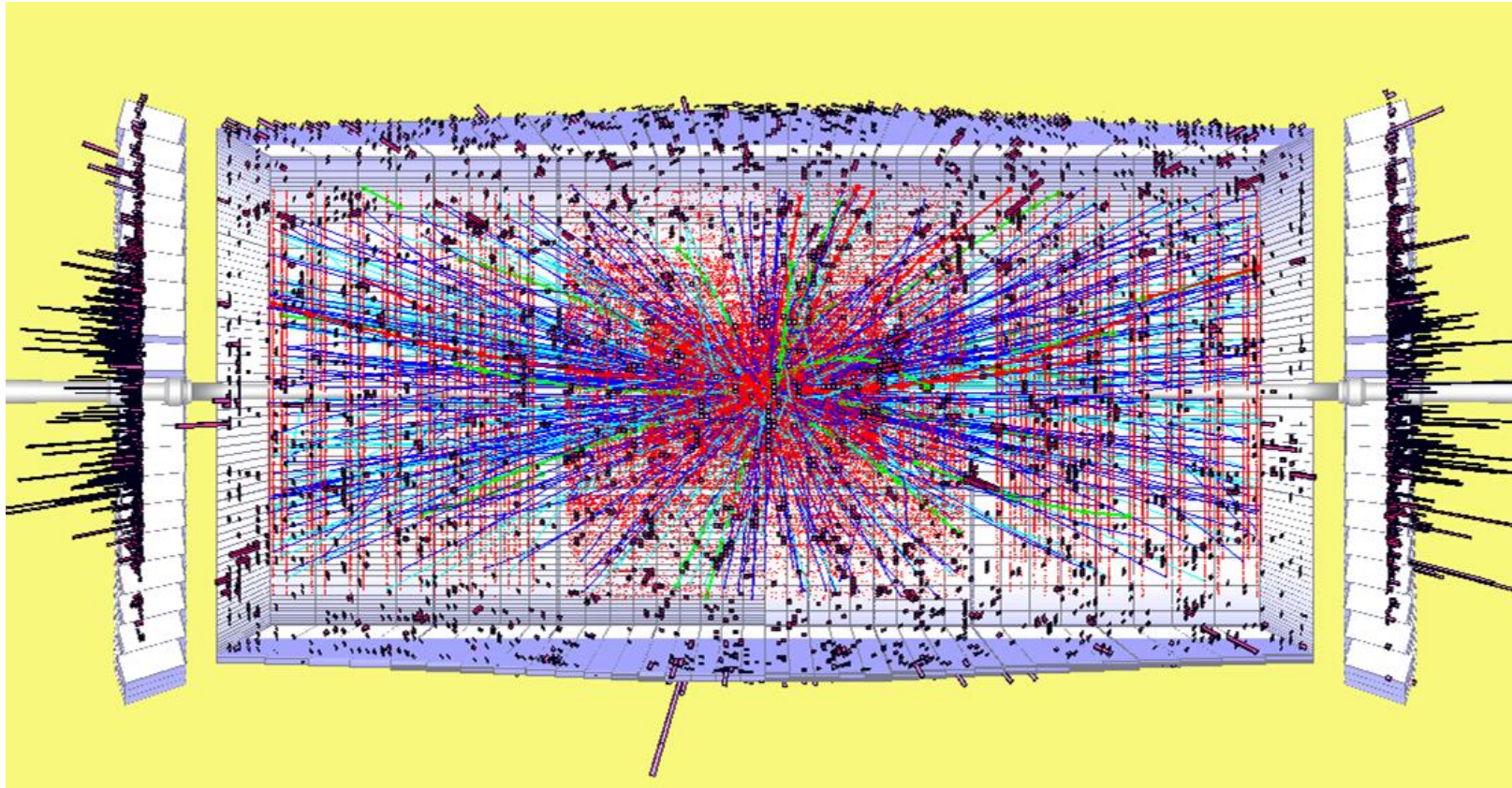
- Detailed exploration of the Higgs discovered during Run 1 is one of the main motivations, e.g. precise coupling strengths:



Is the Higgs responsible for mass generation?

# HL-LHC Challenges

In 2025 the LHC will collide protons at a rate of 140 to 200 proton-proton collisions every 25 ns: ~5-8 billion collisions a second!



**Radiation hardness** – survival of detectors

**Data rate** – data needs to be read out and processed

**Performance** – resolution, efficiency etc.

# Upgrades of the CMS Detector

## Trigger/HLT/DAQ

- Track information at L1-Trigger
- L1-Trigger: 12.5  $\mu$ s latency - output 750 kHz
- HLT output  $\approx$ 7.5 kHz

## Barrel EM calorimeter

- Replace FE/BE electronics
- Lower operating temperature (8 $^{\circ}$ )

## Muon systems

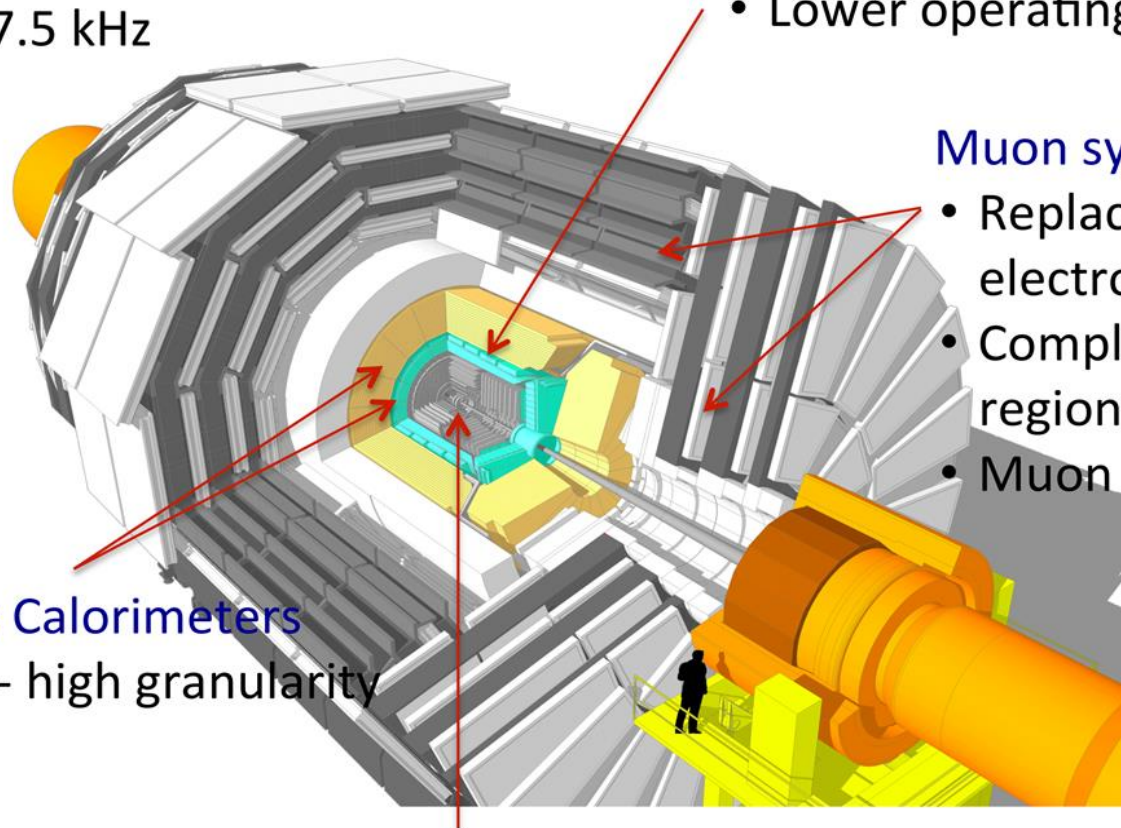
- Replace DT & CSC FE/BE electronics
- Complete RPC coverage in region  $1.5 < \eta < 2.4$
- Muon tagging  $2.4 < \eta < 3$

## Replace Endcap Calorimeters

- Rad. tolerant - high granularity
- 3D capability

## Replace Tracker

- Rad. tolerant - high granularity - significantly less material
- 40 MHz selective readout ( $Pt \geq 2$  GeV) in Outer Tracker for L1-Trigger
- Extend coverage to  $\eta = \sim 4$



# Trigger Challenge

Each collision at the HL-LHC generates about 4 MB of data, @ 40MHz this means 160 TB/s – 1 petabyte in 6s. We can not readout or store this amount of data.

Most events are not interesting; we use the trigger to filter out the interesting events. We have to stages:

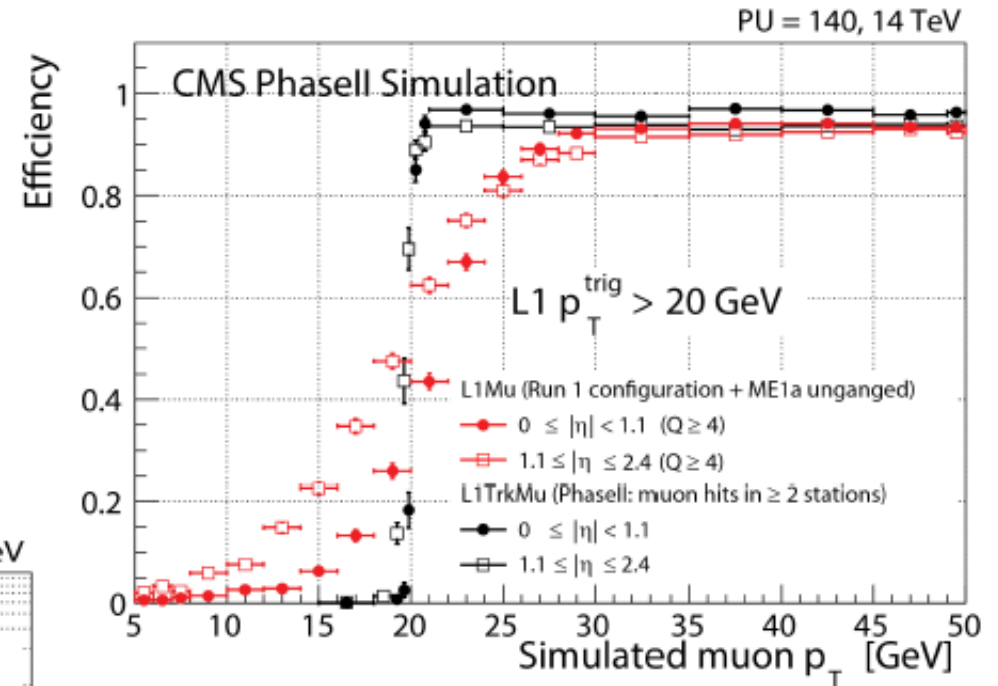
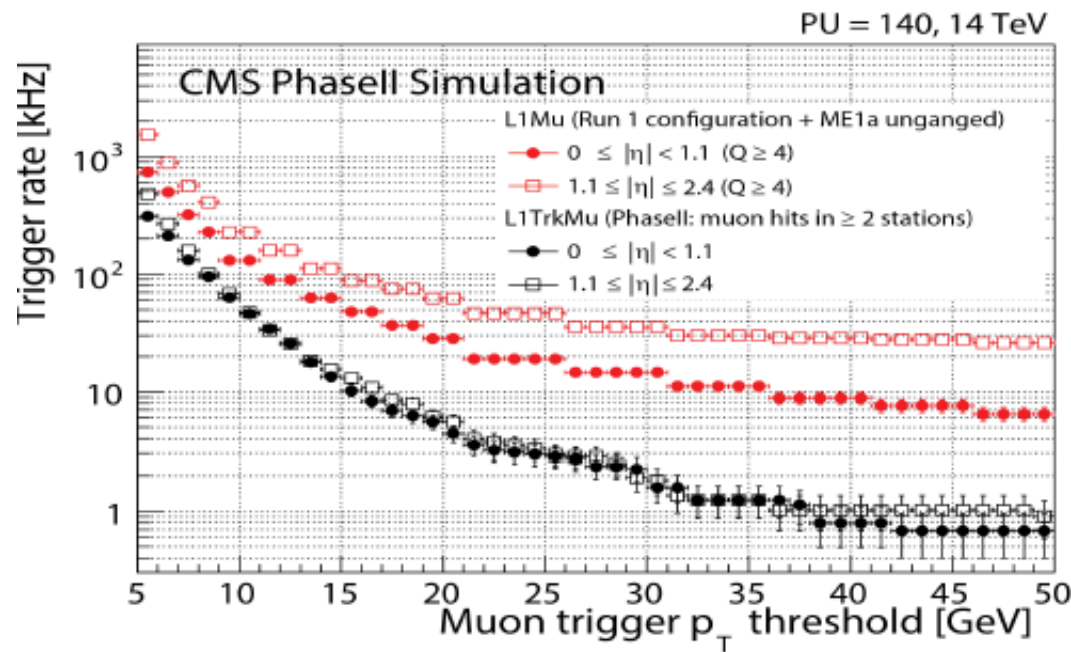
**L1 Trigger** (40 MHz → 750 kHz) – hardware trigger based on reduced readout of Calorimeter, Muon, and Outer Tracker

Outer Tracker is new in the L1 Trigger for HL-LHC

**High-level Trigger** (750 kHz → 7.5 kHz) – Software based trigger with access to full event data

# Use of Tracking in the Trigger

- Track matching to muon candidates has high efficiency
- Muons+L1Tracks provide much sharper threshold

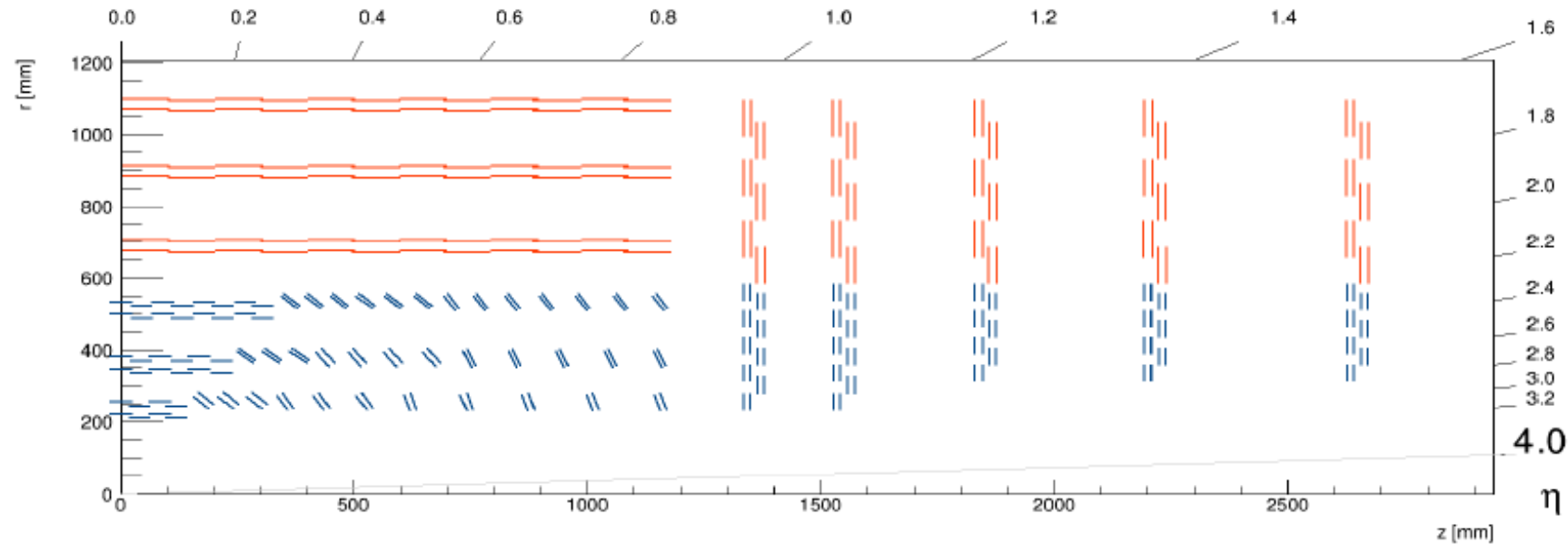


- Sharp threshold allows a significant rate reduction:
  - ♦ Factor  $\sim 10$  reduction @20 GeV

Tracking at L1 is also powerful tool for electrons, taus, jets, photons as detailed in the CMS TP:

<https://cds.cern.ch/record/2020886>

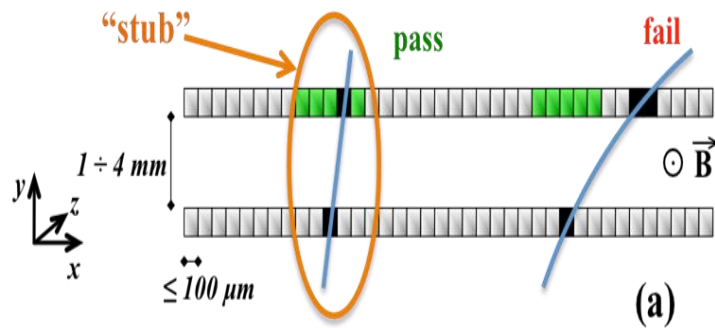
# CMS Tracker Trigger



¼ of Outer Tracker

6 Layers

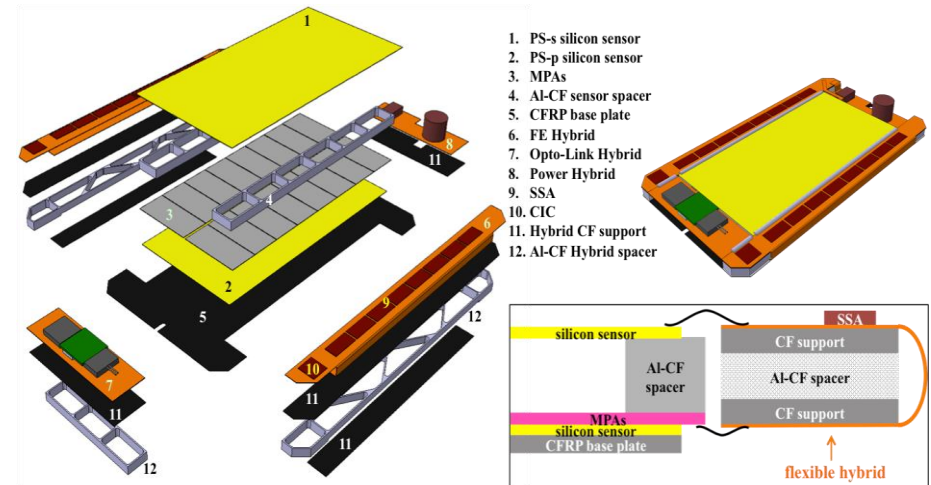
5 Disks



Need  $O(14,000)$  Modules  
Each module 10 Gbits/s

Reduce data volume to  $\sim 100$  Tbits/s  
About 10,000 stubs every 25 ns (40 MHz)

Challenge: Reconstruct about 200 tracks  
every 25 ns – within  $\sim 4 \mu\text{s}$





# Track Trigger Goals

The goals of the track trigger are challenging:

- Tracking in full CMS tracking detector ( $|\eta| < 2.5$ )
- Find tracks with  $p_T > 2$  GeV
- Process every BX
- Latency  $< 5 \mu\text{s}$

A system like this has never been built before (and more challenging than what e.g. ATLAS are planning)

# Track Trigger Implementation

Three major R&D projects with different approaches:

- **Tracklets** - conventional road search
- **Time Multiplexed** - Hough transform based binning
- **Associative Memory** - ASIC assisted parallel lookup

The first two of these are based only on processing in FPGAs. These algorithms make use of the processing power in modern FPGA.

The third approach makes use of an ASIC to do the pattern finding a CAM (Content Addressable Memory).

Last week we had a review of these approaches during the tracker upgrade week. All approaches has made great progress and each shown to provide a viable solution.

# Field Programmable Gate Array

Most (off-detector) electronics for fast signal processing in HEP is now done using FPGAs

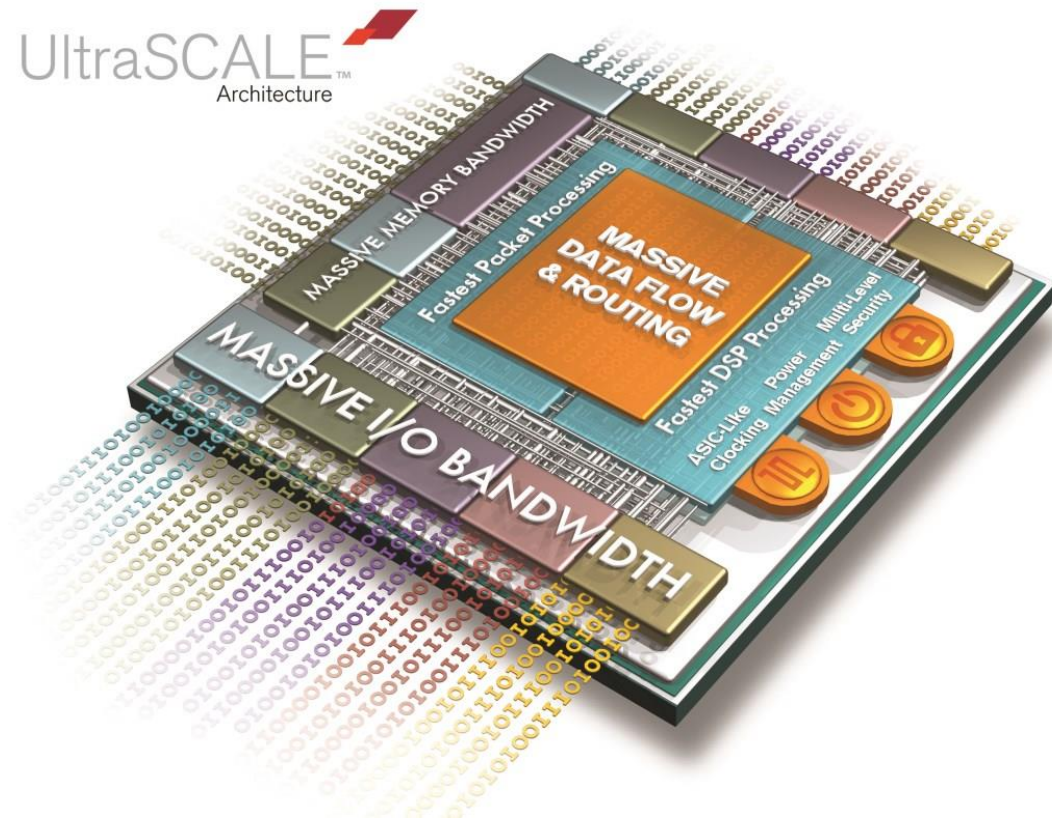
Allows similar performance to ASICs – but the flexibility to be reprogrammed

Performance improvements over the last ~10 years has been remarkable

- 5,000 Digital Signal Processors:  $>8 \times 10^{12}$  multiply-and-add per sec
- 120 Transceivers – each up to 33 Gbits/s: 5.8 Tbits/s
- 4,000 18 kbit memory blocks
- 4,000,000 Logic blocks

Resources allow us to keep up with HL-LHC data (but cost \$\$\$\$)

UltraSCALE™  
Architecture

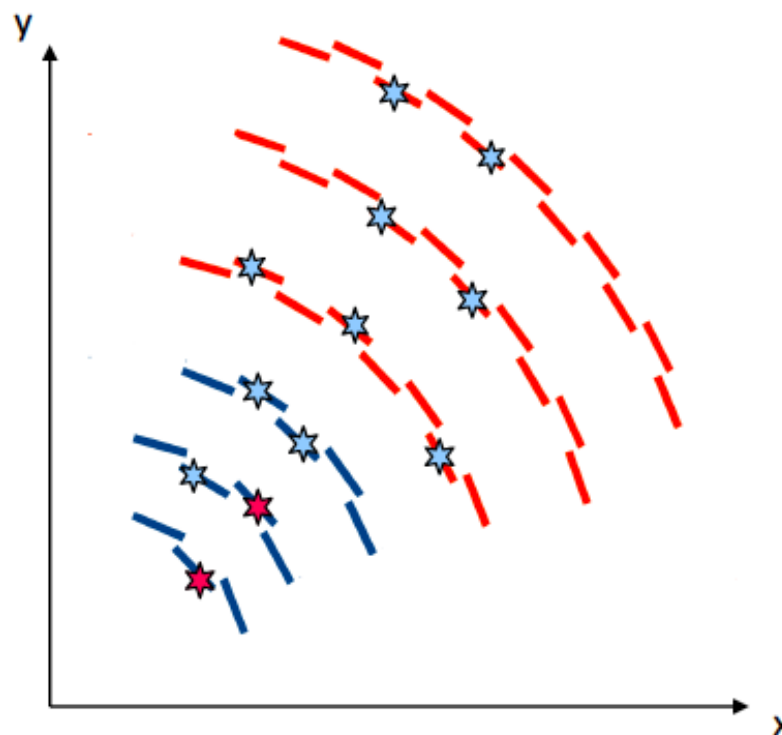


# Tracklet Approach

- I'll show a few slides from the tracklet approach to illustrate the work and challenges that we are addressing

# Tracklet Based Track Finding

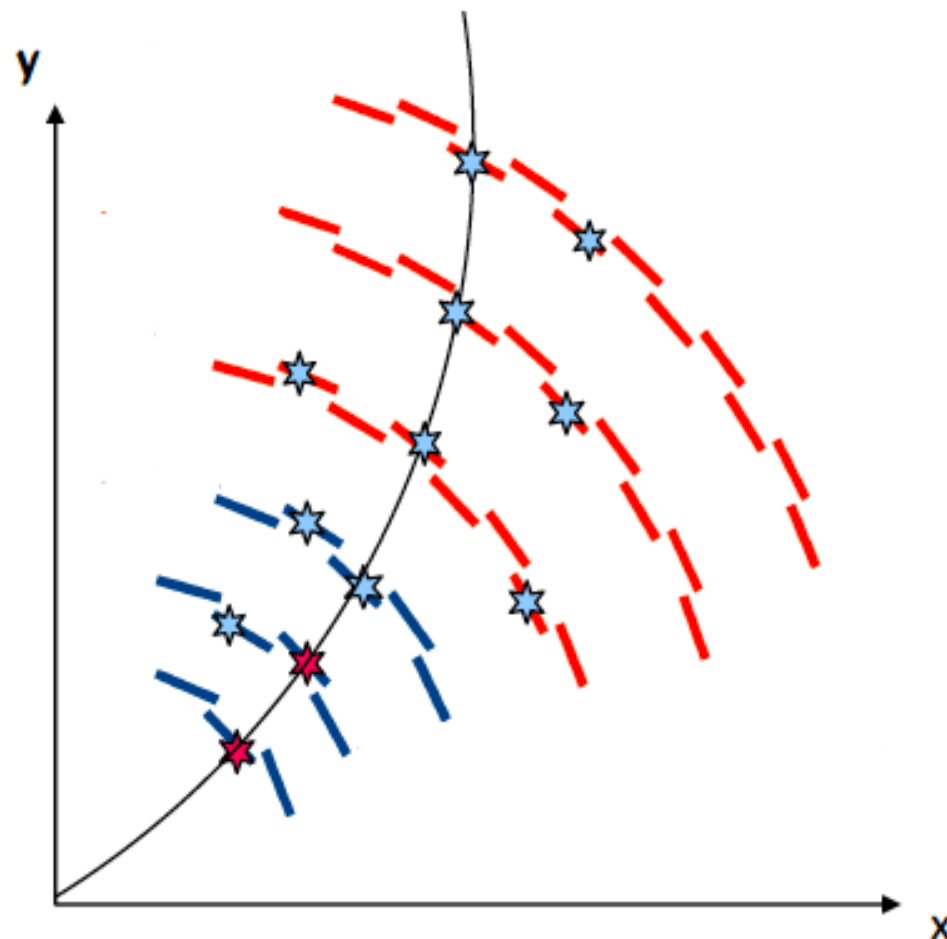
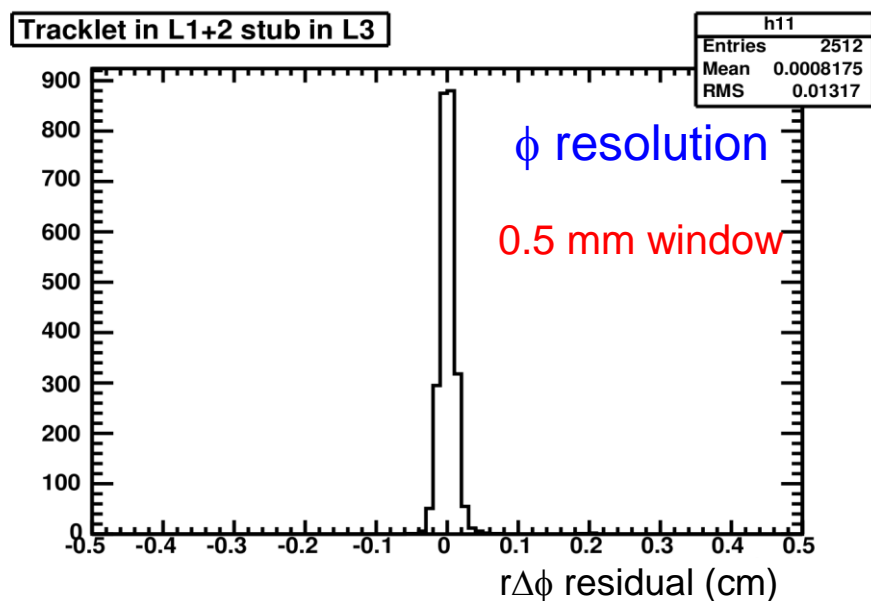
- Form track seeds, tracklets, from pairs of stubs in neighboring layers



# Tracklet Based Track Finding

- Form track seeds, tracklets, from pairs of stubs in neighboring layers
- Match stubs on road defined by tracklet and IP constraint

Matching resolutions for tracklets in L1+L2 projected to L3

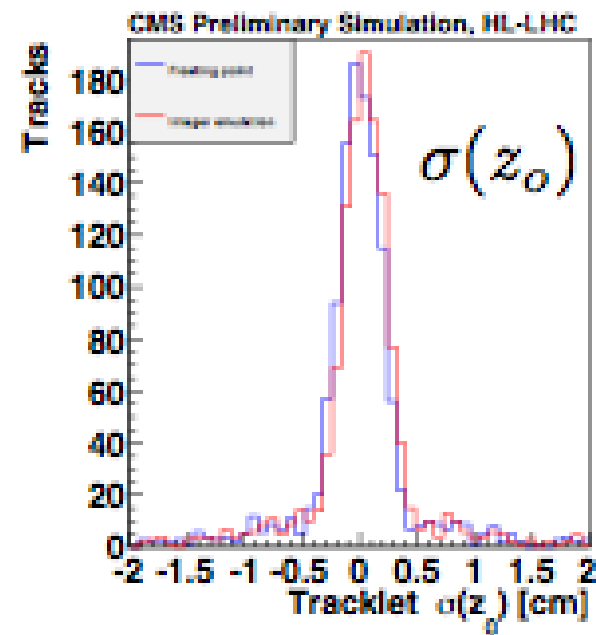
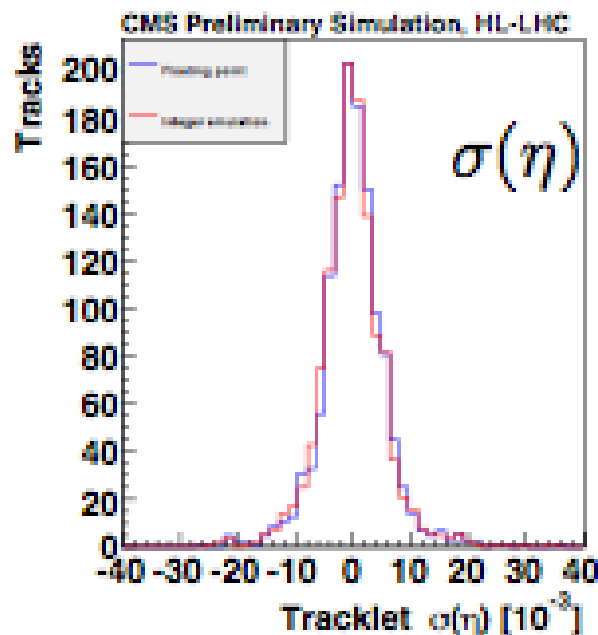
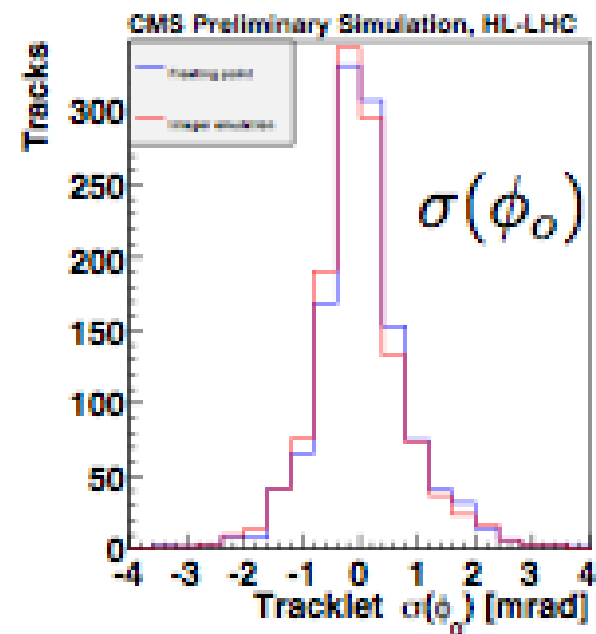
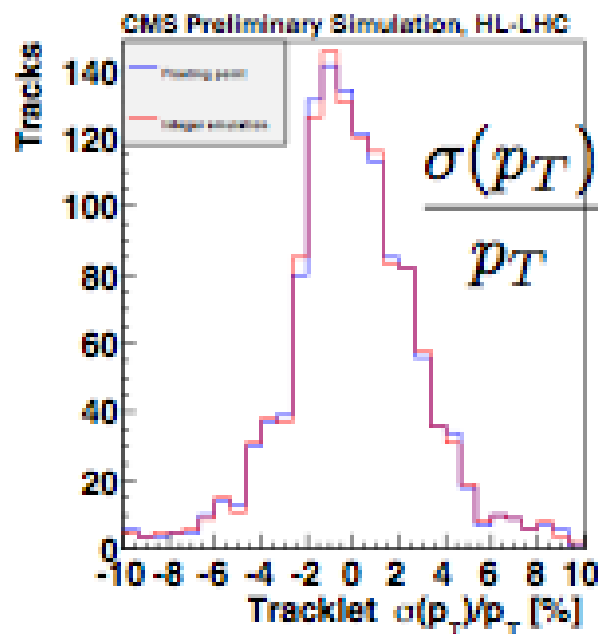


# Tracklet parameter resolutions

Already tracklets have good track parameter resolutions

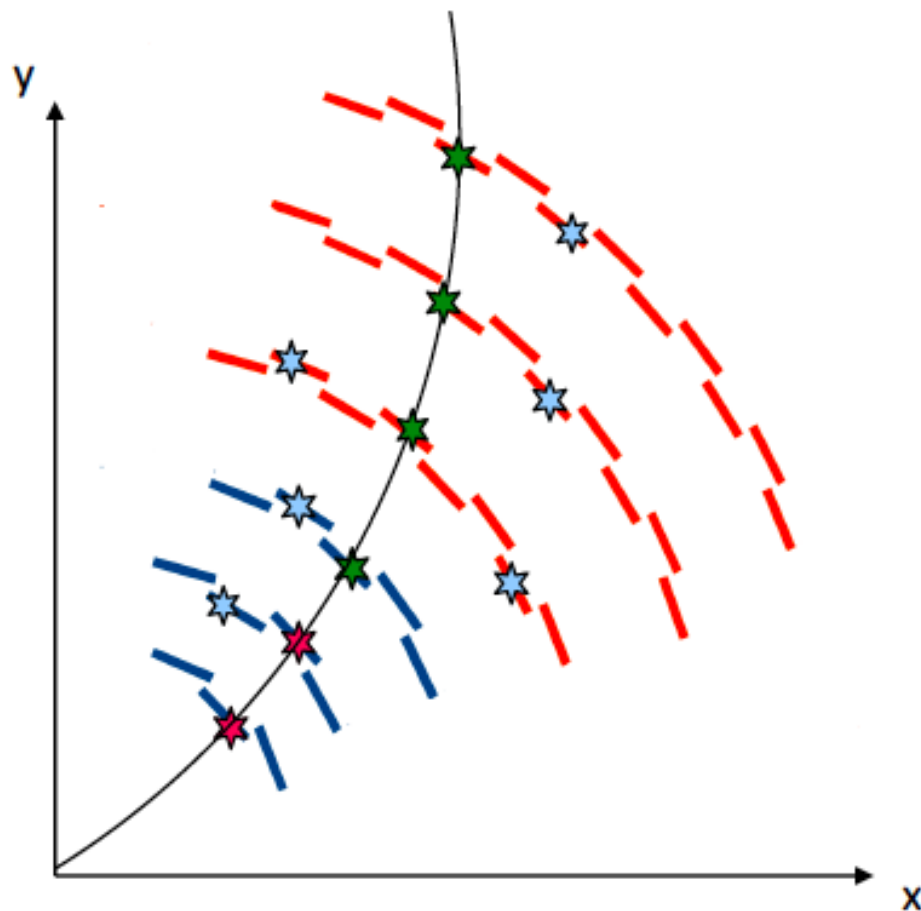
Important for projection stage!

Floating-point calculation  
Integer emulation



# Tracklet Based Track Finding

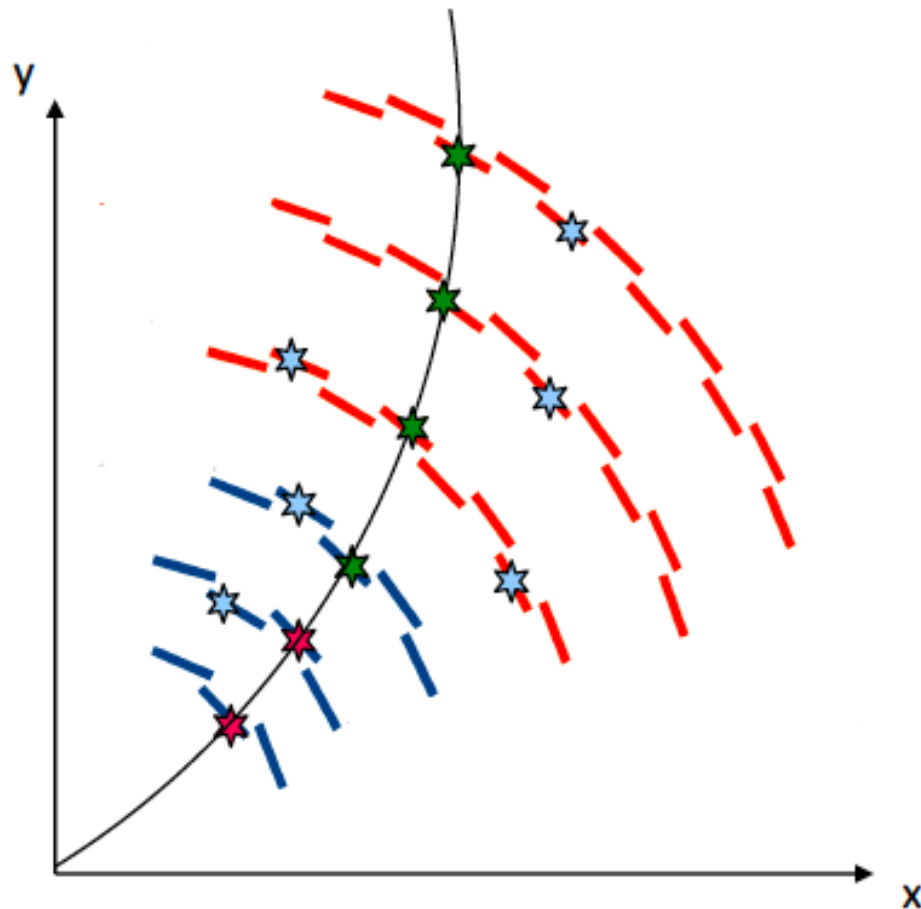
- Form track seeds, tracklets, from pairs of stubs in neighboring layers
- Match stubs on road defined by tracklet
- Fit the hits matched to the tracklet using a linearized  $\chi^2$  fit
  - Fit track if 2 or more matches stubs
  - Tracklet parameters good – linear fit works very well
  - Only fit – no hit filtering





# Tracklet Based Track Finding

- Form track seeds, tracklets, from pairs of stubs in neighboring layers
- Match stubs on road defined by tracklet
- Fit the hits matched to the tracklet using a linearized  $\chi^2$  fit
- Seeding is done in parallel in different layers
- Duplicate tracks are removed if they share 2 or more stubs



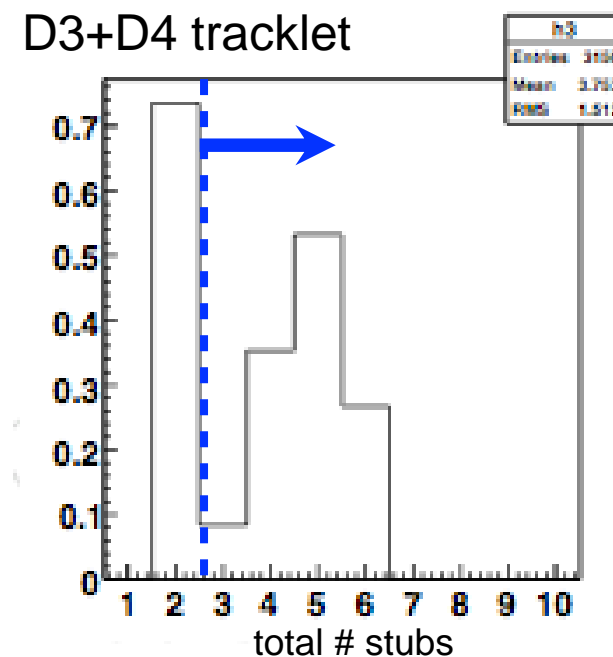
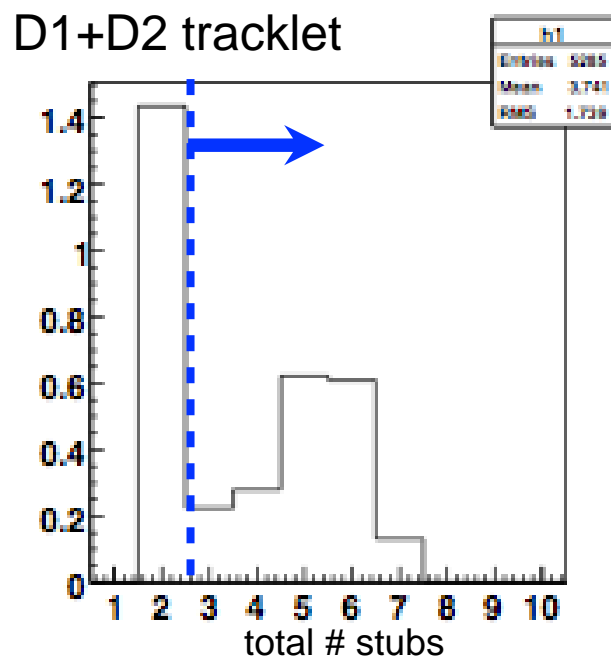
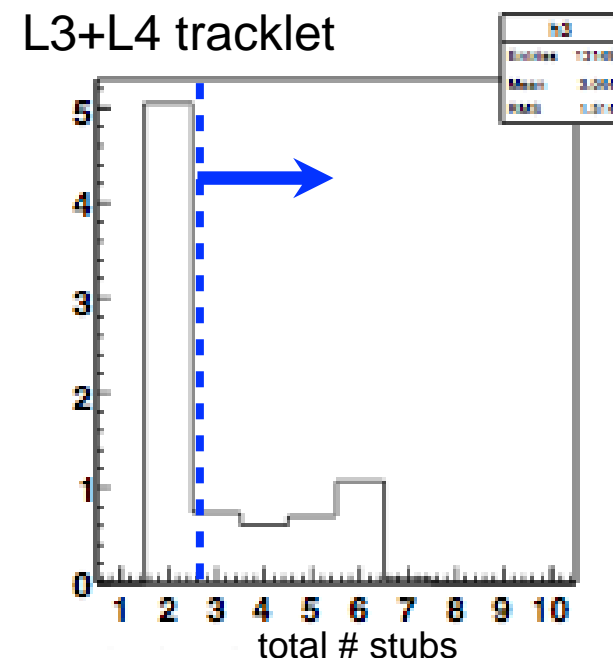
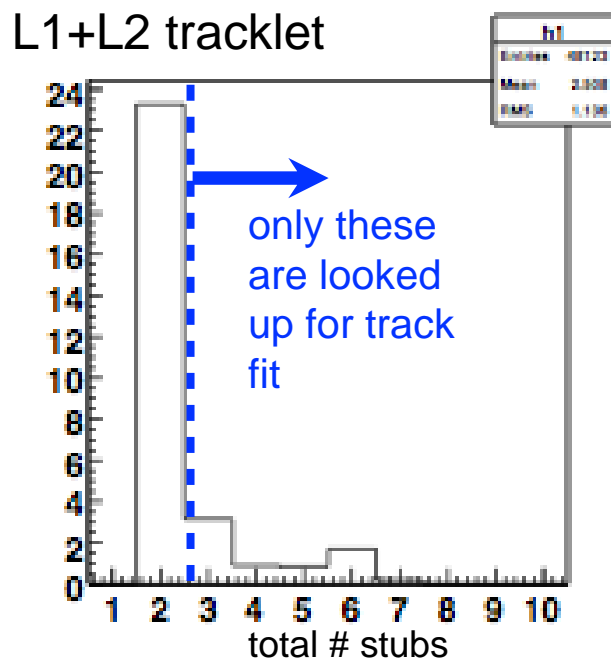
# Track fit & tracklet rejection

Track fit start from list of matches

- ▶ Tracklet +  $\geq 1$  matched stubs
- ▶ Fit improves tracklet parameters

Fake tracklets w/o any matches are therefore not looked at for fitting stage

Fake tracklets efficiently rejected!



# Tracklet formation (2)

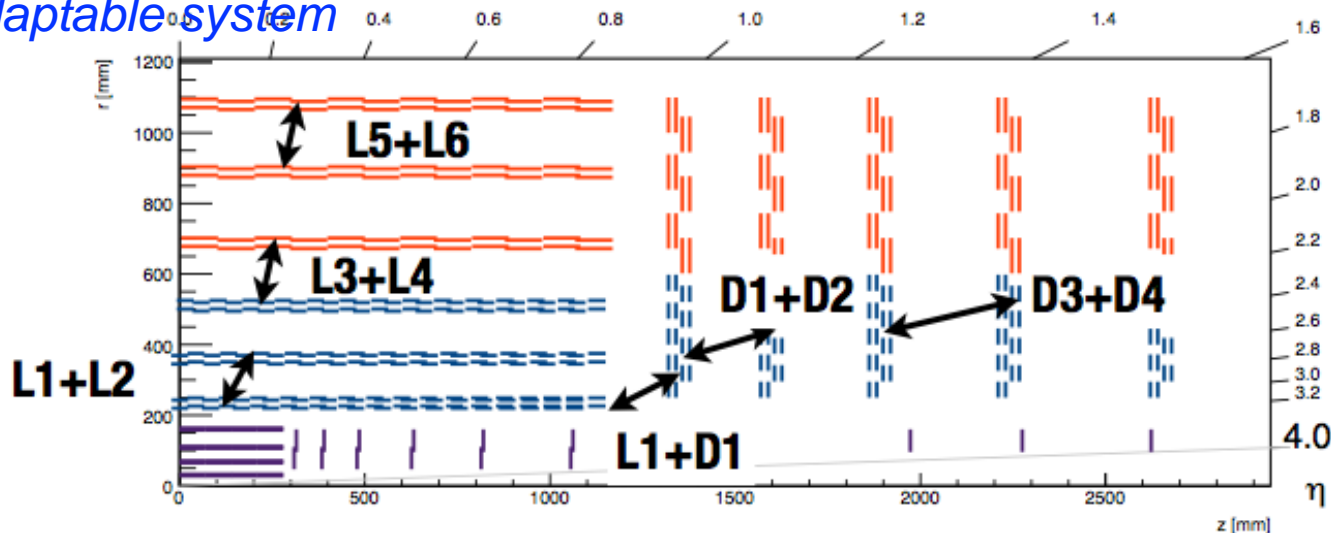
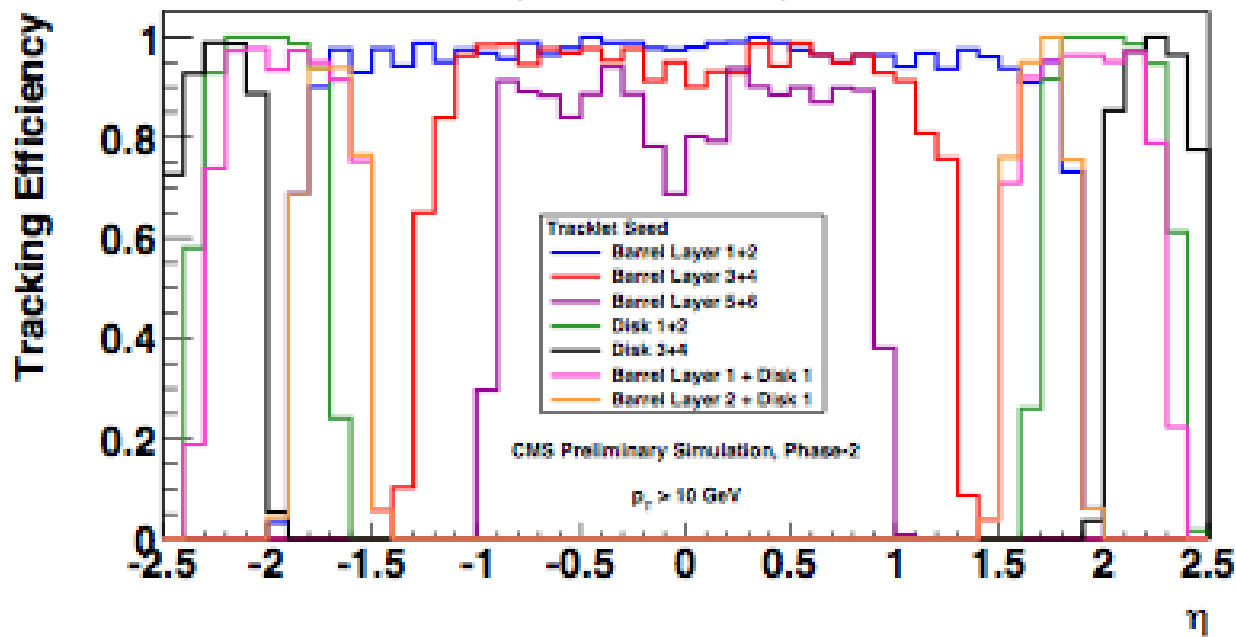
Seed multiple times in parallel to ensure good coverage & redundancy

Current configuration

- ▶ Barrel: L1+L2, L3+L4, L5+L6
- ▶ Disk: D1+D2, D3+D4
- ▶ Overlap: L1+D1

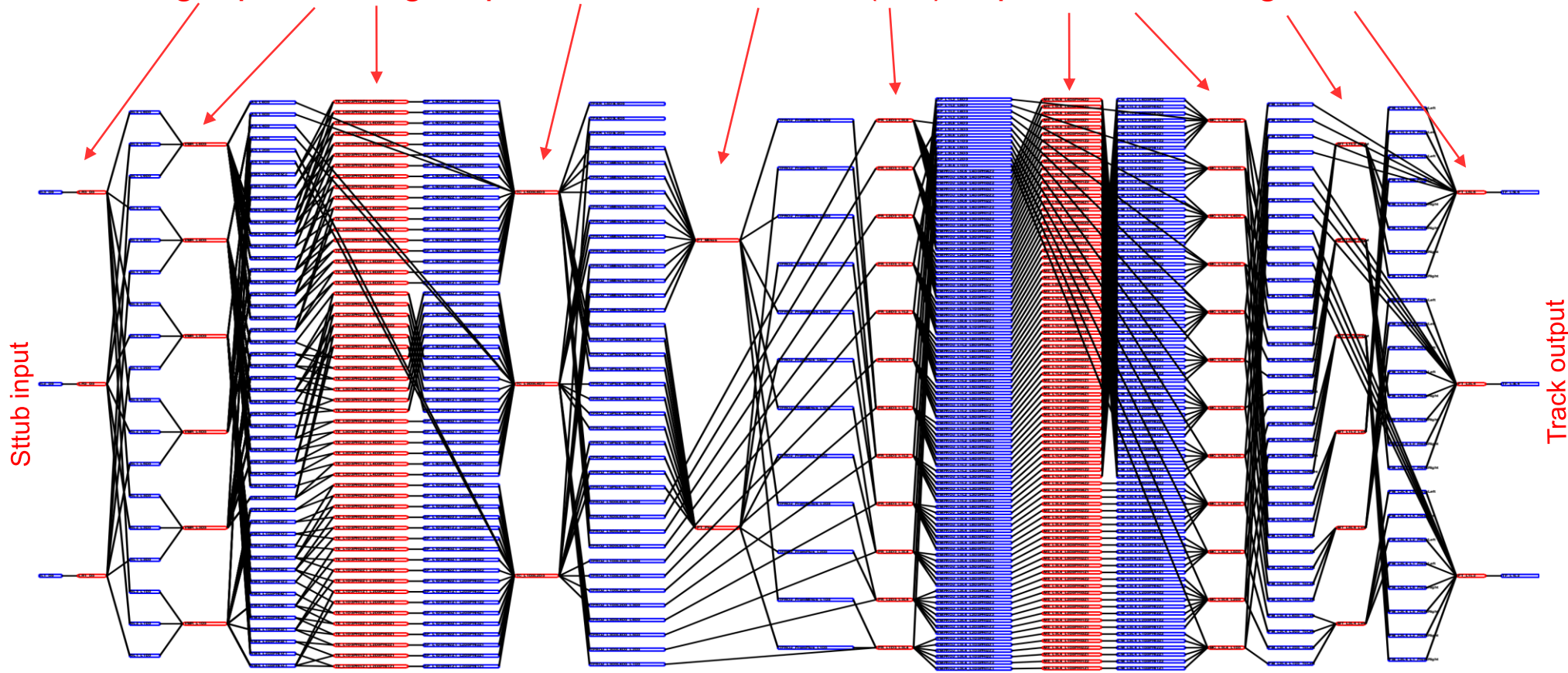
• *Adaptable system*

Efficiency for single muons (using firmware emulation)



# Firmware Implementation (1/4 of barrel)

Eight processing steps + two transmission (red) implements the algorithm



Stub organization		Forming tracklets		Projection transmission to neighbors	Organize tracklet projections	Match tracklet projections to stubs	Match transmission	Track fit
LayerRouter & VMRouter	TrackletEngine & TrackletCalculator	Projection-Transceiver	Projection-Router	MatchEngine & MatchCalculator	Match-Transceiver	Track-Fit		

# Tracklet Teststand

- Goal: Establish overall viability of tracklet approach.

- Firmware/Algorithm
- I/O Tests (input, neighbor, output)
- Latency
- Stress tests with data volumes

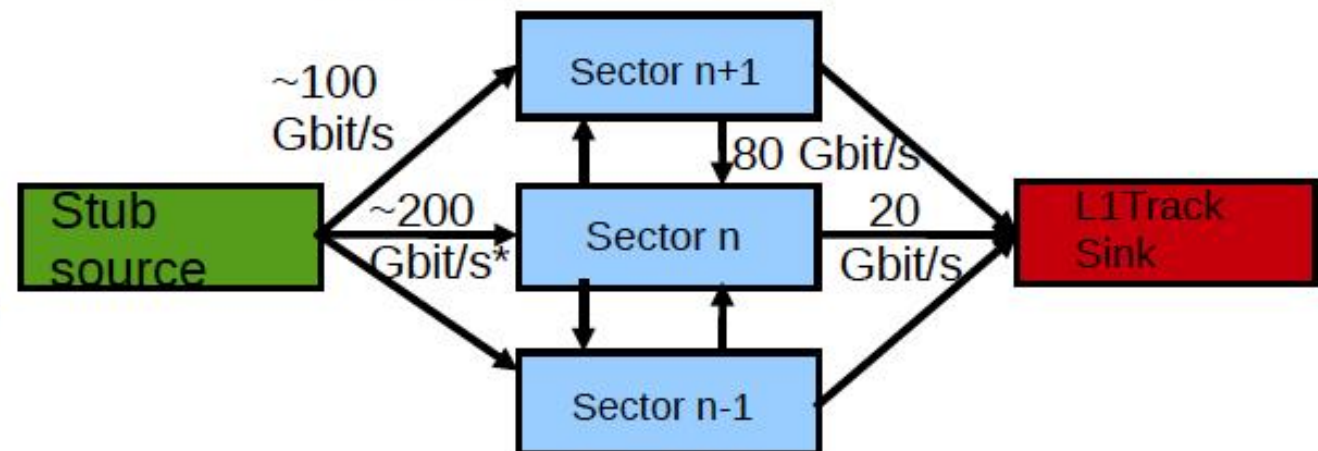
- Setup:

- Firmware/Algorithm
- I/O Tests (input, neighbor, output)
- Latency
- Stress tests est crate at CERN
- Four  $\mu$ TCA cards (CTP7)
  - 4th acting as data source/sink.
  - Each board has a Xilinx Vertex-7 FPGA and a Zynq chip.
  - Core sector board + 2 neighbors
- AMC13 card for clock dist.

Test crate at CERN



$\mu$ TCA boards (CTP7) developed by University of Wisconsin for the current 2016 Level-1 Trigger upgrade.



# Summary

- Since the concept for the upgraded CMS tracker started to form in 2008 to 2010 CMS has come a long way to proving all the concepts:
  - Many of the challenges in building the  $p_T$  modules has been solved, and prototype modules has proved the concept in test beams
  - The track trigger demonstrators has proved the feasibility to build a track trigger that meets the primary goals
- There are still many challenges and significant work needed to implement the track trigger
  - Trigger algorithm studies needs to better define the track trigger requirements; optimization in latency vs. threshold vs. efficiency vs. cost is a significant undertaking over the next few years
  - Build online and offline software system for track trigger
  - Building/Installing/Commissioning the hardware and algorithms

# Backup

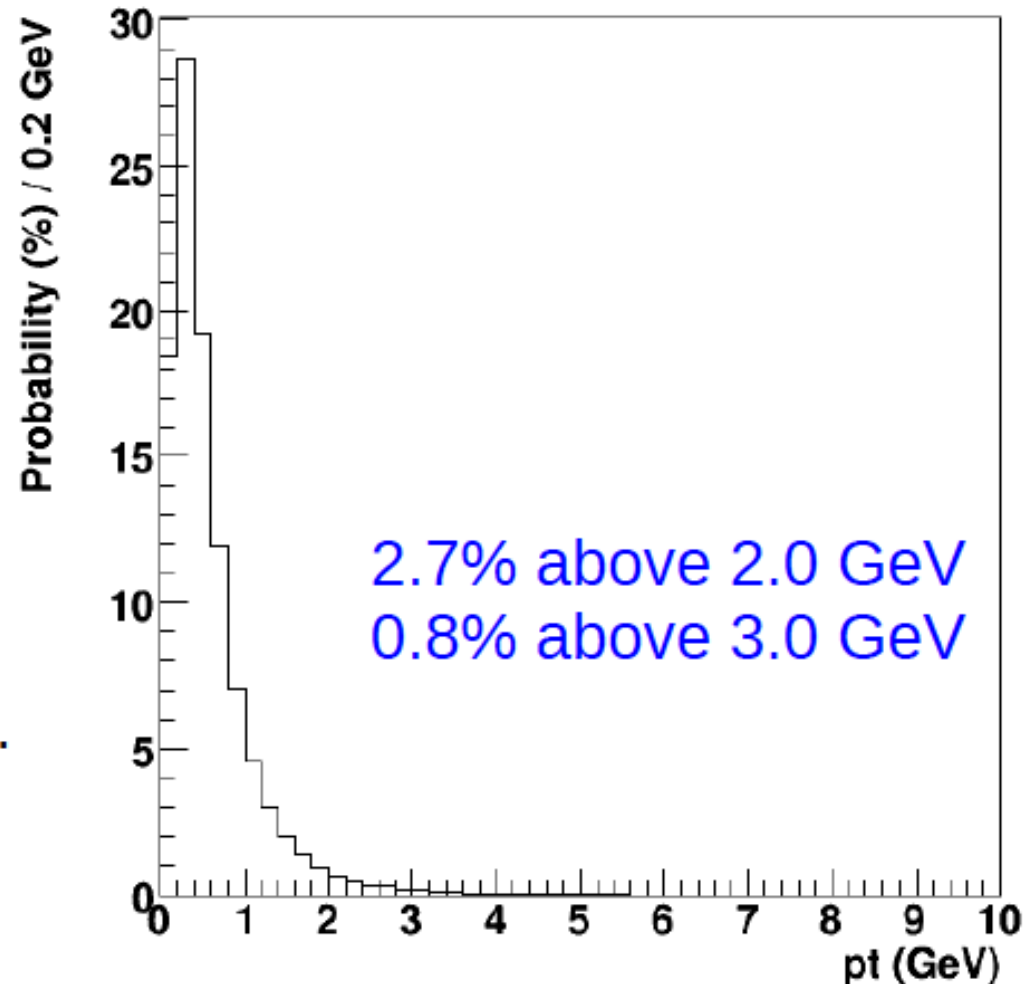
# Minbias Events

- **14 TeV minbias:**
  - ♦ 6.5 charged particles, mostly pions, per unit of rapidity or 33 charged particles in the tracking volume  $|\eta| < 2.5$
  - ♦ With 140 PU  $\rightarrow$  4600 charged particles per bunch crossing.
  - ♦ Soft spectrum – peaks at  $p_T$  of about 200 MeV.
- **The average min bias event has**  $33 \times 2.7\% = 0.89$  tracks with  $p_T > 2.0$ .
  - ♦ For PU=140 we expect  $\sim 125$  tracks with  $p_T > 2.0$ .

## Data volume:

- In 140 PU average of about 12,000 stubs/BX
- Each stub is  $\sim 36$  bits
  - ♦ At 40 MHz BX rate we have 17 Tbits/s

[  $p_T$  distribution in 14 TeV minbias



Only  $\sim 5\%$  of stubs are from tracks with  $p_T > 2\text{GeV}$