Thin planar pixel sensor productions at MPP for the ATLAS ITk

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Introduction

- Possible silicon surface to be covered in the ATLAS ITK pixel system ~ 11-14 m², depending on the final layout choice

- Planar pixel sensors possible candidate technology for all layers except innermost one

- Choice between 100 and 150 μm sensors still open for the different layers, depending on the radiation and cooling performance requirements

- MPP especially focusing on the development of 100 μm thin sensors in collaboration with CIS and MPG-HLL

- Different technologies investigated for the production of thin planar sensors
Thin planar pixel sensors with backside cavities

First production on 4\" wafers at CIS
- starting thickness 525\mum,
- target thicknesses 150/100\mum
- Anisotropic etching by KOH
- Two sets of dicing lines:
  - On the 420 \mum wide frame between the structures
  - Dicing along the sensor perimeter on the thinned substrate

FE-I4 compatible single chip sensors + FE-I4 quad sensors \rightarrow many test-beam results shown later
New production on 6” wafers at CIS

- New production on 6” wafers now started at CIS
- Local thinning to 100-150 µm thickness
- Collaboration MPP-LAL-LPNHE

NEW: RD53 compatible sensors with 50x50 and 25x100 µm$^2$ pitch
FE-I4 compatible sensors with small pitch columns
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**UBM processing at CIS**

Mask-based electroless Ni-UBM
- applied for CMS-Pixel production, in combination with In-bumps
- relatively thin film on sensor surface
- Now employed with AgSn bumps at IZM

Mask-based electroless Pt-UBM
- First experience at CIS
- Some deposition steps are outsourced

- Single chip and quad sensors with Ni and Pt UBM have been flip-chipped at IZM

Ni UBM for quad FE-I4 module with 150 µm thickness: good interconnection efficiency

100 µm thin sensor with Pt UBM

Hit map of test-beam at CERN SPS

No need of support wafer during the sensor wafer production and post-processing
For some sensor production technology (backside cavities, active edge sensors) the deposition of BCB isolation layer on the sensors is problematic or impossible.

A possible solution is to have the BCB isolation deposited on the chip side, first 4 FE-I4 wafers with BCB processed at IZM (LPNHE and MPP project).

This approach would also allow for cost-reduction thanks to the larger size of chip wafers compared with sensor wafers → more structures processed in a single step.

Sensor coated with BCB have shown HV capabilities after interconnection up to 900-1000V.
- Two different implementations on a single wafer:
  - BCB only on the chip edges where the chip faces the not active area of the sensor at HV potential
  - BCB everywhere except on the bumps → option now disfavored by IZM

- Further tests foreseen with BCB deposited on a daisy chain run on 12” wafers again at IZM in preparation for the RD53A processing
BCB isolation on chips

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HLL SOI3 sensor 100 um thick
• CIS4 sensor 150 µm thick
  irradiated at $\Phi = 10^{16}$ n$_{eq}$/cm$^2$
  at CERN-PS
• $V_{bias} = 900$V
• Itk test-beam October 2016
  at CERN SPS

Hit efficiency saturation between 700 and 900V at a fluence of $10^{16}$ n$_{eq}$/cm$^2$
Hit efficiencies in different eta ranges

- CIS4 sensor 150 mm thick irradiated at $\Phi=10^{16} \text{n}_{\text{eq}}/\text{cm}^2$, $V_{\text{bias}}=900\text{V}$
- Itk test-beam October 2016 at CERN SPS

Hit efficiency improves already at moderate eta: effect of biasing structures is decreased

To be confirmed with 50x50 $\mu\text{m}^2$ cell pixels
Comparison of hit efficiencies for 100 and 150 µm thick sensors

- Comparison of hit efficiencies after an irradiation to $1 \times 10^{16}$ $n_{eq}$/cm$^2$ shows an earlier hit efficiency saturation for the module with 100 µm thick sensor compared to the CIS module with a 150 µm thick sensor.

- Lower operation bias voltages at high fluence results in lower power dissipation and help to relax the requirements on the cooling system.
Charge sharing effect for a $50 \times 50 \, \mu\text{m}^2$ pixel (I)

- Sensor implemented in the CIS4 production
- Layout with $50 \times 50 \, \mu\text{m}^2$ implants
- Neighbouring pixel implants are read out by different read-out channels to reproduce the effect of charge sharing in $50 \times 50 \, \mu\text{m}^2$ pixel cells and still be compatible with FE-I4 chips.

- RD53 compatible sensors implemented in the new CIS 6” production
Charge sharing effect for a 50x50 $\mu m^2$ pixel (II)

- CIS4 sensor 150 $\mu m$ thick irradiated at $\Phi=3\times10^{15}$ $n_{eq}/cm^2$ in Birmingham
- $V_{bias}=300V$
- Itk test-beam October 2016 at CERN SPS

Charge sharing effects between neighbouring implants seen at low voltages in charge and hit efficiencies maps.
Estimation of the hit efficiency for a 50x50 µm² pixel

- Increasing the bias voltage to 500V the loss of efficiency due to charge sharing is less relevant
- In-pixel efficiency of the 50x50 µm² implant (implant at the edge) is the closest approximation of the possible performance of a planar pixel cell RD53 compatible without any biasing structure

98.2 ± 0.3 % at 500V

Same kind of modules now being irradiated to higher fluences in Birmingham
SOI productions at MPG-HLL

- High resistivity SOI 6” wafers
  - 6 wafers 100 \( \mu \text{m} \) thick
  - 4 wafers 150 \( \mu \text{m} \) thick
- Post-processing at IZM completed and sensor delivered to MPP for measurement
- BCB and UBM processing
- Complete etching of the handle wafer + Aluminum on backside

IV curves of RD53 compatible sensors

- 25x100 \( \mu \text{m}^2 \) cell
- 50 x 50 \( \mu \text{m}^2 \) cell
- 25 x 100 \( \mu \text{m}^2 \) cell
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100 µm thin RD53A sensor with UBM

First IV curve after post-processing agrees with measurements at wafer scale
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SOI3 production - FEI4 Quads

- Measurements performed after post-processing and dicing
- Process yield very satisfactory

Flip-chipping at IZM to prove interconnection yield also for 100 µm quads with higher statistics
SOI4 production at MPG-HLL

- New production of 9 wafers started with similar technology of SOI3 at MPG-HLL:
  - 100 and 150 µm active thickness
  - BCB, UBM processing + thinning planned to be performed at HLL.
  - Cu used as UBM, compatible with the SnAg IZM bumps
New RD53 designs in SOI4

- Common PT implant with smaller dimensions with respect to previous implementations (implant diameter from 18 to 10 µm)

- Developing ideas how to contact the pixels without PT for testing before flip-chipping

- Double chip RD53A sensor (prototype for the inner layer or the inclined sections):
  - Two different implementations of pixels in the inter-chip area
Some sensors without bumps on BR:

- Investigate if it is possible to reduce the effect of PT on hit efficiency after irradiation leaving the BR floating
- Drawback: currents from the edges will flow directly into edge columns

Second bias ring design: decouple the testing functionality before interconnection from the grounding after flip-chipping

- Bias rails are all linked to a metal line not connected through contacts to the implant
- bumps on BR are in contact to the BR implant
Conclusions and Outlook

- Feasibility of producing thin quad sensors with good yield (100 and 150 μm thickness) demonstrated at CIS and HLL
- UBM at the sensor vendors under development with different technologies
- RD53 sensor design improved following the results of the test-beam analysis on FE-I4 sensors, several variants included in the ongoing productions
- Starting to think about possible methods of implementing testing of sensors without PT
Additional slides
FE-I4 sensors in CIS 6” wafers and SOI4 production

- FE-I4 quad with common PT and 3 ganged rows each chip \( \Rightarrow \) 180 \( \mu \)m distance between physical edges of the chips
- 400 \( \mu \)m long pixels per side

- Quad with standard PT and 4 ganged rows \( \Rightarrow \) 280 \( \mu \)m distance between chips
- 450 \( \mu \)m long pixels per side

- FE-I4 compatible sensors with half the cells of 50x50 \( \mu \)m\(^2\) pitch and no biasing structures
- Especially important to study post-irradiation performance of small cell sizes while waiting for the RD53A chip
Thin sensors performance at high fluences

- 100 μm thin sensors yield the best hit eff. at 5x10^{15} \text{n}_{eq}/\text{cm}^2
- VTT FE-I4 module with 100 μm thin sensor irradiated at JSI at 1x10^{16} \text{n}_{eq}/\text{cm}^2
- Tested at DESY with 5 GeV electrons, threshold tuning to 1300 e

- significantly lower efficiencies at 200 and 300 V at \Phi=1x10^{16} \text{n}_{eq}/\text{cm}^2
- efficiencies at different fluences have similar saturation values (~97%)

U= 500 V

\[ 97.3 \pm 0.3 \% \]
Power dissipation for thin planar sensors at high fluences

IV curve of bare FE-I4 sensor at -25°C irradiated to $1 \times 10^{16}$ n$_{eq}$/cm$^2$ after 11 days of annealing, as measured in direct thermal contact in a probe-station.

Estimated power dissipation per cm$^2$ at -25°C for a 100 µm thin sensor irradiated to $1 \times 10^{16}$ n$_{eq}$/cm$^2$.

- The possible range of operation bias voltage for a pixel module with a 100 µm thick sensor is 500-700 V.
- The resulting power dissipation at 500-700 V is ~25-50 mW/cm$^2$ at $1 \times 10^{16}$ n$_{eq}$/cm$^2$ irradiation.
**ADVACAM: 50 µm thick sensors**

- Active edge sensors produced on SOI wafers at ADVACAM

- Modules with 50 µm thin sensors and Cu-Au UBM show a perfect interconnection efficiency

- Collected charge by $^{90}$Sr scans agrees with expectations for the three thickness

- 50 µm thin sensors needs a special tuning to very low thresholds ≤ 1000 e
Hit efficiencies for active edge devices

- August + October test-beam at CERN: systematic comparison of different sensor thicknesses

- New measurements with 50 µm thin sensors at lower threshold then presented before (600 e- nominal instead of 800 e-)

- Higher efficiency on pixel implant with lower threshold (~98.8%) but still worse edge eff. with respect to thicker sensors

- Very good performance up to the edge of 100-150 µm thick sensors