Thin planar pixel sensor productions at MPP for the ATLAS ITk

A. Macchiolo

J. Beyer, A. La Rosa, K. Oswald, R. Nisius, L. Renkl, N. Savic

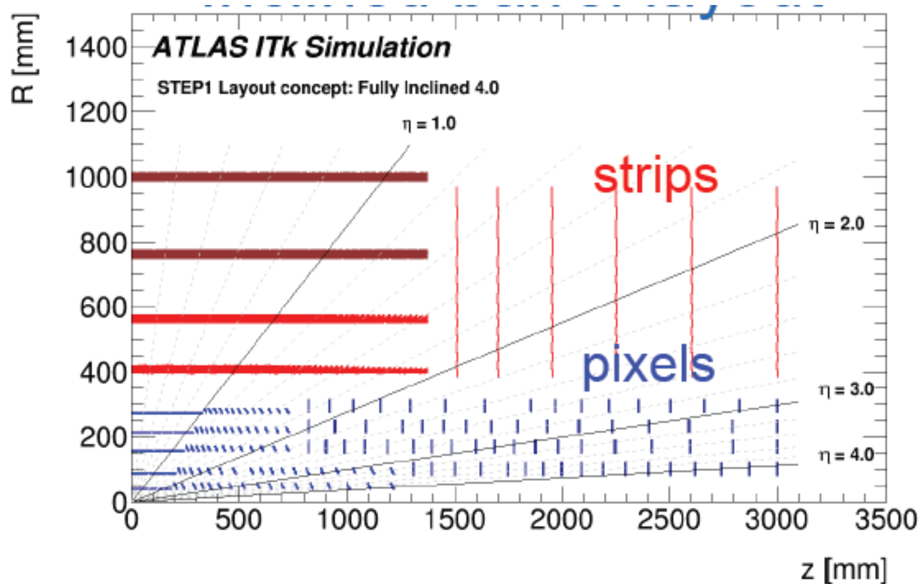
Max-Planck-Institut für Physik, Munich

12th Trento Workshop on Advanced Silicon Radiation Detectors, 20-22 February 2017

Introduction

- Possible silicon surface to be covered in the ATLAS ITK pixel system ~ 11-14 m^2, depending on the final layout choice

- Planar pixel sensors possible candidate technology for all layers except innermost one



- Choice between 100 and 150 μm sensors still open for the different layers, depending on the radiation and cooling performance requirements

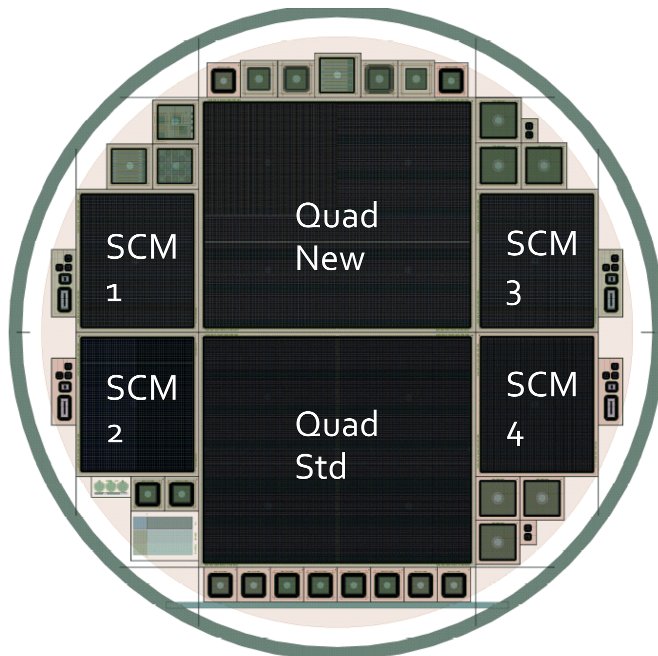
- MPP especially focusing on the development of 100 μm thin sensors in collaboration with CIS and MPG-HLL

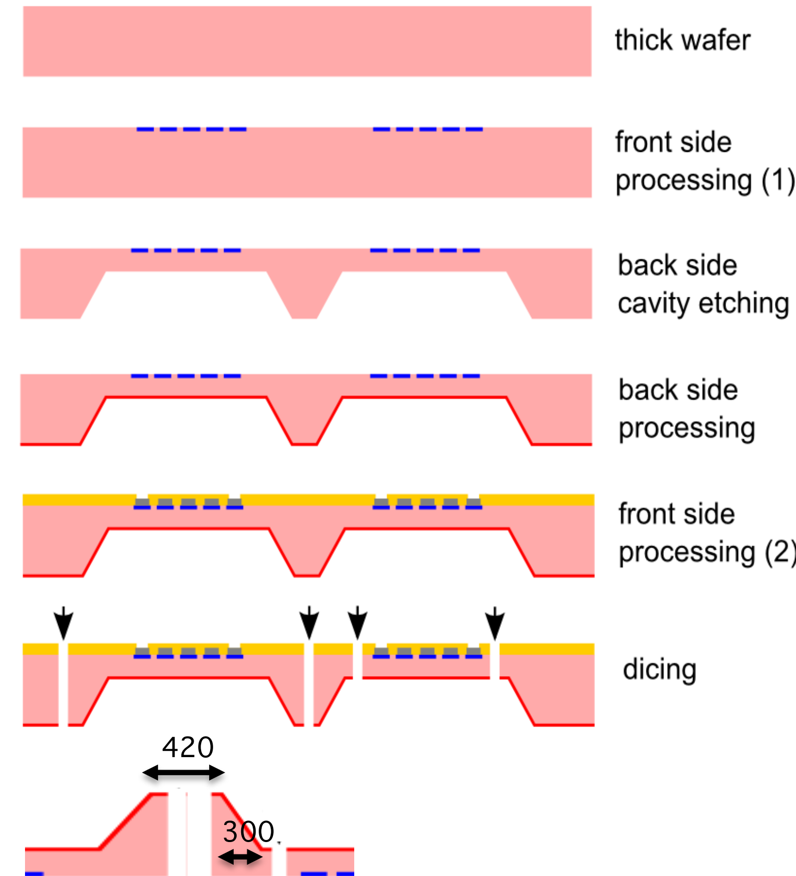
- Different technologies investigated for the production of thin planar sensors

Thin planar pixel sensors with backside cavities

First production on 4" wafers at CIS

- starting thickness 525µm,
- target thicknesses 150/100µm
- Anisotropic etching by KOH
- Two sets of dicing lines:
  - On the 420 µm wide frame between the structures
  - Dicing along the sensor perimeter on the thinned substrate



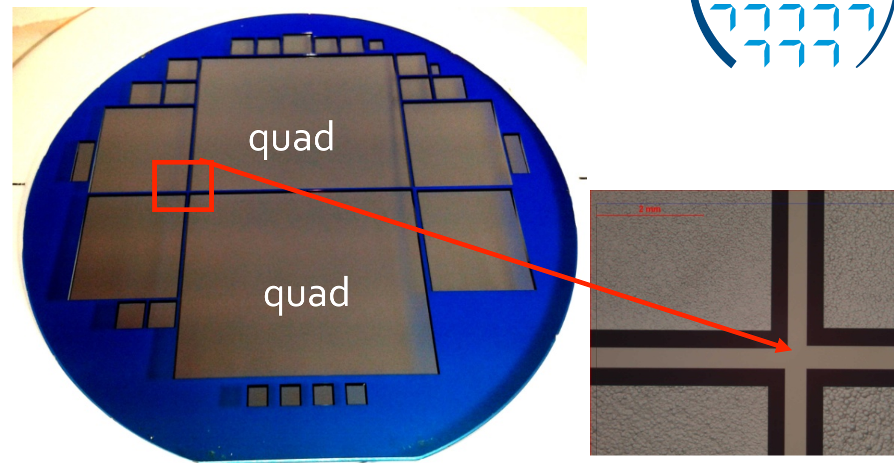


FE-I4 compatible single chip sensors + FE-I4 quad sensors → many test-beam results shown later

New production on 6" wafers at CIS

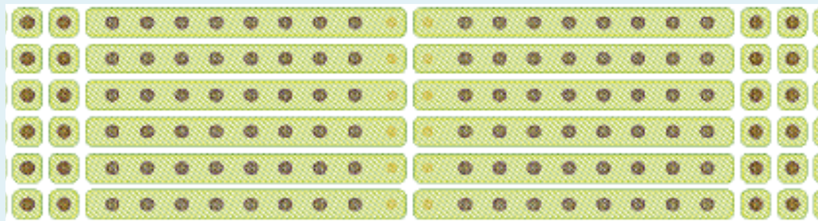
- New production on 6" wafers now started at CIS
- Local thinning to 100-150 μm thickness

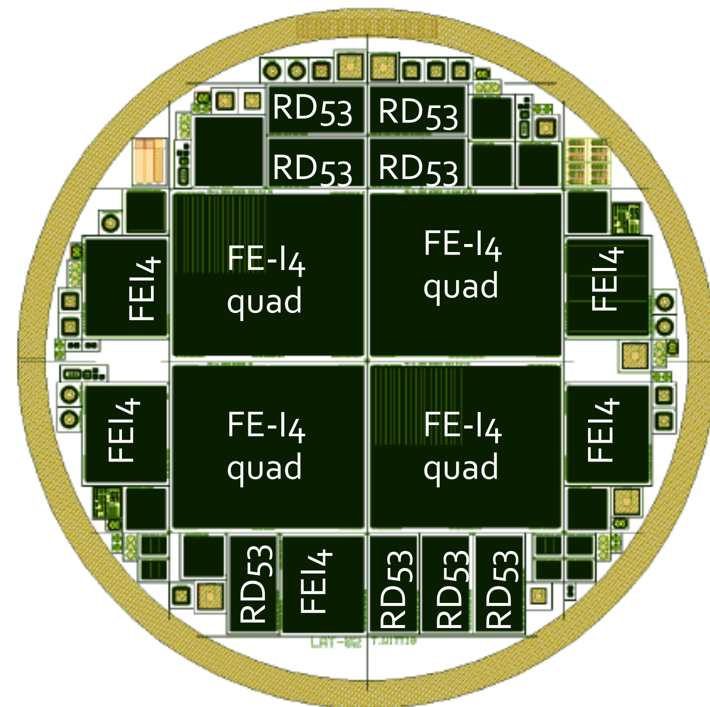
- Collaboration MPP-LAL-LPNHE



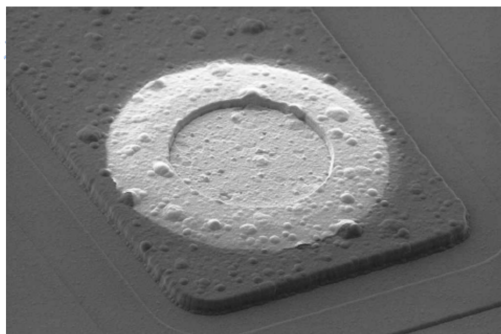
NEW: RD53 compatible sensors with 50x50 and 25x100 μm^2 pitch

FE-I4 compatible sensors with small pitch columns





UBM processing at CIS



Nickel UBM

Mask-based electroless Ni-UBM

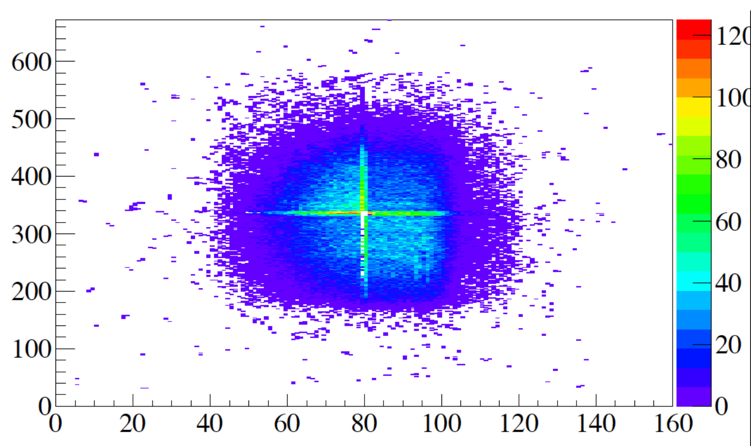
- applied for CMS-Pixel production, in combination with In-bumps
- relatively thin film on sensor surface
- Now employed with AgSn bumps at IZM

Mask-based electroless Pt-UBM

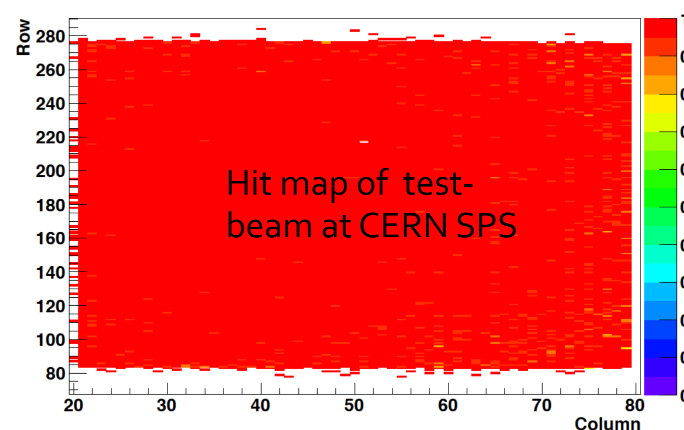
- First experience at CIS
- Some deposition steps are outsourced

- Single chip and quad sensors with Ni and Pt UBM have been flip-chipped at IZM

Ni UBM for quad FE-I4 module with 150 um thickness: good interconnection efficiency



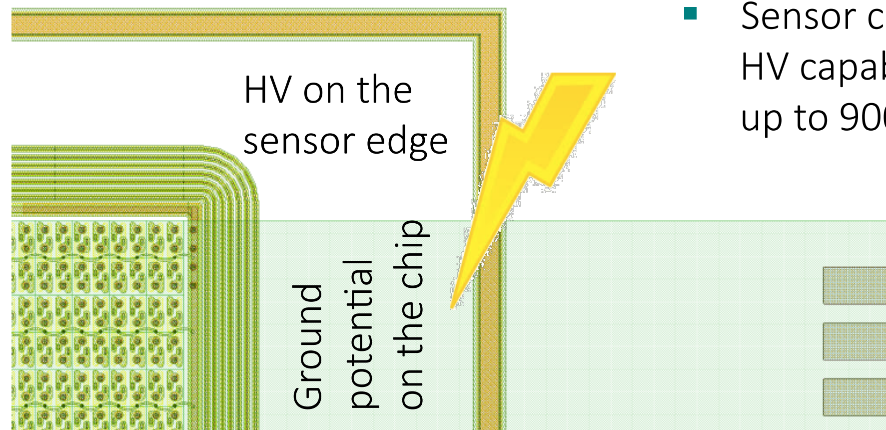
100 μm thin sensor with Pt UBM



No need of support wafer during the sensor wafer production and post-processing

BCB isolation on chips

Fraunhofer IZM



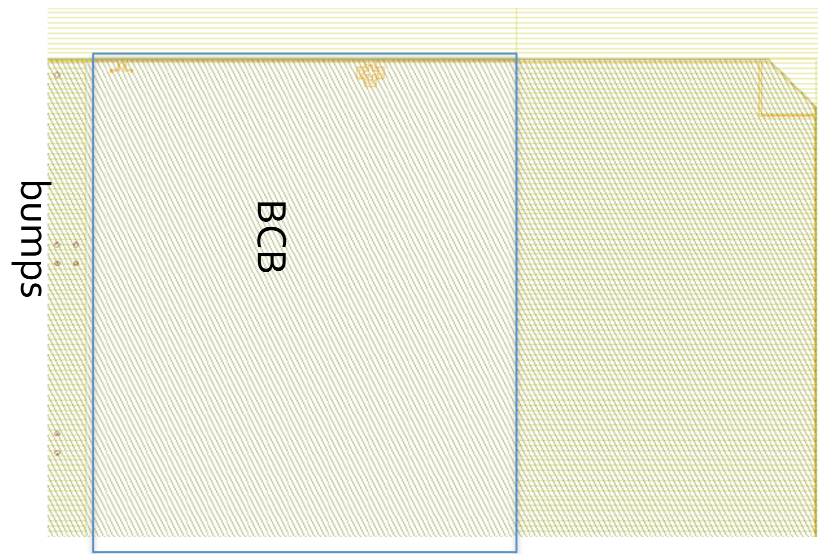
- Sensor coated with BCB have shown HV capabilities after interconnection up to 900-1000V

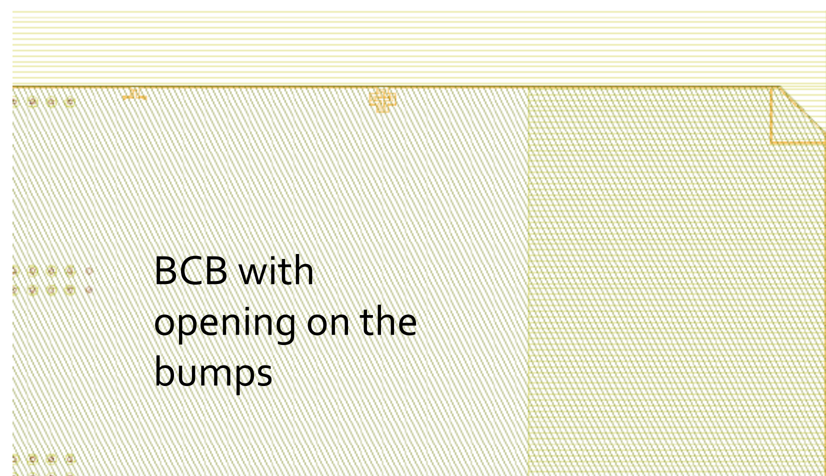
- For some sensor production technology (backside cavities, active edge sensors) the deposition of BCB isolation layer on the sensors is problematic or impossible
- A possible solution is to have the BCB isolation deposited on the chip side, first 4 FE-I4 wafers with BCB processed at IZM (LPNHE and MPP project)
- This approach would also allow for cost-reduction thanks to the larger size of chip wafers compared with sensor wafers → more structures processed in a single step

BCB isolation on chips

Fraunhofer IZM

- Two different implementations on a single wafer:
  - BCB only on the chip edges where the chip faces the not active area of the sensor at HV potential
  - BCB everywhere except on the bumps → option now disfavored by IZM



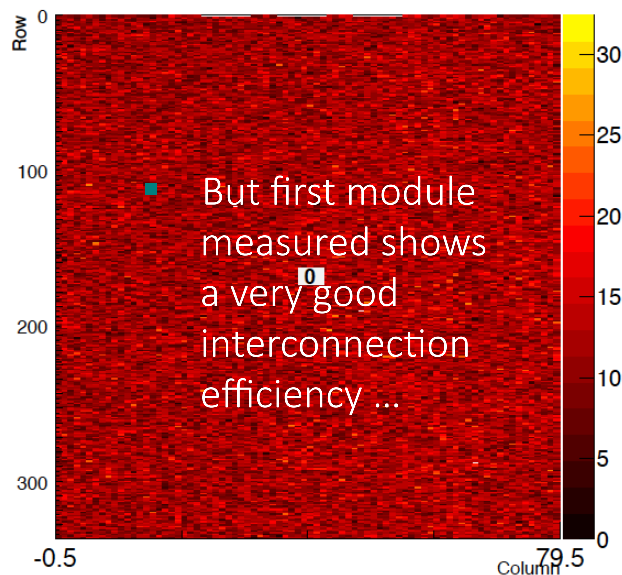


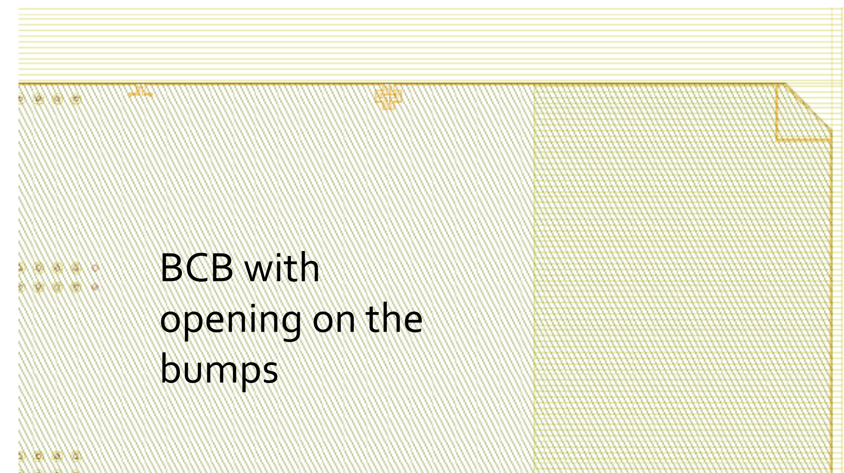
- Further tests foreseen with BCB deposited on a daisy chain run on 12” wafers again at IZM in preparation for the RD53A processing

BCB isolation on chips

Fraunhofer IZM

- Two different implementations on a single wafer:
  - BCB only on the chip edges where the chip faces the not active area of the sensor at HV potential
  - BCB everywhere except on the bumps → option now disfavored by IZM

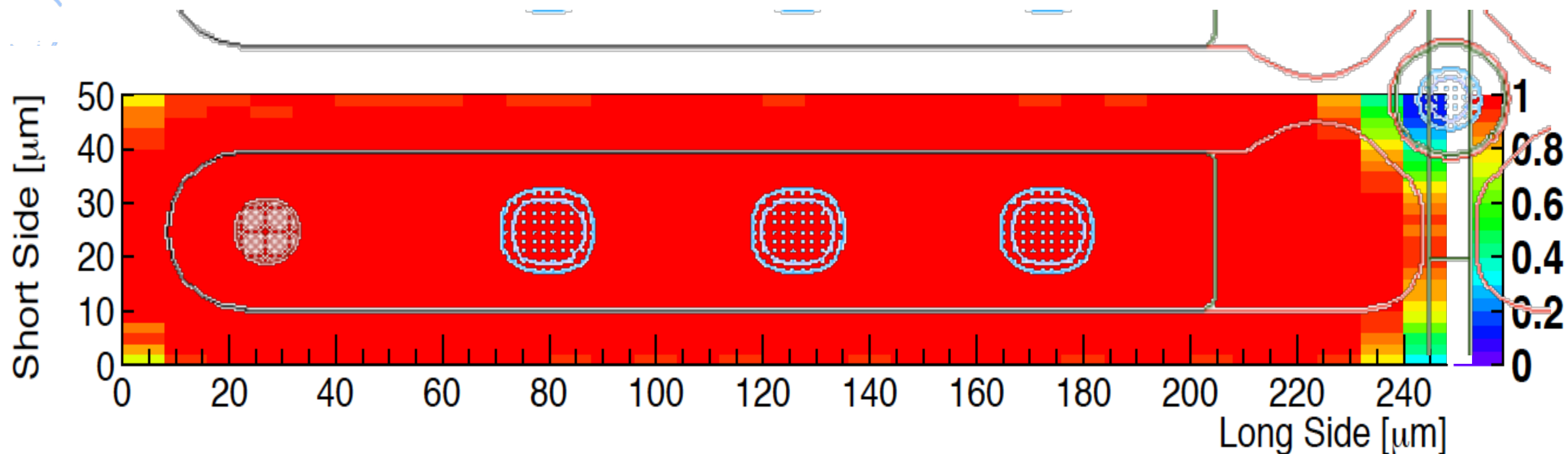




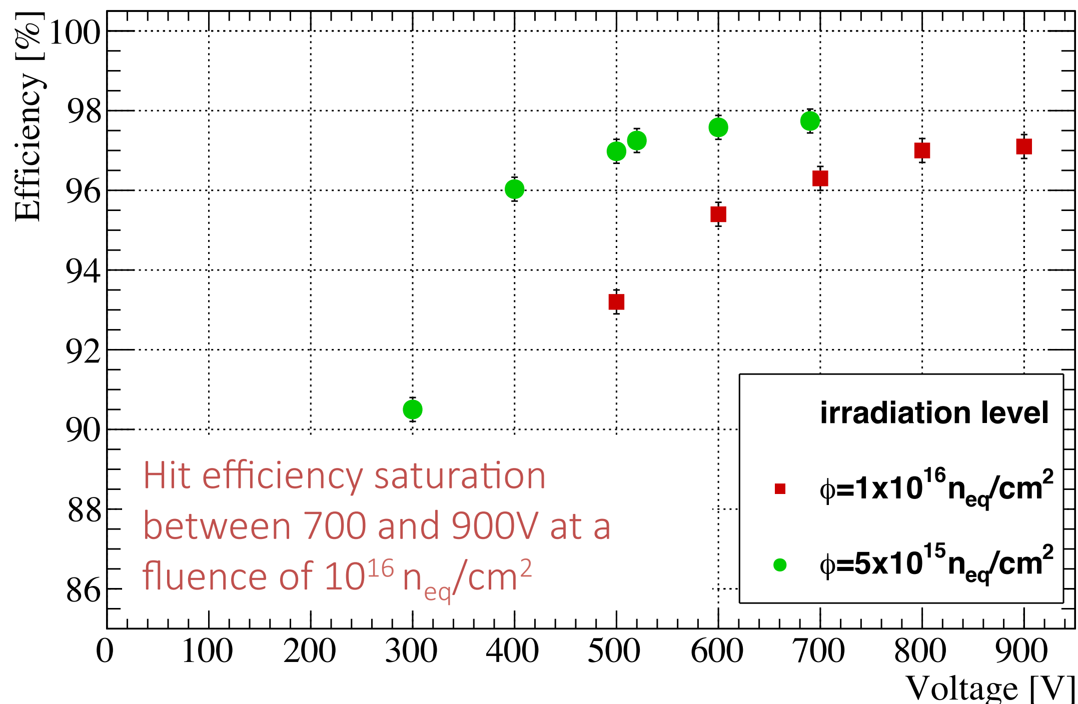
HLL SOI3 sensor 100 um thick

- Further tests foreseen with BCB deposited on a daisy chain run on 12" wafers again at IZM in preparation for the RD53A processing

Study of the hit efficiency for 150 μm thick sensors

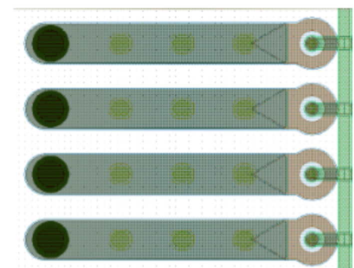


- CIS4 sensor 150 μm thick irradiated at $\Phi=10^{16}\ n_{eq}/cm^2$ at CERN-PS
- Vbias=900V
- Itk test-beam October 2016 at CERN SPS

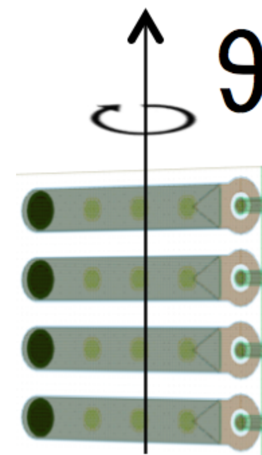


Hit efficiencies in different eta ranges

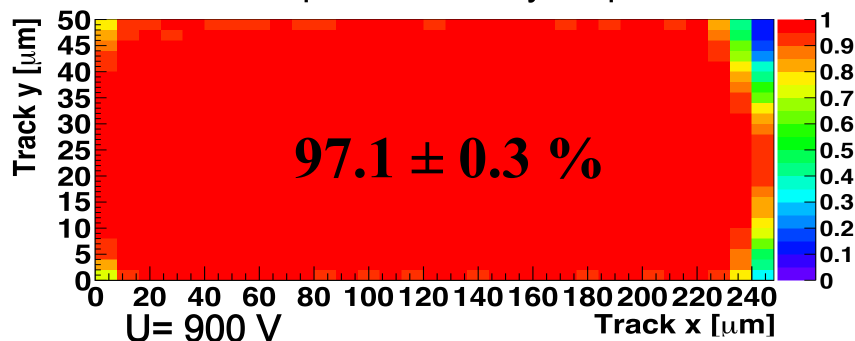
- CIS4 sensor 150 mm thick irradiated at $\Phi=10^{16}\ n_{eq}/cm^2$, Vbias=900V
- Itk test-beam October 2016 at CERN SPS

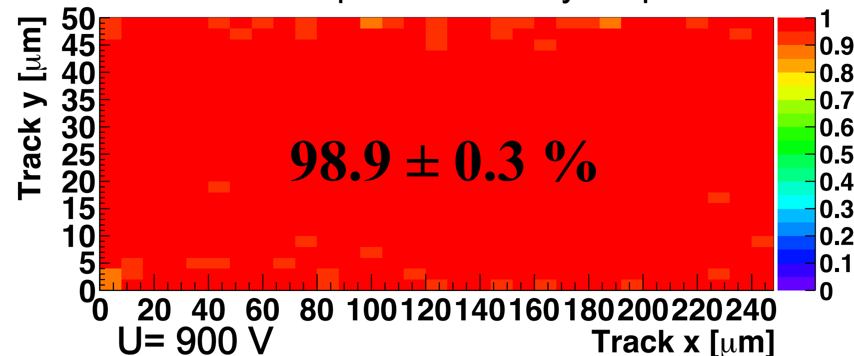


0°



45°



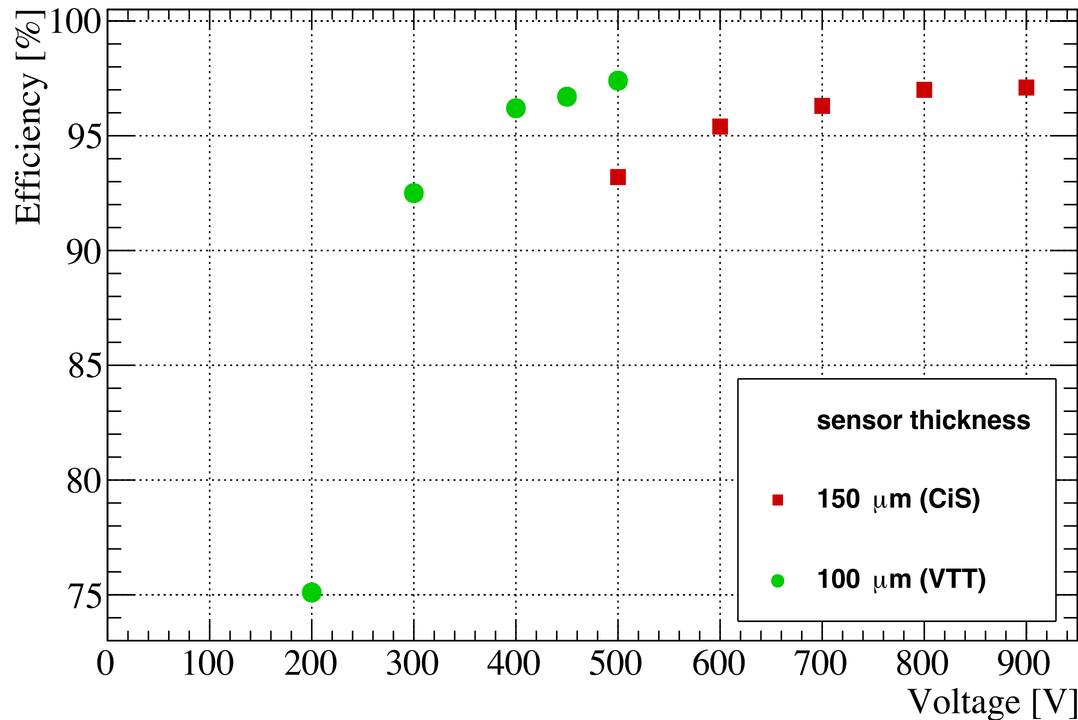


Hit efficiency improves already at moderate eta: effect of biasing structures is decreased

To be confirmed with 50x50 μm^2 cell pixels

Comparison of hit efficiencies for 100 and 150 µm thick sensors

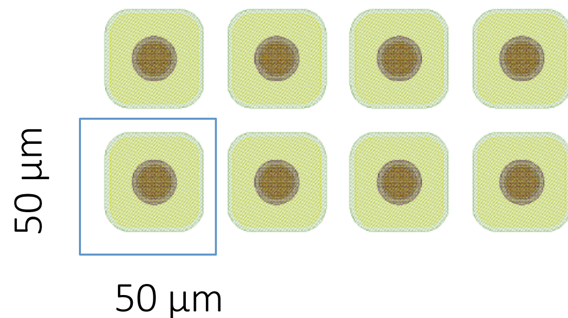
- Comparison of hit efficiencies after an irradiation to $1x10^{16}$ n_{eq}/cm^2 shows an earlier hit efficiency saturation for the module with 100 µm thick sensor compared to the CIS module with a 150 µm thick sensor.

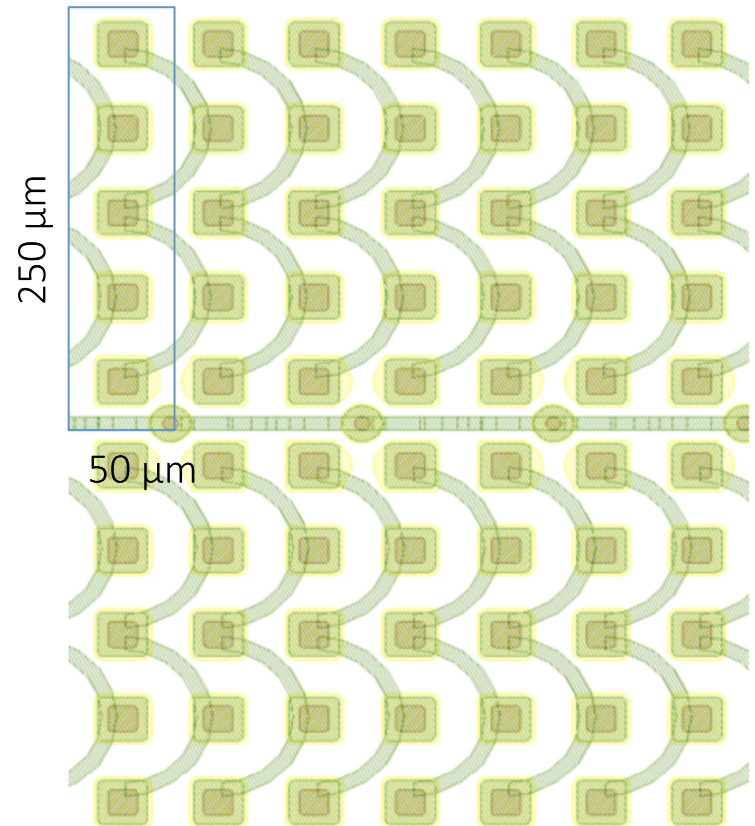


- Lower operation bias voltages at high fluence results in lower power dissipation and help to relax the requirements on the cooling system

Charge sharing effect for a 50x50 μm² pixel (I)

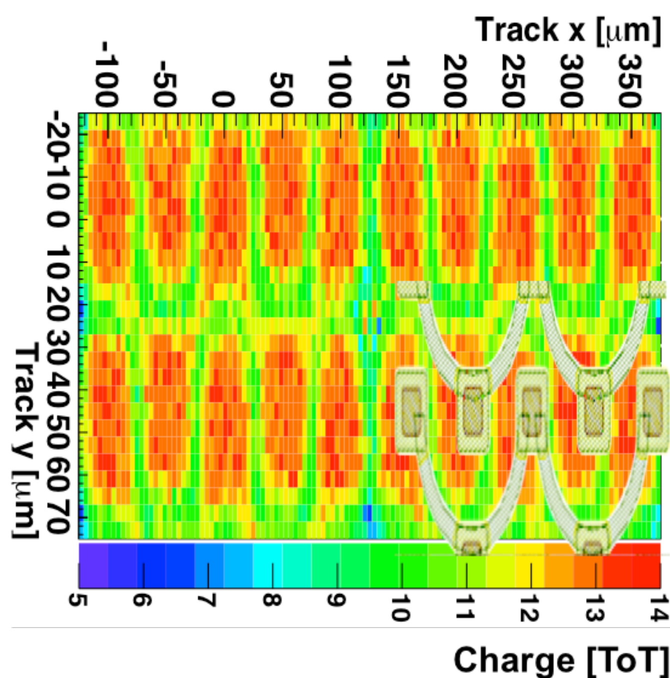
- Sensor implemented in the CIS4 production
- Layout with 50x50 μm^2 implants
- Neighbouring pixel implants are read out by different read-out channels to reproduce the effect of charge sharing in 50x50 μm^2 pixel cells and still be compatible with FE-I4 chips.





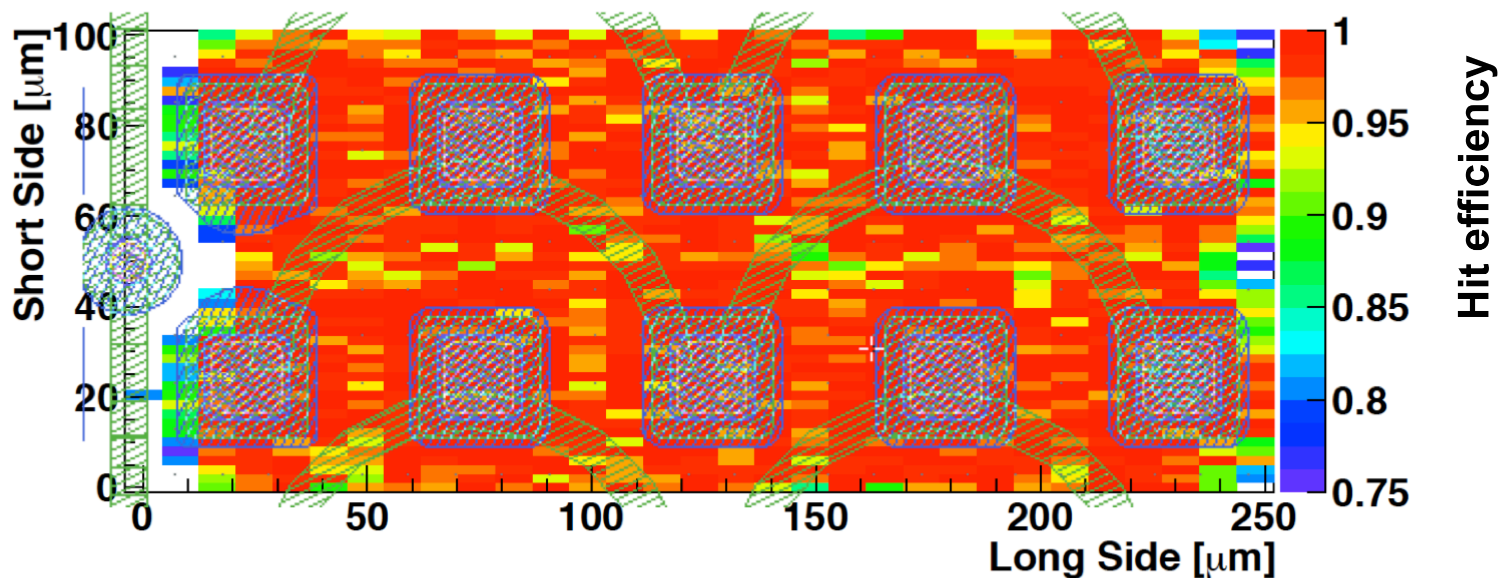
- RD53 compatible sensors implemented in the new CIS 6“ production

Charge sharing effect for a 50x50 μm² pixel (II)

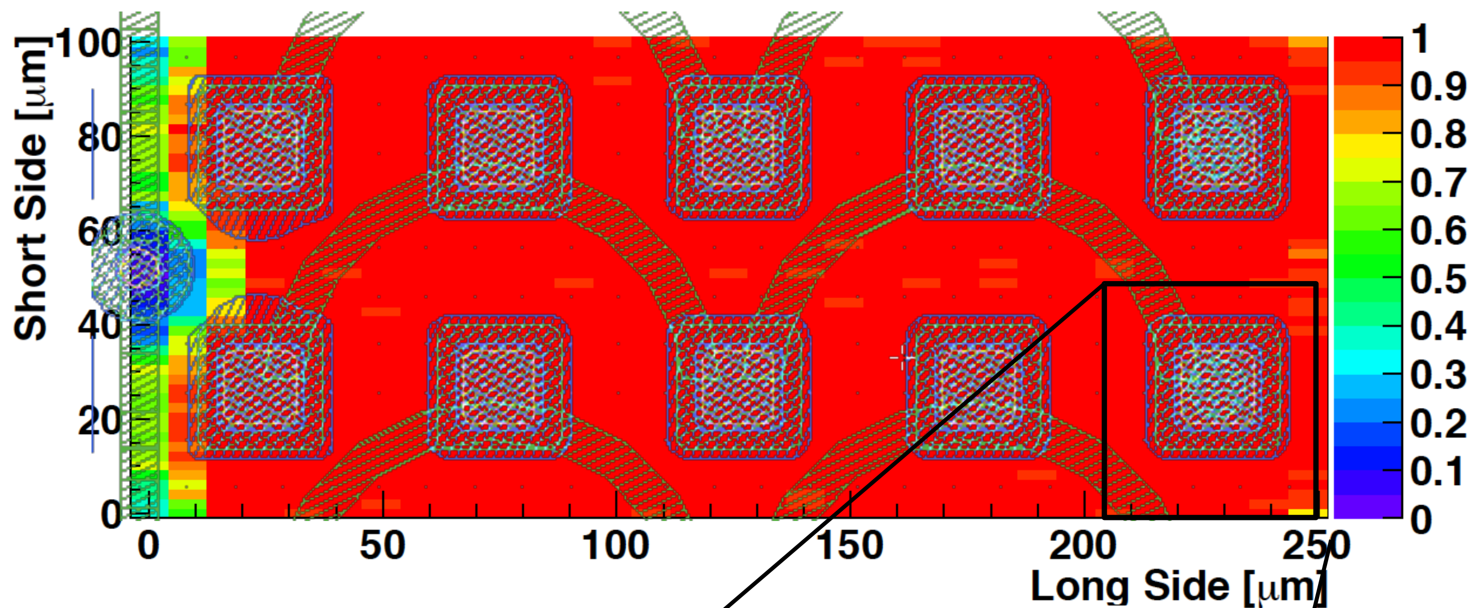


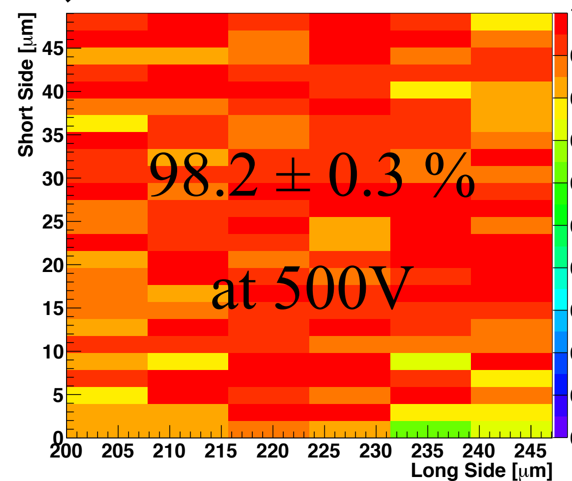
- CIS4 sensor 150 μm thick irradiated at Φ=3x10^{15} n_{eq}/cm^2 in Birmingham
- Vbias=300V
- Itk test-beam October 2016 at CERN SPS

Charge sharing effects between neighbouring implants seen at low voltages in charge and hit efficiencies maps



Estimation of the hit efficiency for a 50x50 μm² pixel





- Increasing the bias voltage to 500V the loss of efficiency due to charge sharing is less relevant
- In-pixel efficiency of the 50x50 μm² implant (implant at the edge) is the closest approximation of the possible performance of a planar pixel cell RD53 compatible without any biasing structure

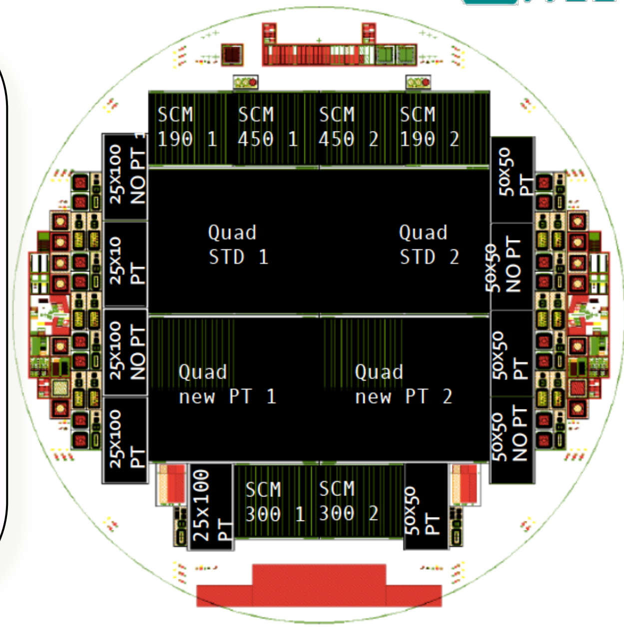
Same kind of modules now being irradiated to higher fluences in Birmingham

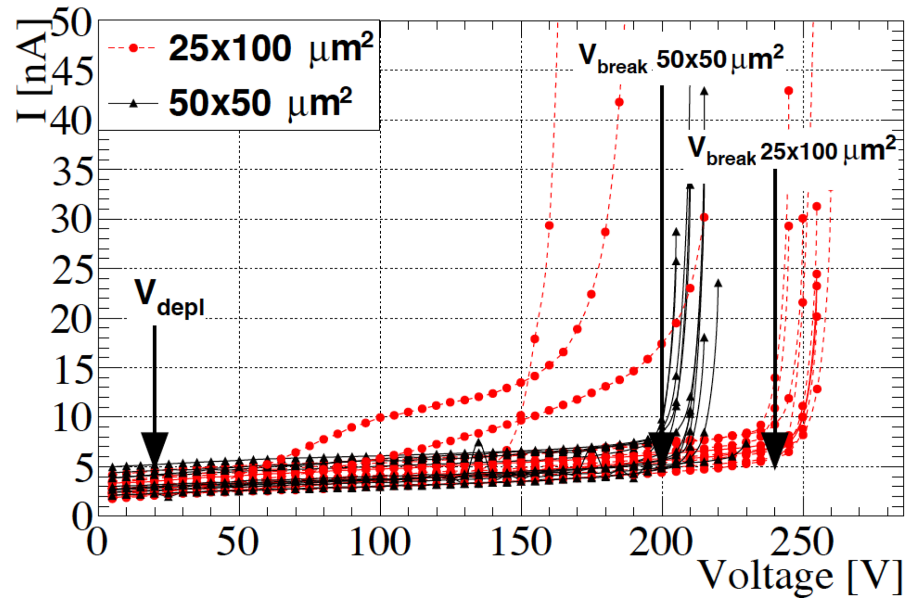
SOI productions at MPG-HLL

- High resistivity SOI 6“ wafers
  - 6 wafers 100 μm thick
  - 4 wafers 150 μm thick

SOI3

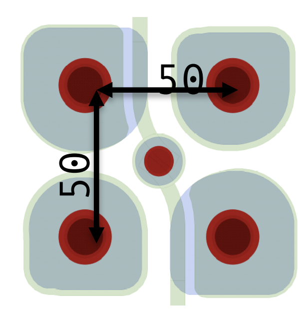
- Post-processing at IZM completed and sensor delivered to MPP for measurement
- BCB and UBM processing
- complete etching of the handle wafer + Aluminum on backside



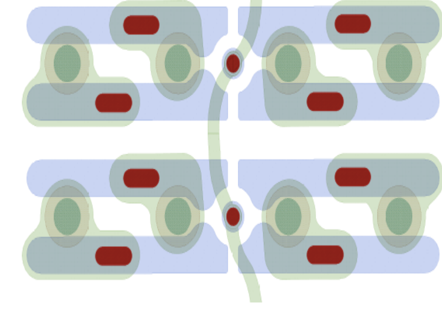


IV curves of RD53 compatible sensors

50 x 50 μm² cell



25 x 100 μm² cell

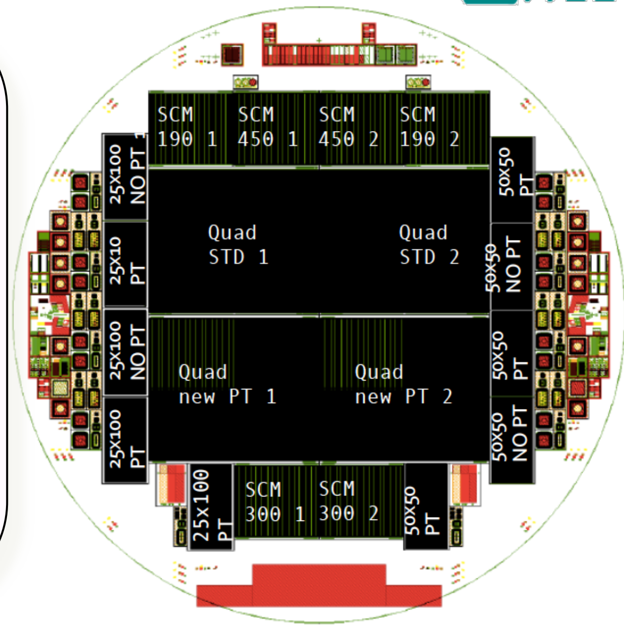


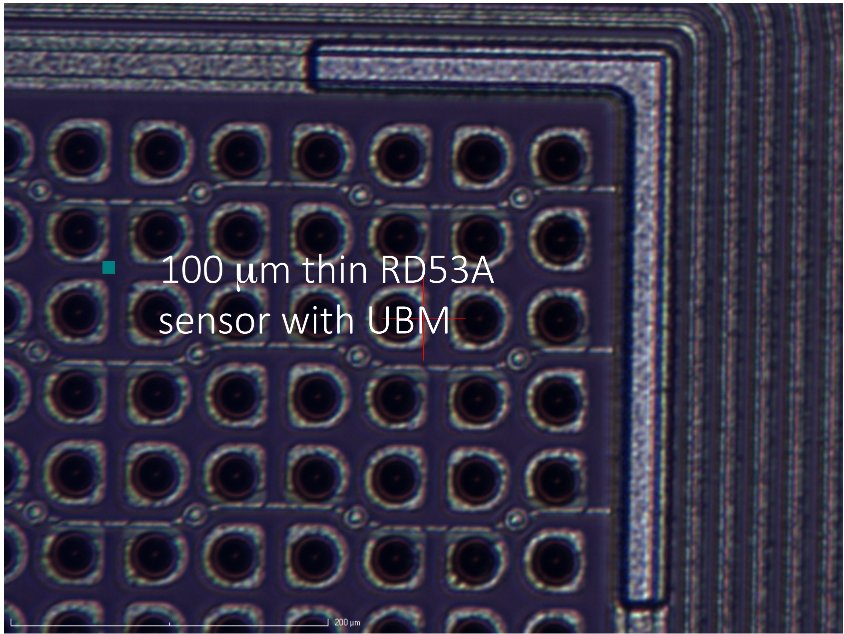
SOI productions at MPG-HLL

- High resistivity SOI 6“ wafers
  - 6 wafers 100 μm thick
  - 4 wafers 150 μm thick

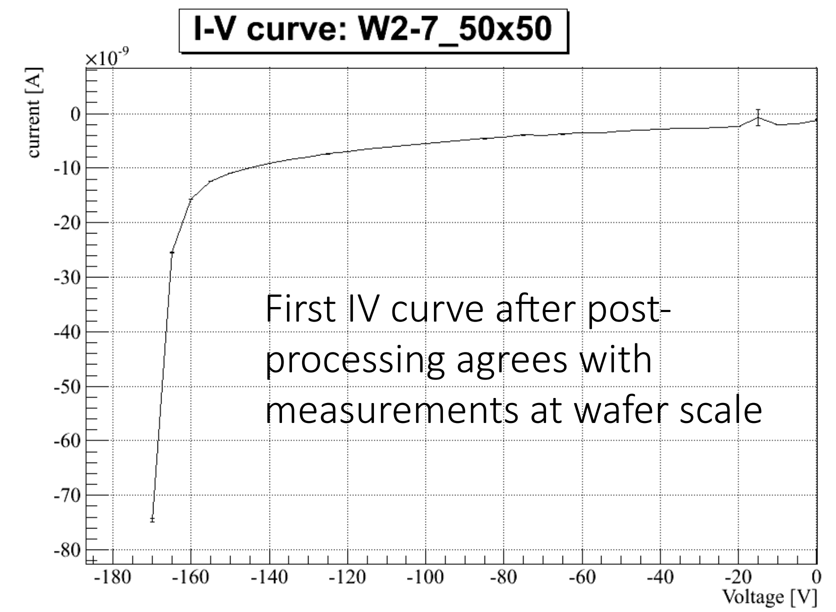
SOI3

- Post-processing at IZM completed and sensor delivered to MPP for measurement
- BCB and UBM processing
- complete etching of the handle wafer + Aluminum on backside



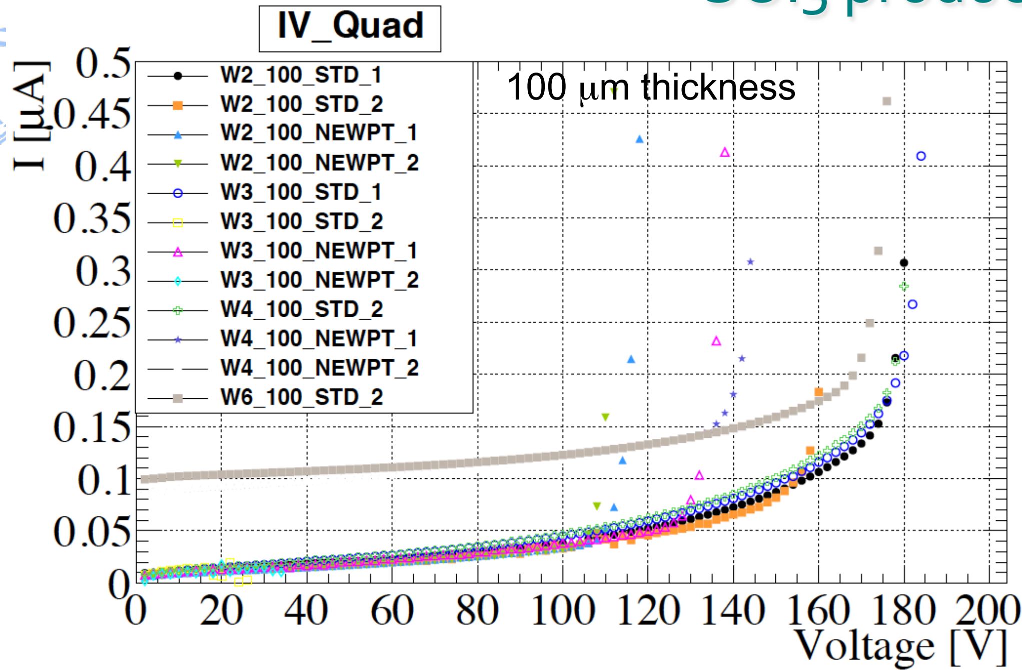


- 100 μm thin RD53A sensor with UBM



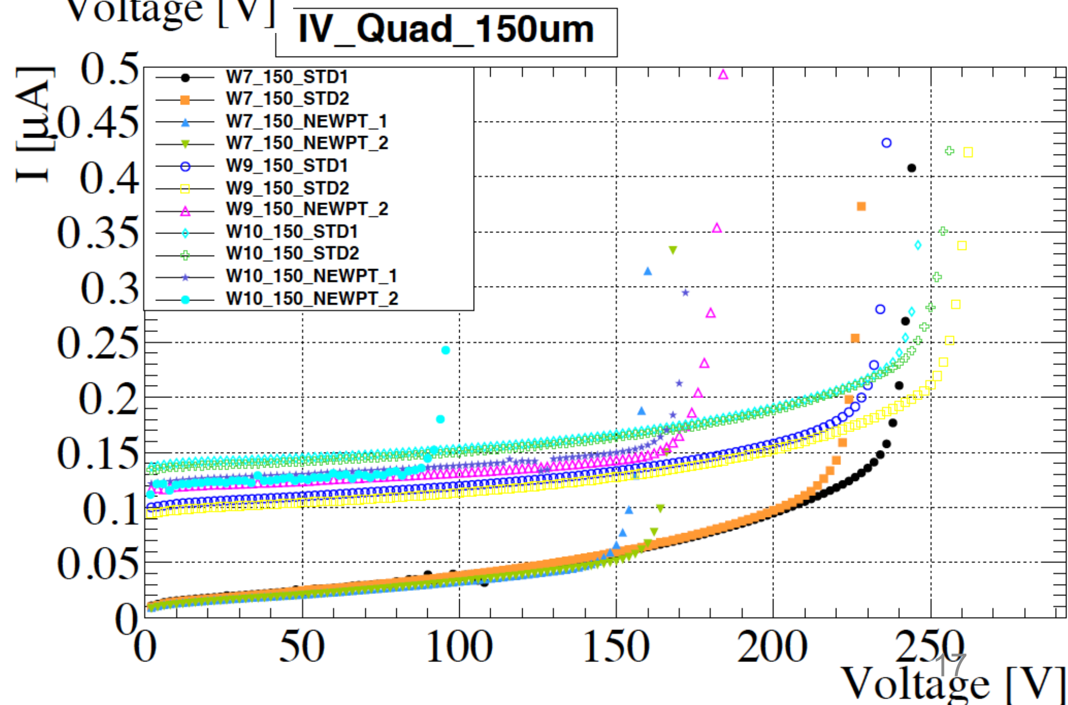
First IV curve after post-processing agrees with measurements at wafer scale

SOI3 production - FEI4 Quads



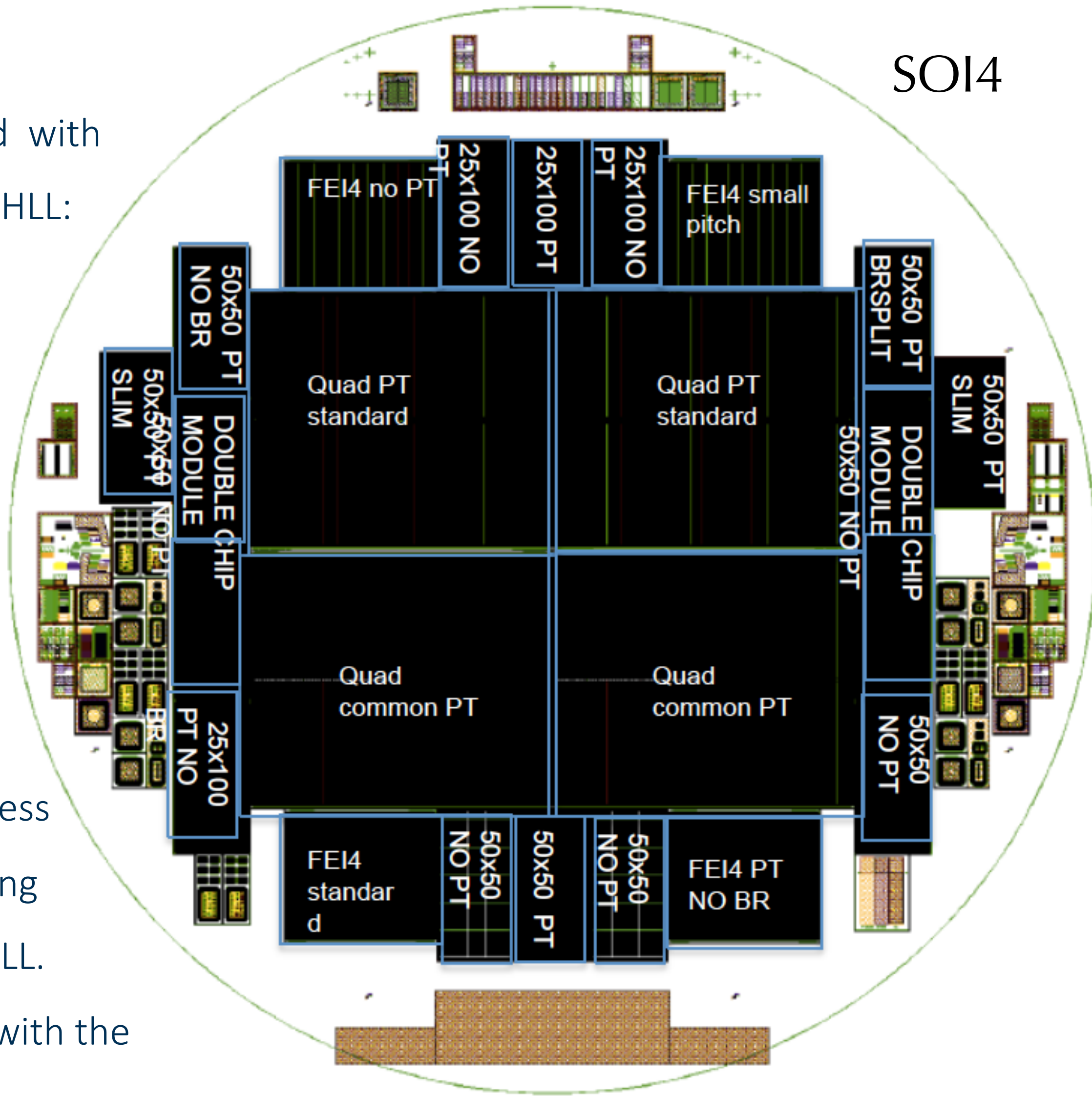
- Measurements performed after post-processing and dicing
- Process yield very satisfactory

- Flip-chipping at IZM to prove interconnection yield also for 100 um quads with higher statistics



SOI4 production at MPG-HLL

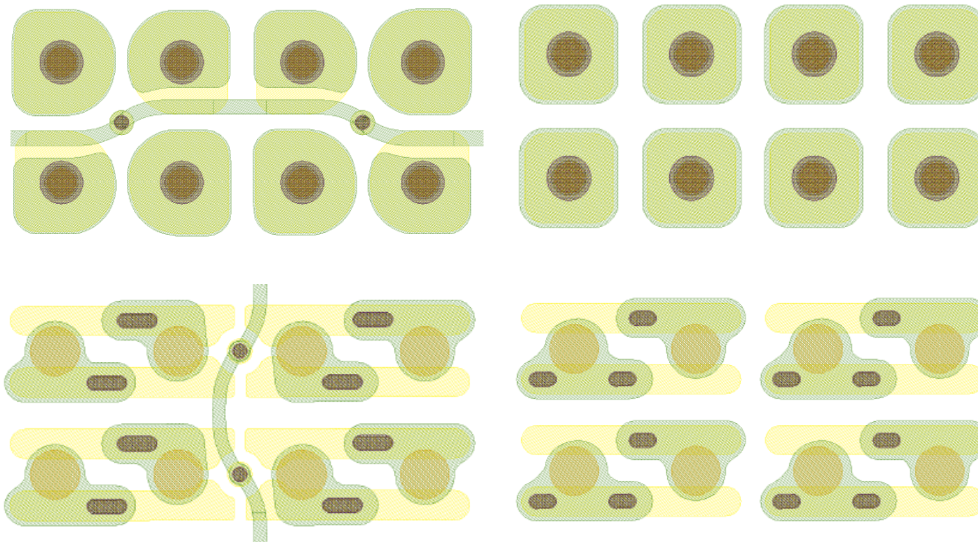
- New production of 9 wafers started with similar technology of SOI3 at MPG-HLL:



- 100 and 150 μm active thickness
- BCB, UBM processing + thinning planned to be performed at HLL.
- Cu used as UBM, compatible with the SnAg IZM bumps

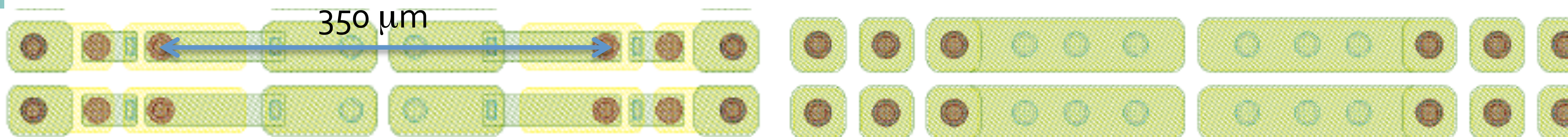
New RD53 designs in SOI4

- Common PT implant with smaller dimensions with respect to previous implementations (implant diameter from 18 to 10 μm)



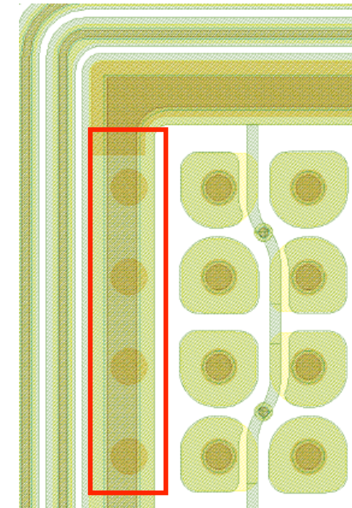
- Developing ideas how to contact the pixels without PT for testing before flip-chipping

- Double chip RD53A sensor (prototype for the inner layer or the inclined sections):
  - Two different implementations of pixels in the inter-chip area



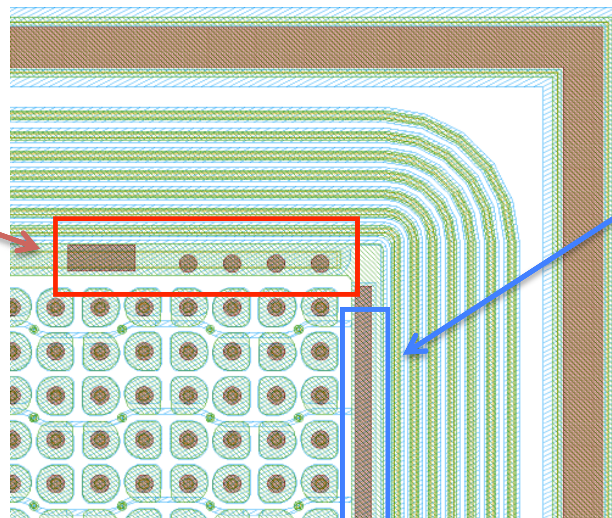
New Bias Ring designs

- Some sensors without bumps on BR:
  - Investigate if it is possible to reduce the effect of PT on hit efficiency after irradiation leaving the BR floating
  - Drawback: currents from the edges will flow directly into edge columns



- Second bias ring design: decouple the testing functionality before interconnection from the grounding after flip-chipping
  - Bias rails are all linked to a metal line not connected through contacts to the implant
  - bumps on BR are in contact to the BR implant

Bumps in contact with the BR implant



R. Richter

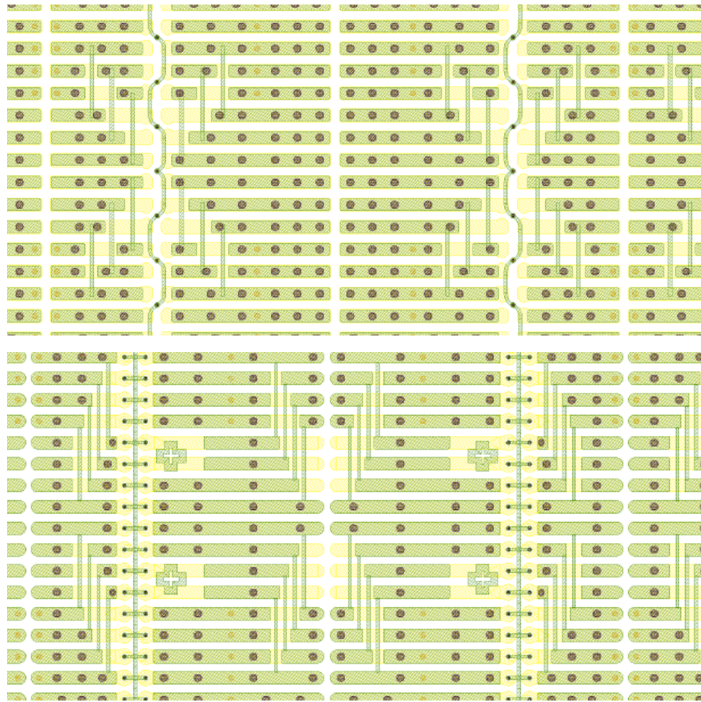
Testing metal line floating on the BR implant

Conclusions and Outlook

- Feasibility of producing thin quad sensors with good yield (100 and 150 μm thickness) demonstrated at CIS and HLL
- UBM at the sensor vendors under development with different technologies
- RD53 sensor design improved following the results of the test-beam analysis on FE-I4 sensors, several variants included in the ongoing productions
- Starting to think about possible methods of implementing testing of sensors without PT

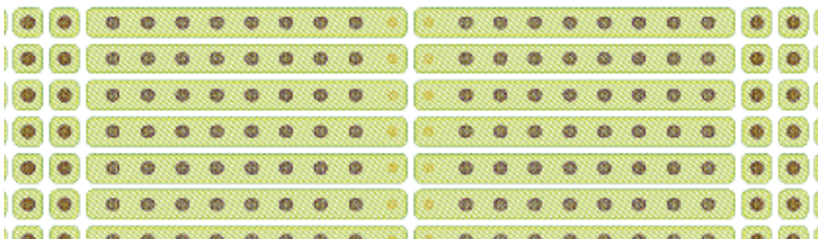
Additional slides

FE-I4 sensors in CIS 6" wafers and SOI4 production



- FE-I4 quad with common PT and 3 ganged rows each chip → 180 μm distance between physical edges of the chips
- 400 μm long pixels per side

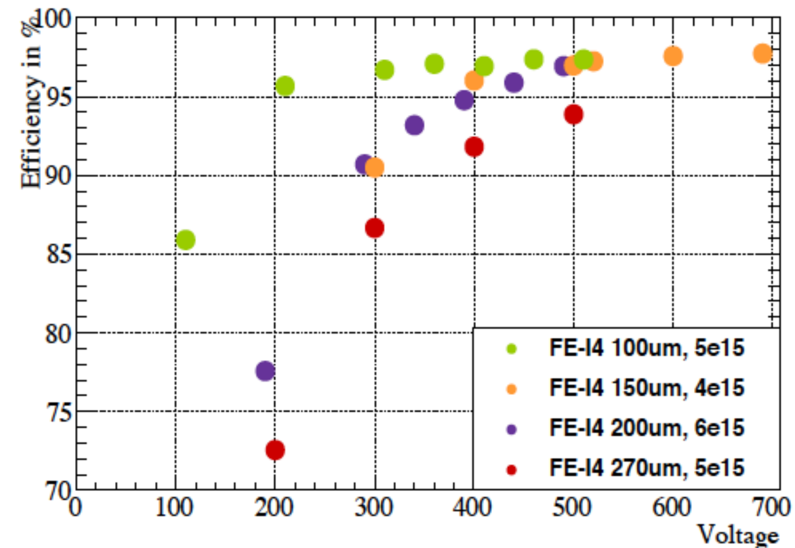
- Quad with standard PT and 4 ganged rows → 280 μm distance between chips
- 450 μm long pixels per side



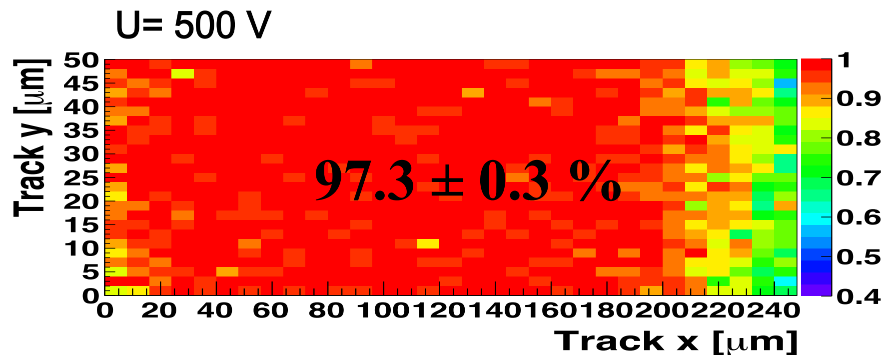
- FE-I4 compatible sensors with half the cells of 50x50 μm^2 pitch and no biasing structures
- Especially important to study post-irradiation performance of small cell sizes while waiting for the RD53A chip

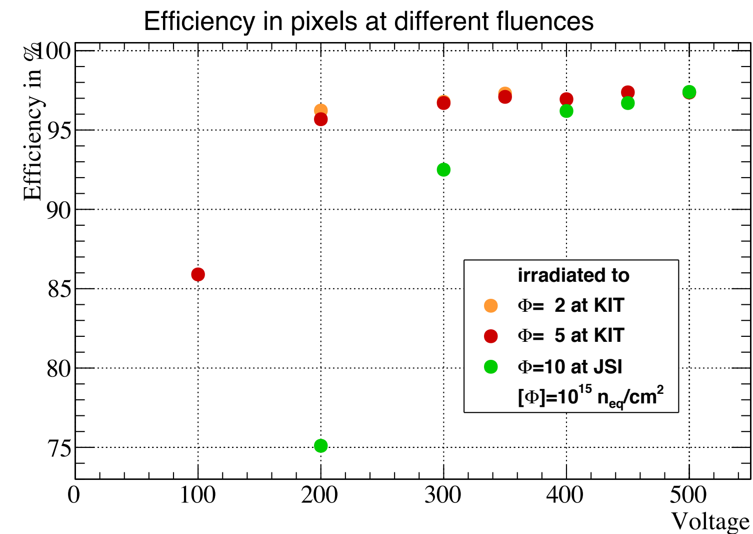
Thin sensors performance at high fluences

- 100 μm thin sensors yield the best hit eff. at 5×10^{15} n_{eq}/cm^2
- VTT FE-I4 module with 100 μm thin sensor irradiated at JSI at 1×10^{16} n_{eq}/cm^2
- Tested at DESY with 5 GeV electrons, threshold tuning to 1300 e

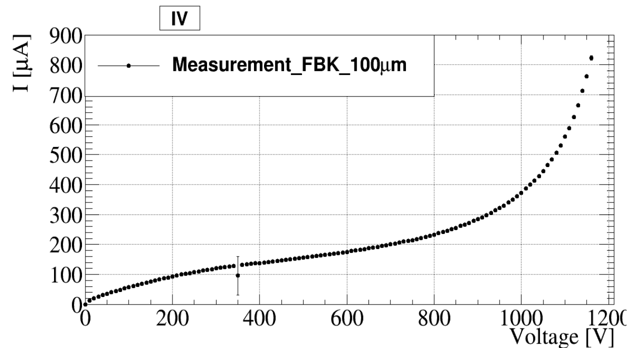


- significantly lower efficiencies at 200 and 300 V at $\Phi=1\times10^{16}$ n_{eq}/cm^2
- efficiencies at different fluences have similar saturation values (~97%)

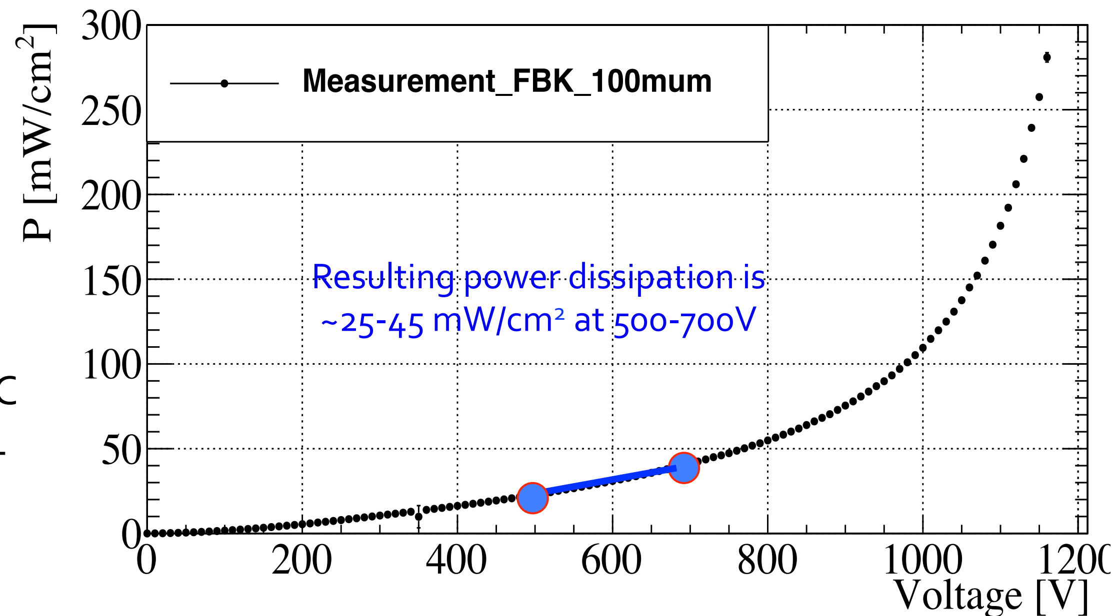




Power dissipation for thin planar sensors at high fluences



IV curve of bare FE-I4 sensor at -25˚C irradiated to **$1x10^{16}$ n_{eq}/cm^2** after 11 days of annealing, as measured in direct thermal contact in a probe-station

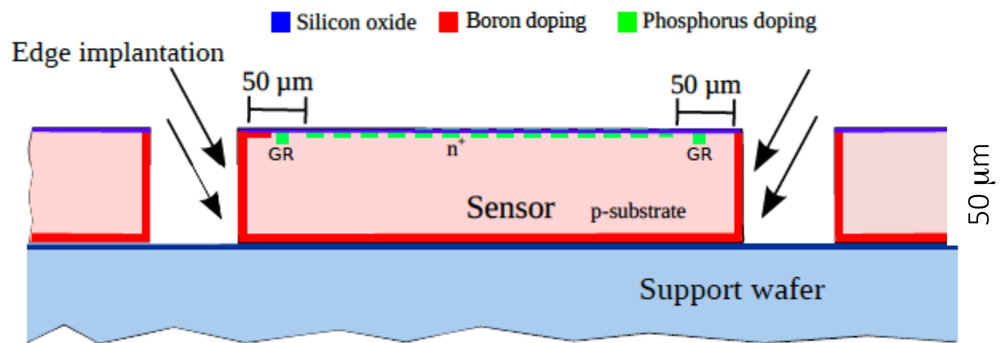


Estimated power dissipation per cm² at -25˚C for a 100 µm thin sensor irradiated to **$1x10^{16}$ n_{eq}/cm^2**

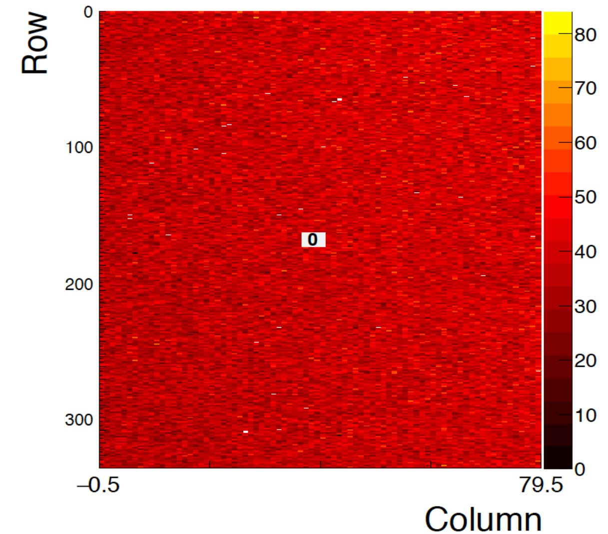
- The possible range of operation bias voltage for a pixel module with a 100 µm thick sensor is **500-700 V**
- The resulting power dissipation at 500-700 V is **~25-50 mW/cm²** at $1x10^{16}$ n_{eq}/cm^2 irradiation

ADVACAM: 50 μm thick sensors

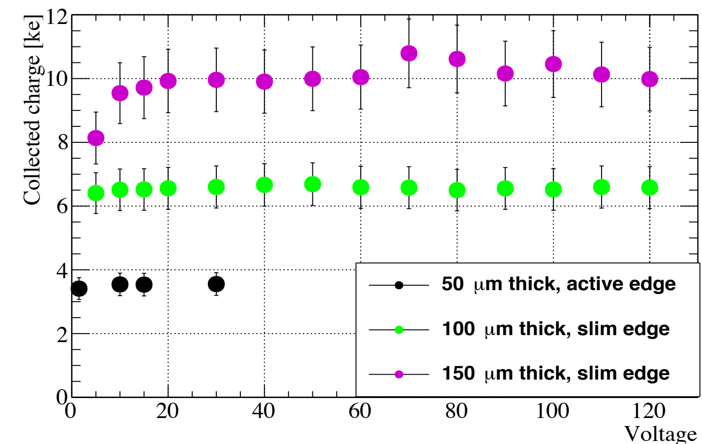
- Active edge sensors produced on SOI wafers at ADVACAM



Occupancy map from Cd scan of a module with a 50 μm sensor

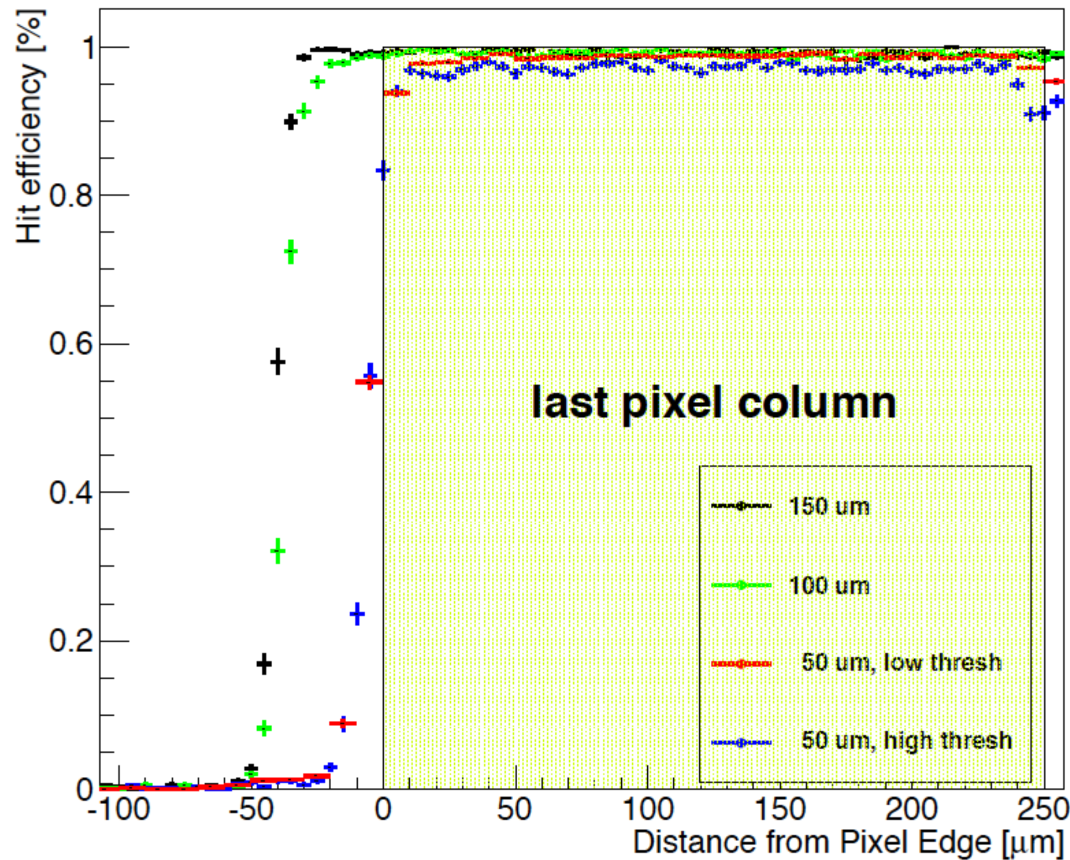


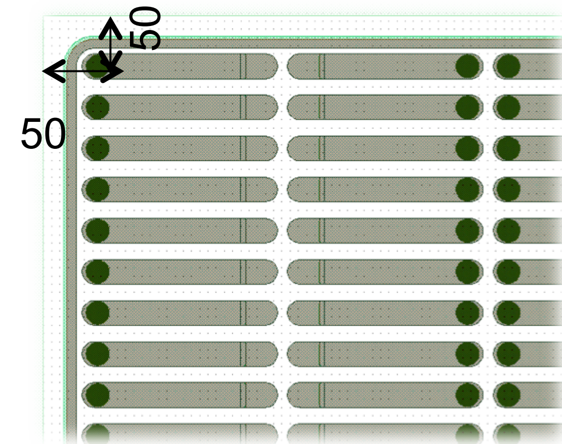
- Modules with 50 μm thin sensors and Cu-Au UBM show a perfect interconnection efficiency
- Collected charge by ^{90}Sr scans agrees with expectations for the three thickness
- 50 μm thin sensors needs a special tuning to very low thresholds ≤ 1000 e



Hit efficiencies for active edge devices

- August + October test-beam at CERN: systematic comparison of different sensor thicknesses





- Very good performance up to the edge of 100-150 μm thick sensors

- New measurements with 50 μm thin sensors at lower threshold then presented before (600 e- nominal instead of 800 e-)
- Higher efficiency on pixel implant with lower threshold (~98.8%) but still worse edge eff. with respect to thicker sensors