POLITECNICO DI MILANO

Silicon Drift Detectors and Readout ASICs for High-Resolution and High-Count Rate X-Ray Spectroscopy

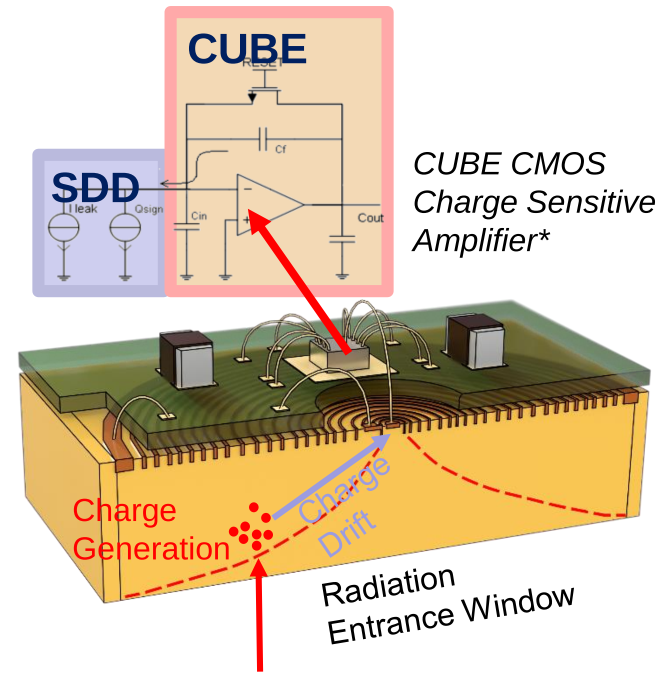
G.Bellotti (1,2), A.D.Butt (1,2), M.Carminati (1,2), C.Fiorini (1,2), G.Borghi (3), C.Piemonte (3), N.Zorzi (3), L.Bombelli (4)

1 Politecnico di Milano, Dipartimento di Elettronica, Informazione e Bioingegneria, Milan, Italy
2 INFN, Sezione di Milano, Milan, Italy
3 Fondazione Bruno Kessler - FBK, Trento, Italy
4 XGLAB srl, Milano, Italy

INFN Istituto Nazionale di Fisica Nucleare SEZIONE DI MILANO

FONDAZIONE BRUNO KESSLER

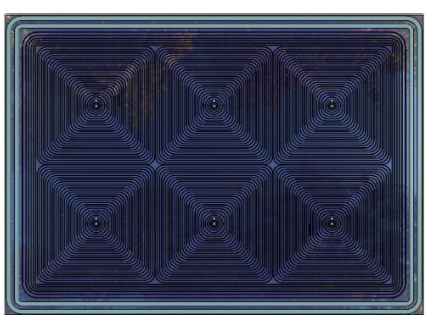
Arrays of Silicon Drift Detectors and CMOS preamplifiers



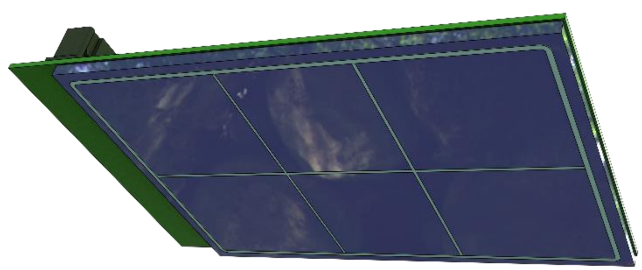
- **Silicon Drift Detectors** allow to reach high energy resolution and high count rate capability
- Low noise **Charge Amplifier** is bonded close to SDD anode
- Further readout electronics can be placed relatively far away from SDD
- **SDDs arrays and CMOS preamplifiers** represent a versatile detector solution for X and γ-ray applications

**L. Bombelli, et al., " "CUBE", A Low-noise CMOS Preamplifier as Alternative to JFET Front-end for High-count Rate Spectroscopy", Nuclear Science Symposium Conference Record, 2011, N40-5.*

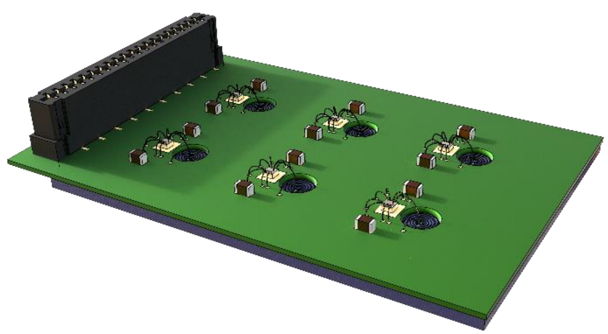
SDD monolithic array



SDD array mounted on a ceramic



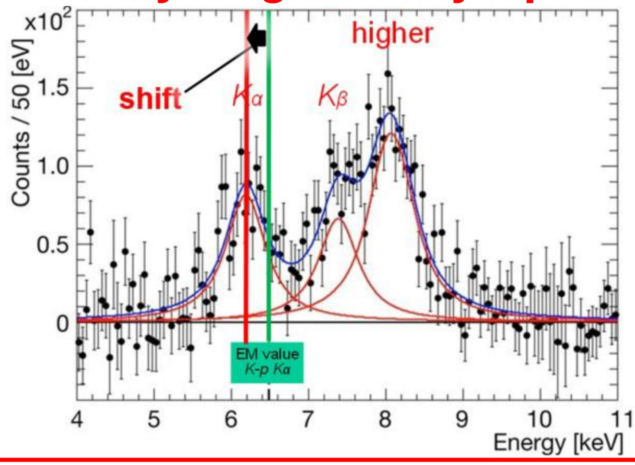
SDD array and CUBE

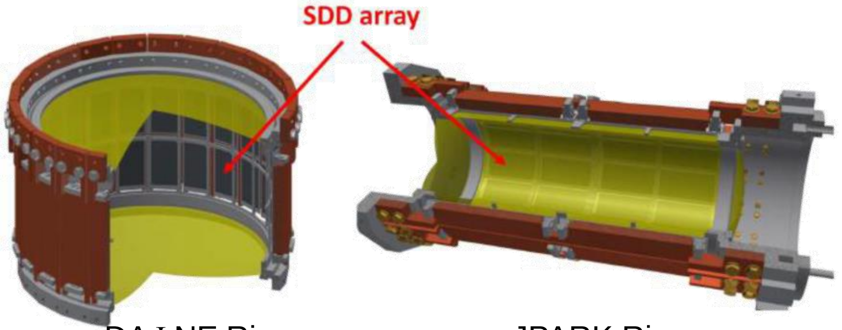


SIDDHARTA-II (1)
Silicon Drift Detectors for Hadronic Atom Research by Timing Application

Goal: Study of strong nuclear interaction using the measurement of hadronic broadening of the 1s state of the kaonic hydrogen with highest possible resolution

Kaonic Hydrogen X-ray Spectrum





DAΦNE Ring JPARK Ring

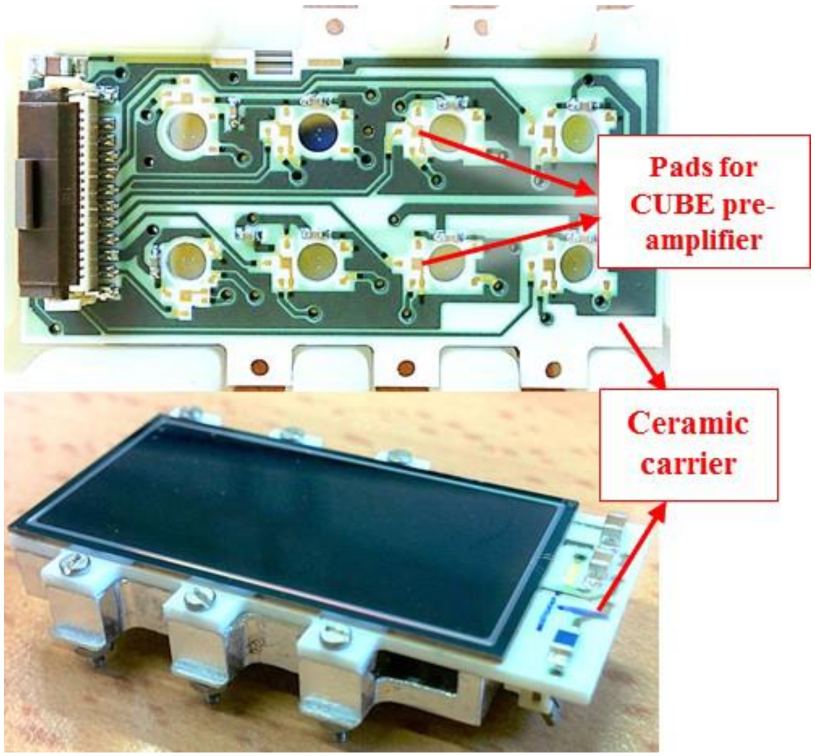
Detector features:

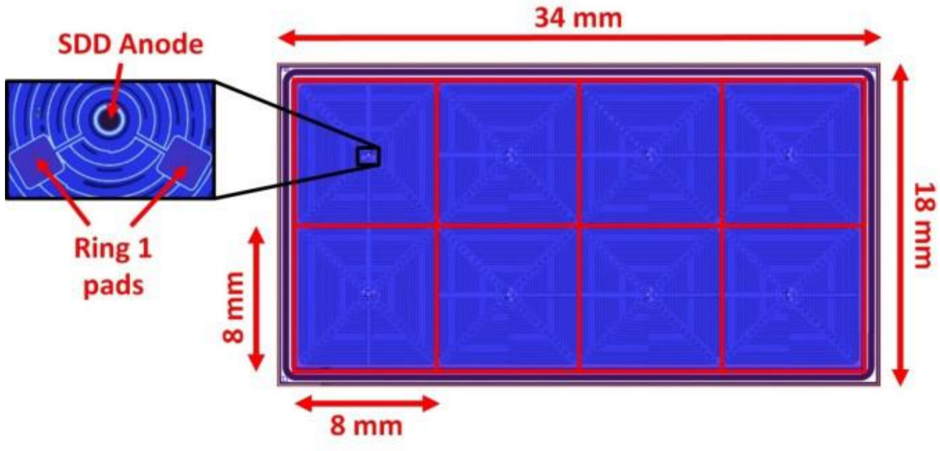
- Energy range: **0.2keV – 18keV**
- Operating **temperature below 120k** to minimize SDD's drift time to improve background suppression
- Big detection area to increase low rate events cunt rate
- **Non-Linearity** below **few eV** within the **4 to 15 keV** energy range
- **Output stability** of a few eV/day

Detector System:

- Detector System ring structures for DAΦNE and JPARK colliders
- DAΦNE structure contains 48 SDD modules, JPARK structure 24

SIDDHARTA-II (2)
Detection Module

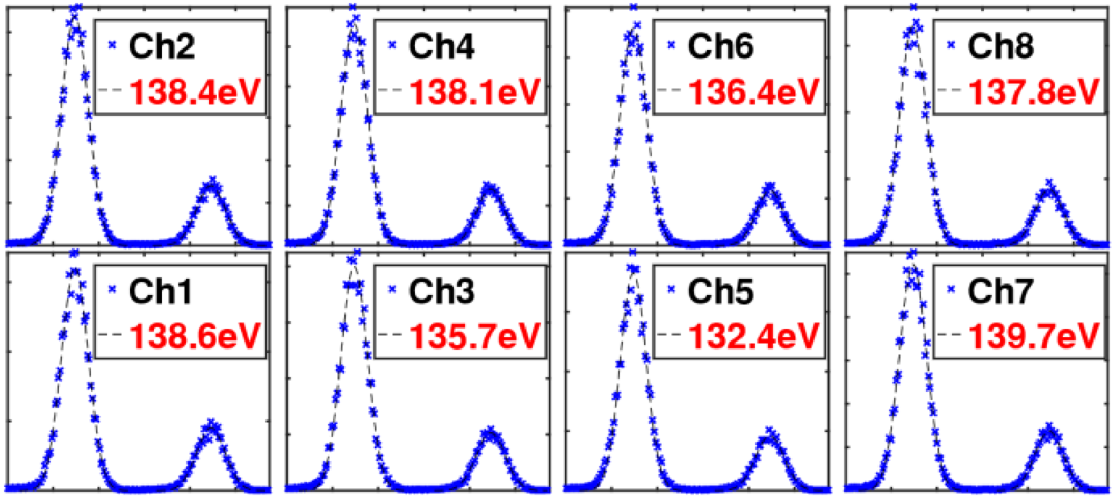




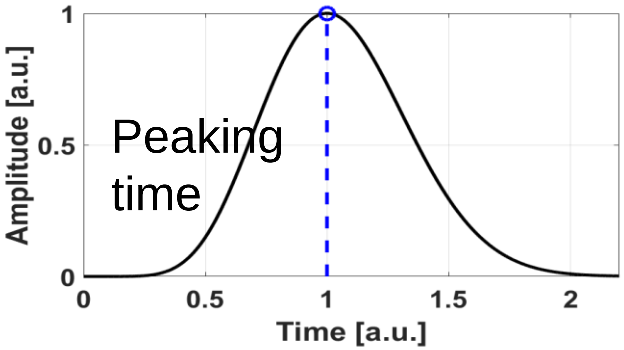
- Detectors by **Fondazione Bruno Kessler** on 450 μm thick silicon wafer
- **2x4 array** with squared elements of **8x8 mm^2** with 1mm dead are around borders
- SDD mounted on **Alumina ceramic carrier** connected to an **aluminum holder block** for cryogenic cooling
- **8 CUBE chips** connected one per channel through chip to chip bonding

SIDDHARTA-II (3)
Energy Resolution at Cryogenic Temperature and Stability

Best ^{55}Fe Spectra at 1 μs peaking time with SFERA ASIC

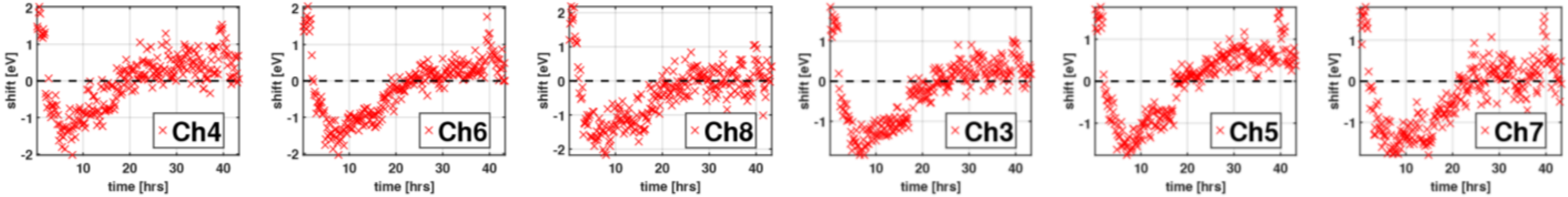


T [k]	109
ICR [kcps]	1
Tpeak	1μs



At 109 k the effect of ballistic deficit on resolution is negligible

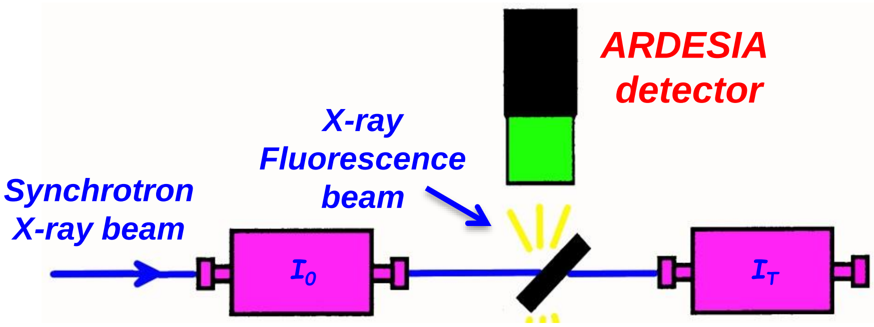
$^{55}Fe\ Mn\ K\alpha$ Peak Stability



Peak position of Mn Kα line during time. Peak drifts by less than 2eV over 40 hours

ARDESIA (1)
Array of Detectors for Synchrotron Radiation Applications

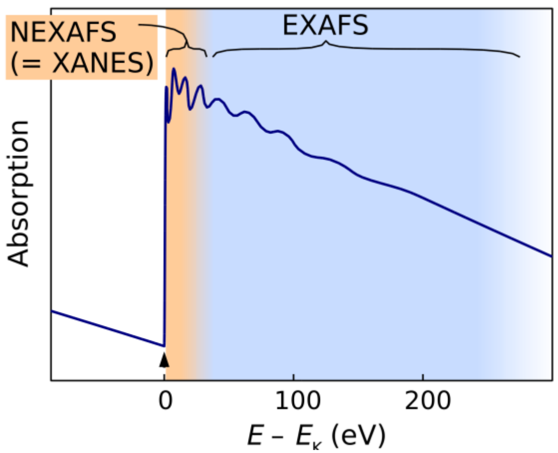
Goal: Development of a **versatile detector** based on **arrays of Silicon Drift Detectors** and **low-noise electronics** for **Synchrotron applications**



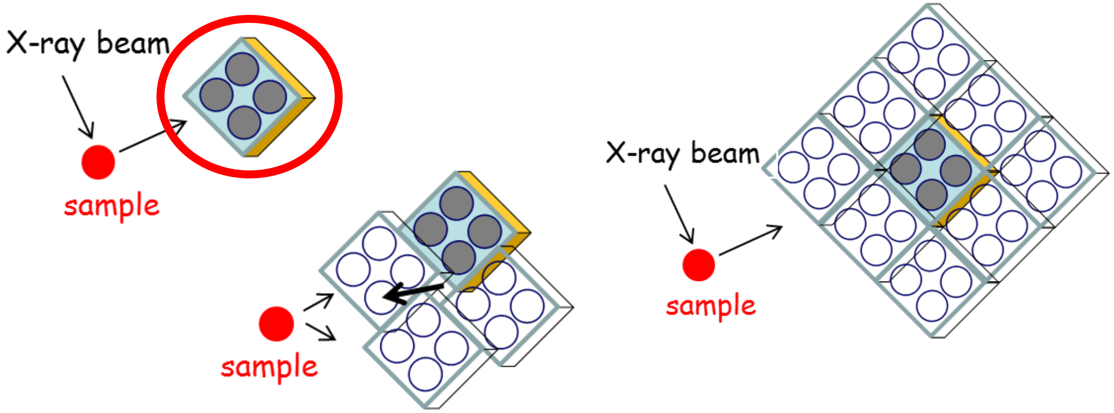
Detector features:

- Energy range: **0.2keV – 20keV** (Silicon detection region)
- **maximized throughput** (> 1Mcps/ch.) still with **good energy resolution**
- **Modularity, versatility, operation close to room T**

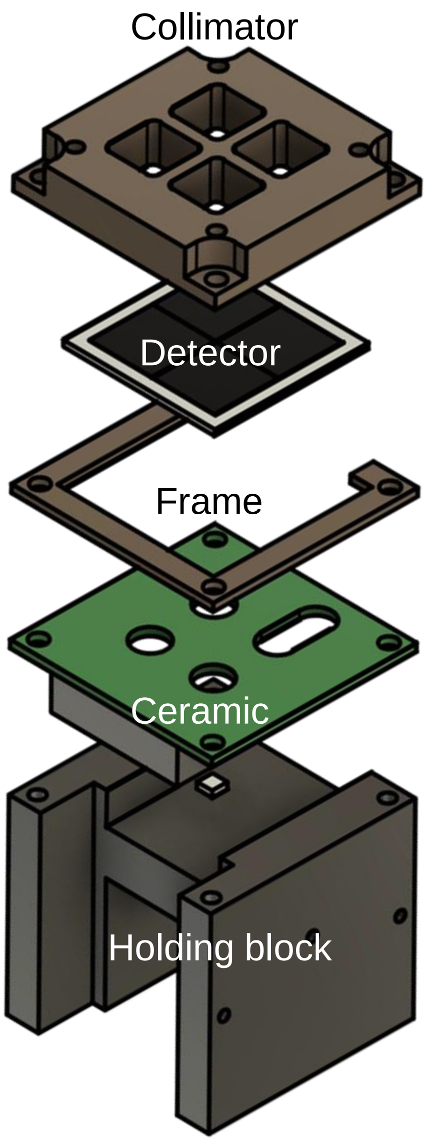
XRF and XAFS applications

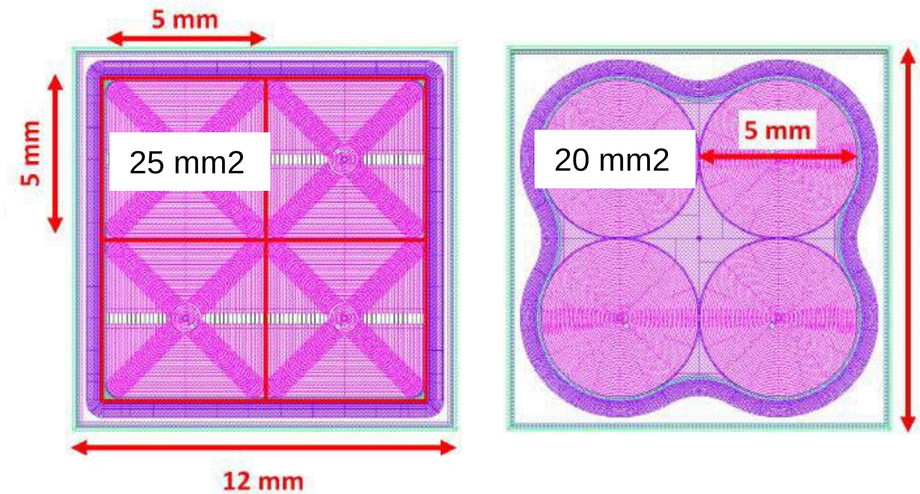


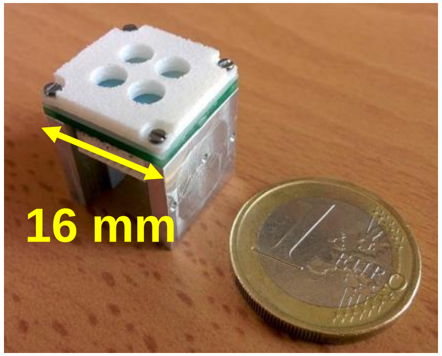
ARDESIA modular design approach:



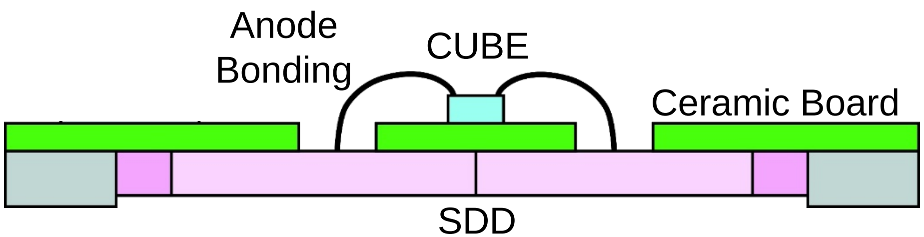
ARDESIA (2)
Detection Module



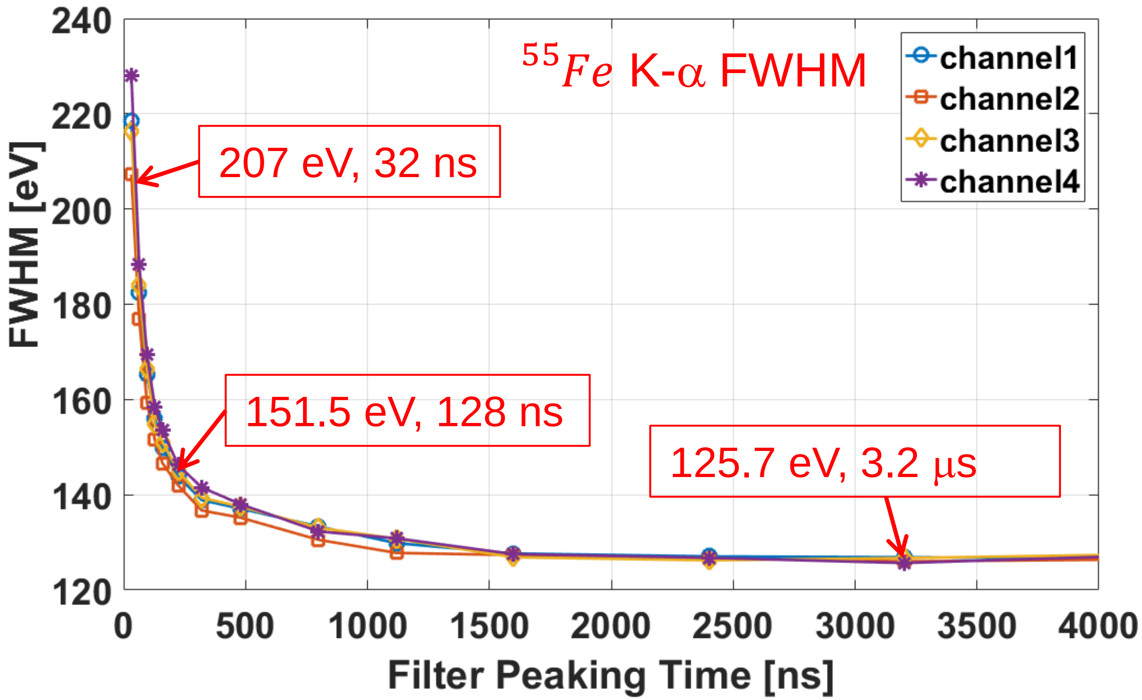




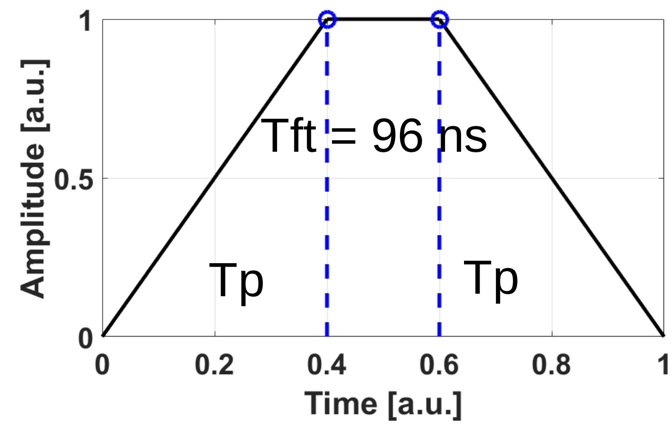
- Detectors by **Fondazione Bruno Kessler** on 450 μm thick silicon wafer
- **Low leakage technology process** (leakage current below $200\, pA/cm^2$ at room T)
- **2x2 array** with squared elements of 25 mm^2 area or circular elements with 20 mm^2 area
- **4 channels** integrated **CUBE** preamplifier



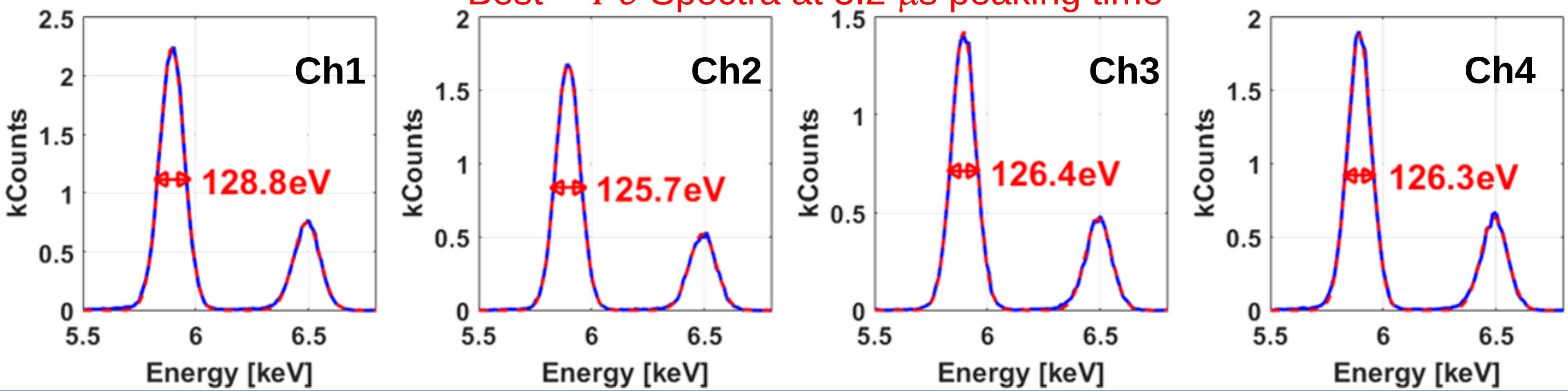
ARDESIA (3)
Energy resolution with XGLab DANTE DPP



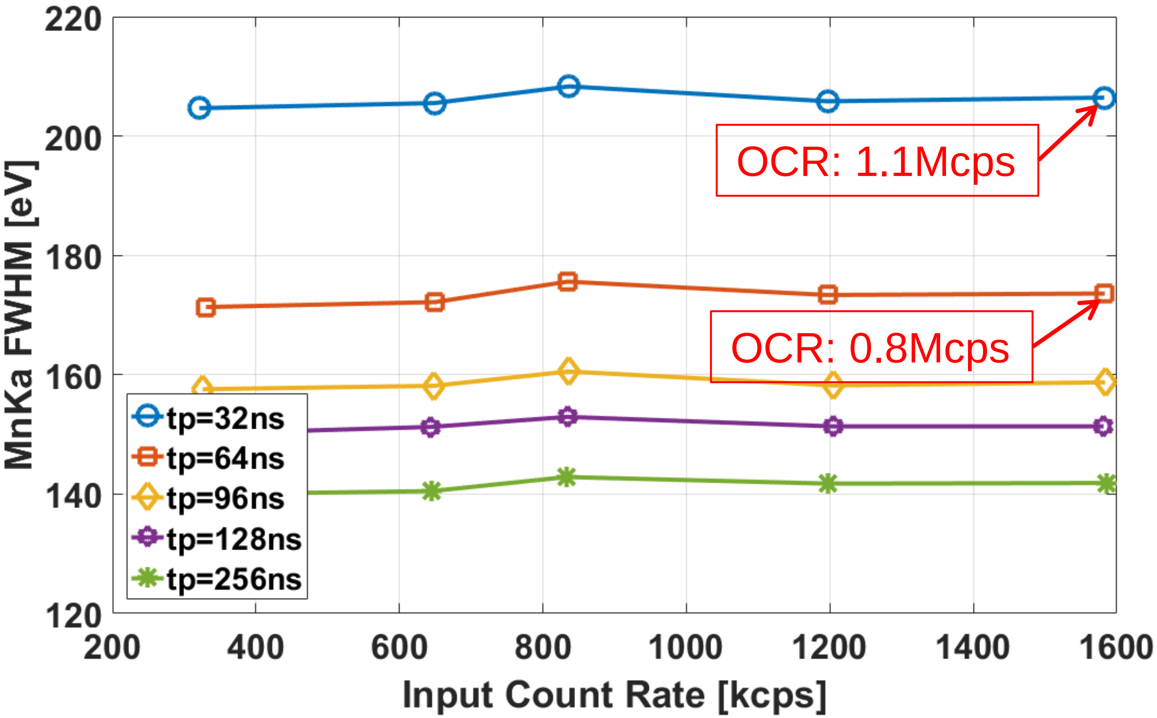
T [°C]	-27
Jleak [pA/cm2]	1
ICR [kcps]	2



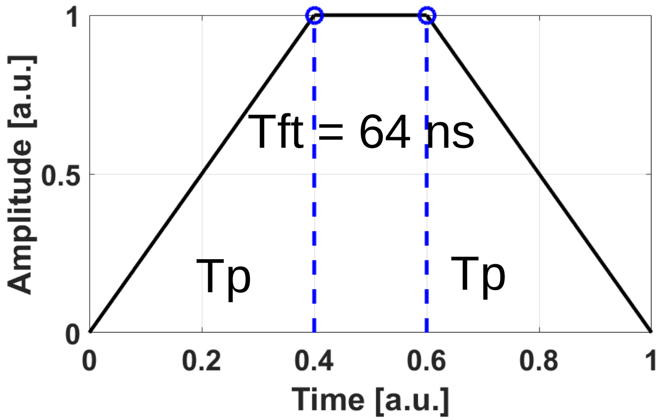
Best ^{55}Fe Spectra at 3.2 μs peaking time

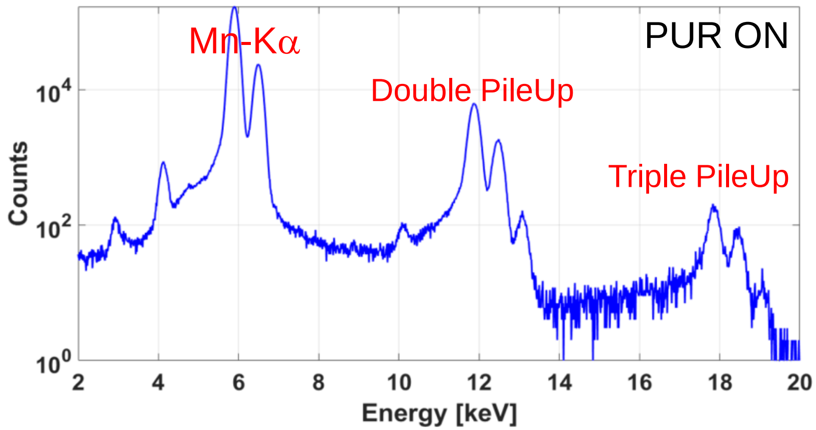


ARDESIA (4)
Energy resolution at High Count Rates



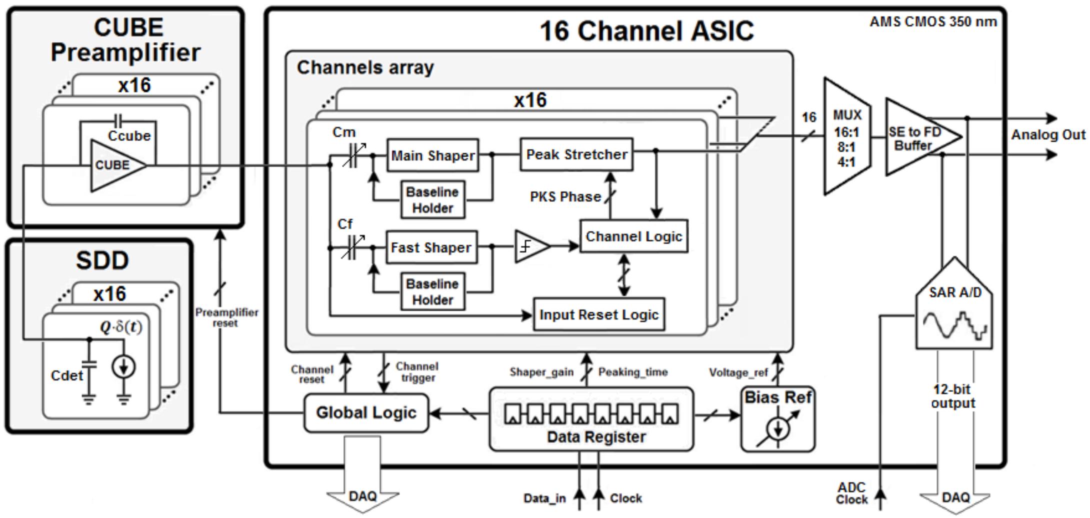
T [°C]	-27
Jleak [pA/cm2]	1

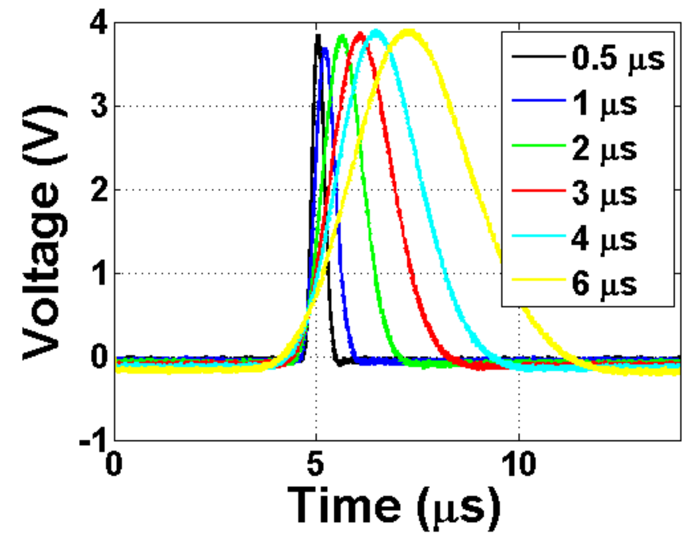


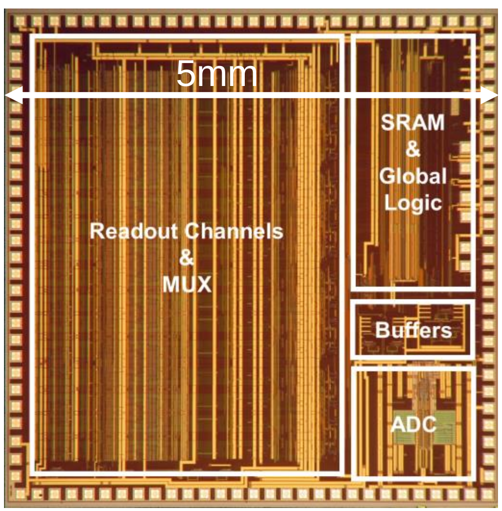


ICR [Mcps]	1.5
Tp [ns]	32
FWHM [eV]	206

SFERA (1)
SDD Front End Readout ASIC







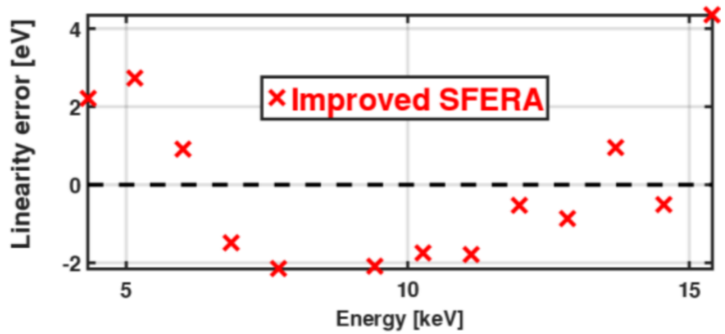
SFERA Main Features:

- **16 channels**, one or two analog multiplexer for serial readout
- **IX order**, time invariant, **semigaussian** pulse shaping amplifier, implemented in single ended topology
- **Six** different selectable **shaping times** (500 ns – 6 μs)
- **Five** selectable **energy ranges** (10 keV – 70 keV)
- **Three** different **multiplexer readout strategies**
- Integrated **12 bits SAR ADC**

F.Schembari et al., "SFERA: An Integrated Circuit for the Readout of X and γ-Ray Detectors", IEEE transactions on nuclear science, vol. 63, issue 3, p.1797-1807, 2016)

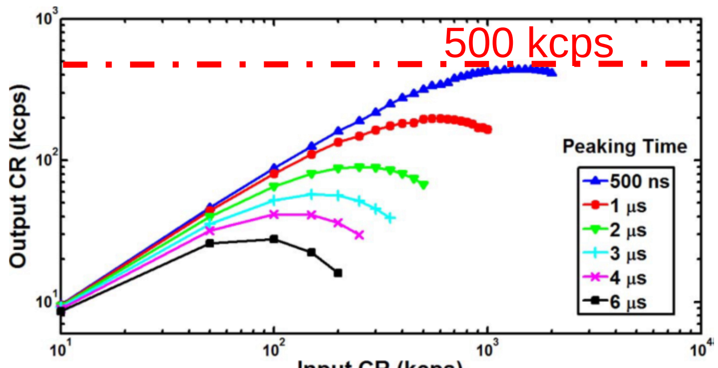
SFERA (2)
ASIC Performances

SFERA linearity on 16 keV energy range



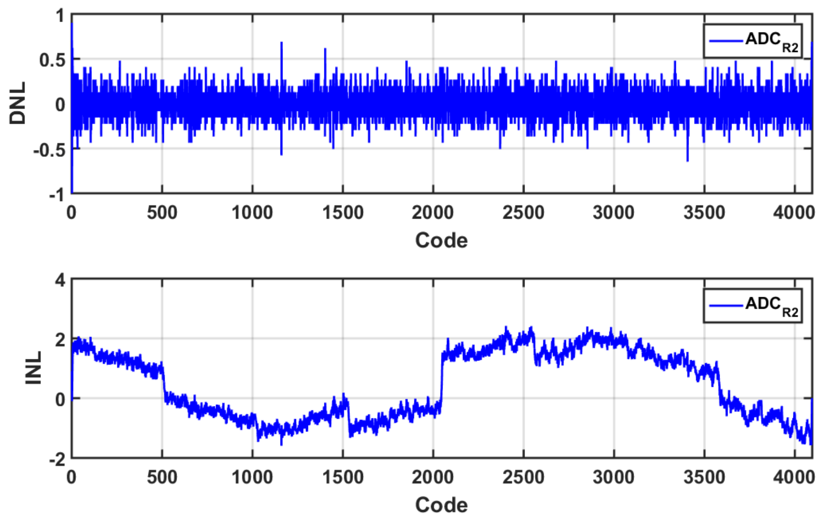
Only 4 electronvolt nonlinearity over 4-16 keV energy range

Input vs Output Count rate for all Peaking times

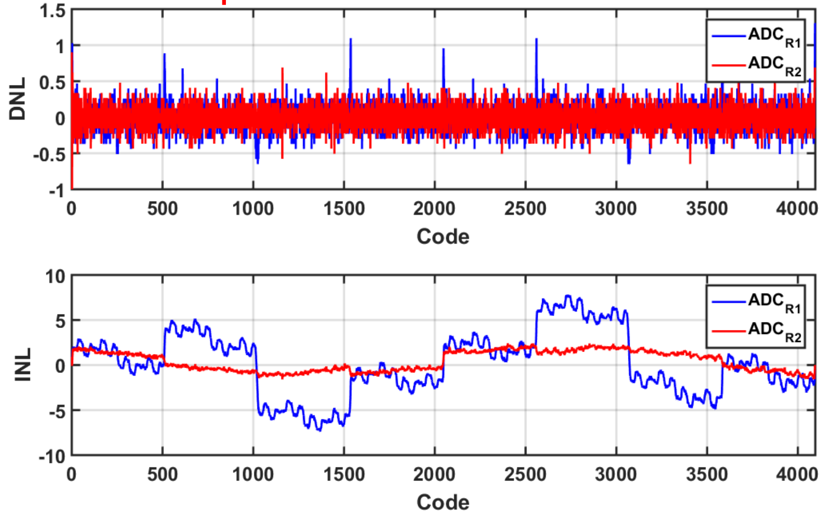


Up to 500 kcps output count rate with shortest, 500 ns, peaking time

Integrated ADC static characteristic

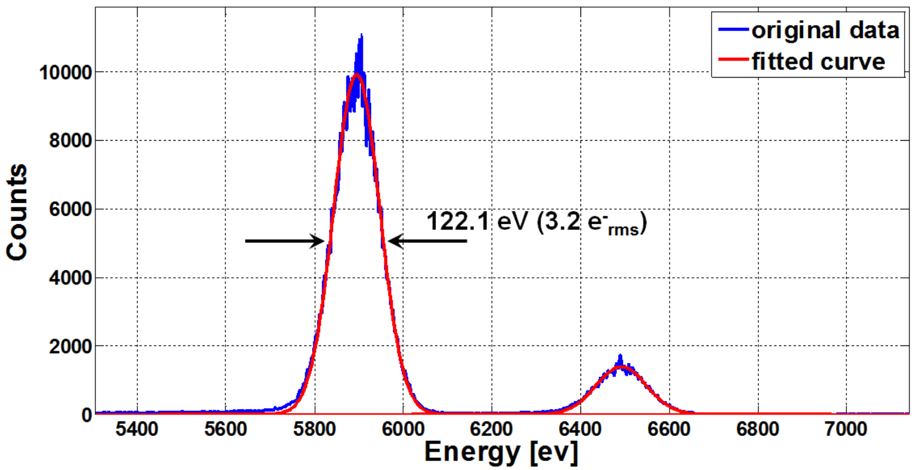


ADC Improvements in Second Release

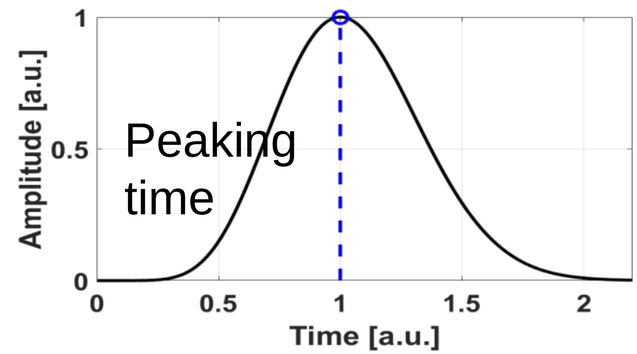


SFERA (3)
Spectroscopic Performances

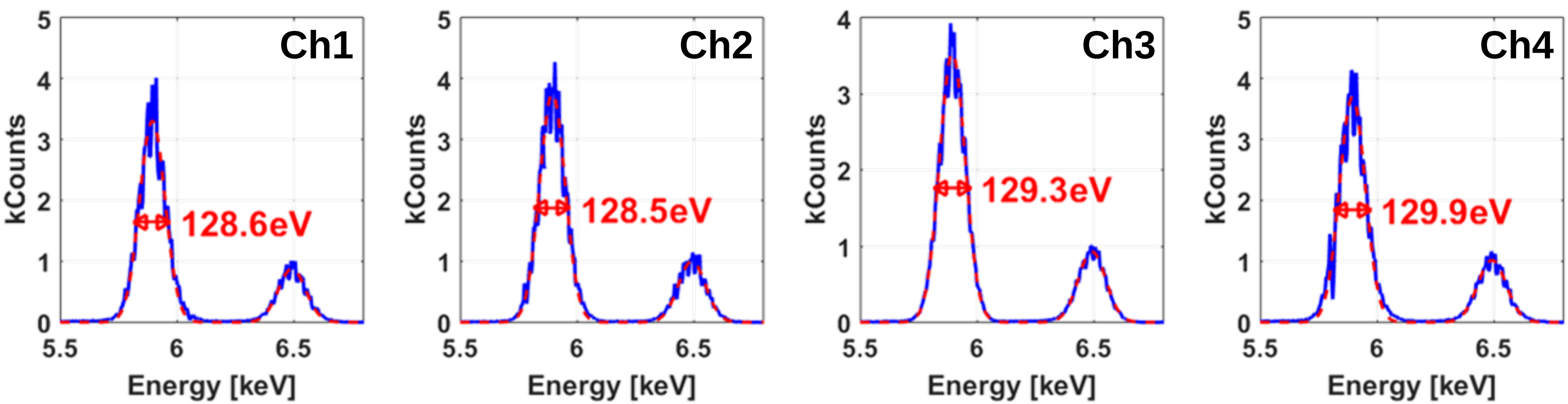
Optimal energy resolution with 10 mm^2 detector single SDD



T [°C]	-35
Jleak@Troom [pA/cm2]	50
Tpeak [μs]	4

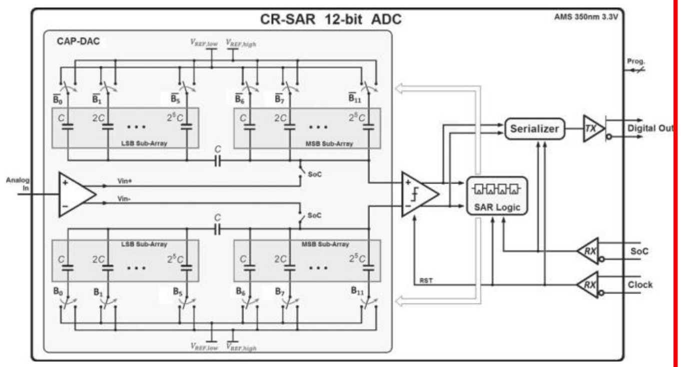


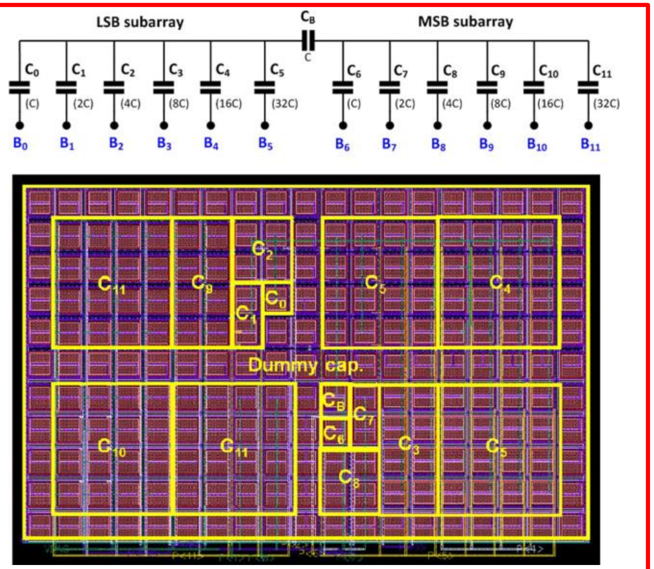
ARDESIA detector best spectra at 3 μs peaking time, measured with **internal ADC**



Thanks for your attention

SFERA (4)
12-bits SAR ADC



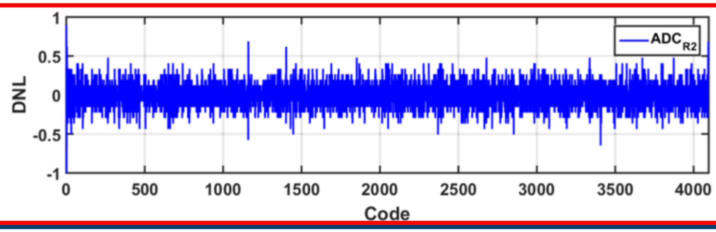


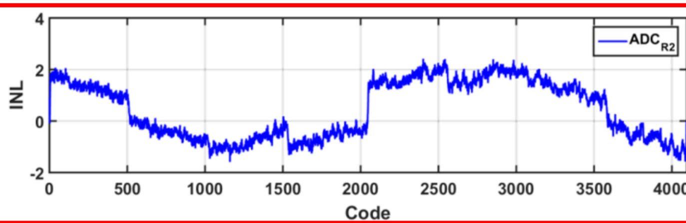
Architecture

- Charge-redistribution with bridge-capacitor-array
- Monotonic bottom-plate switching algorithm (highest power efficiency)
- Fully-differential topology to minimize the influence of common-mode noise and disturbances from the power supply

Capacitive DAC

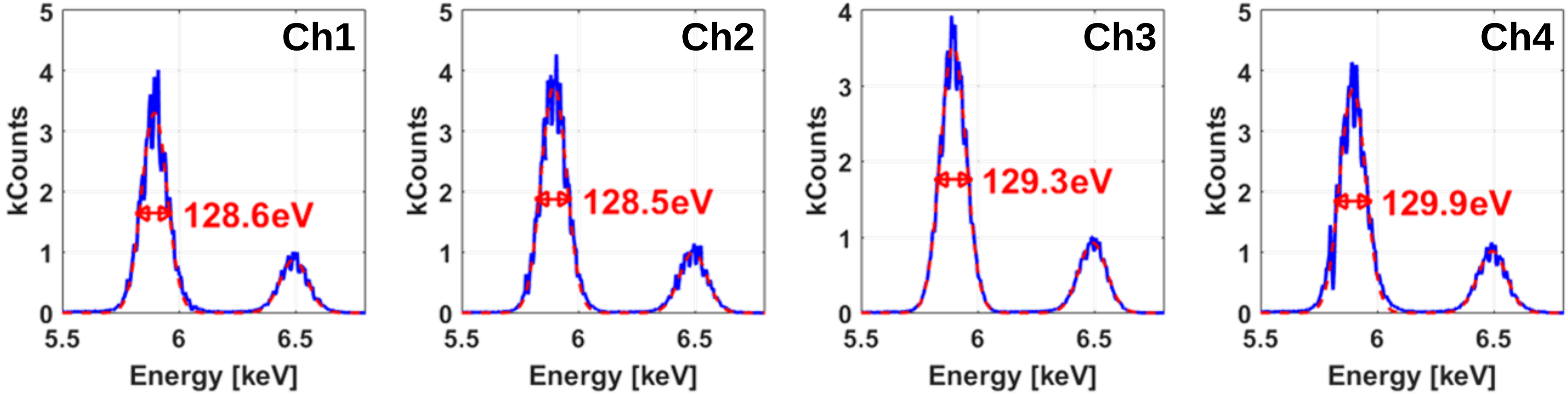
- Unitary capacitance is 140 fF
- Common centriod capacitances arrangements to cope with process oxide spreads
- Stray capacitances among one sub array top plate and other array bottom plate have been minimized by layout
- Top bottom stray capacitance of the same array have been optimized



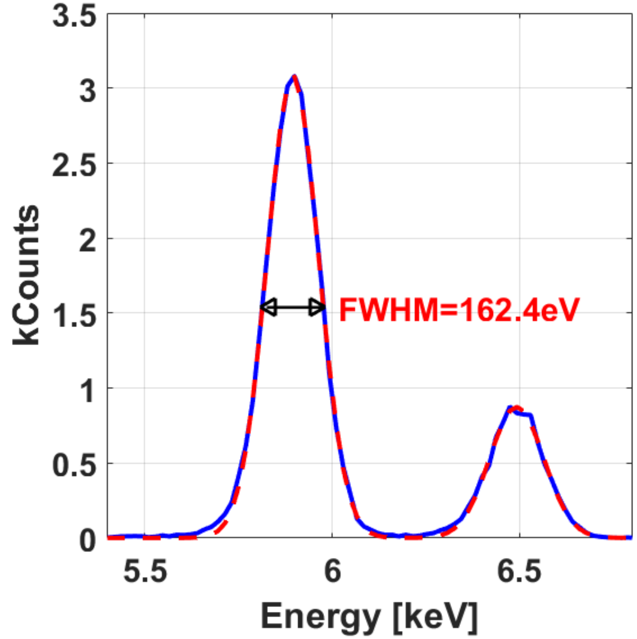


Measurements (3): Energy Resolution with SFERA ASIC

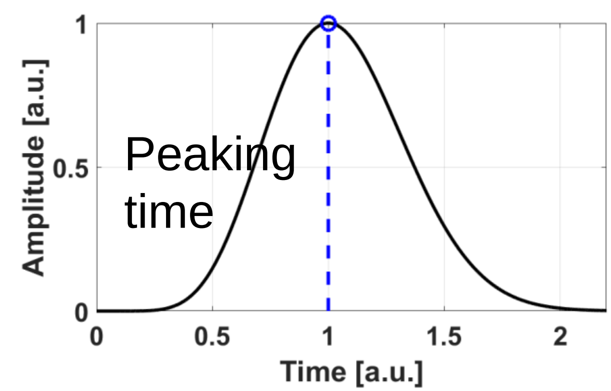
Best spectra at 3 µs peaking time, measured with **internal ADC** (12 bits, 4Msps, SAR)



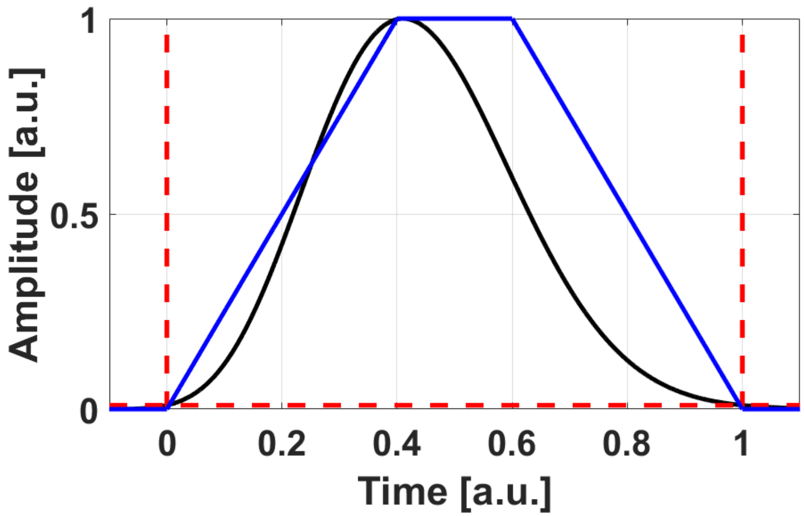
Spectrum acquired with fastest peaking time (**200 ns**)
Pulse shape acquired with oscilloscope and post processed.



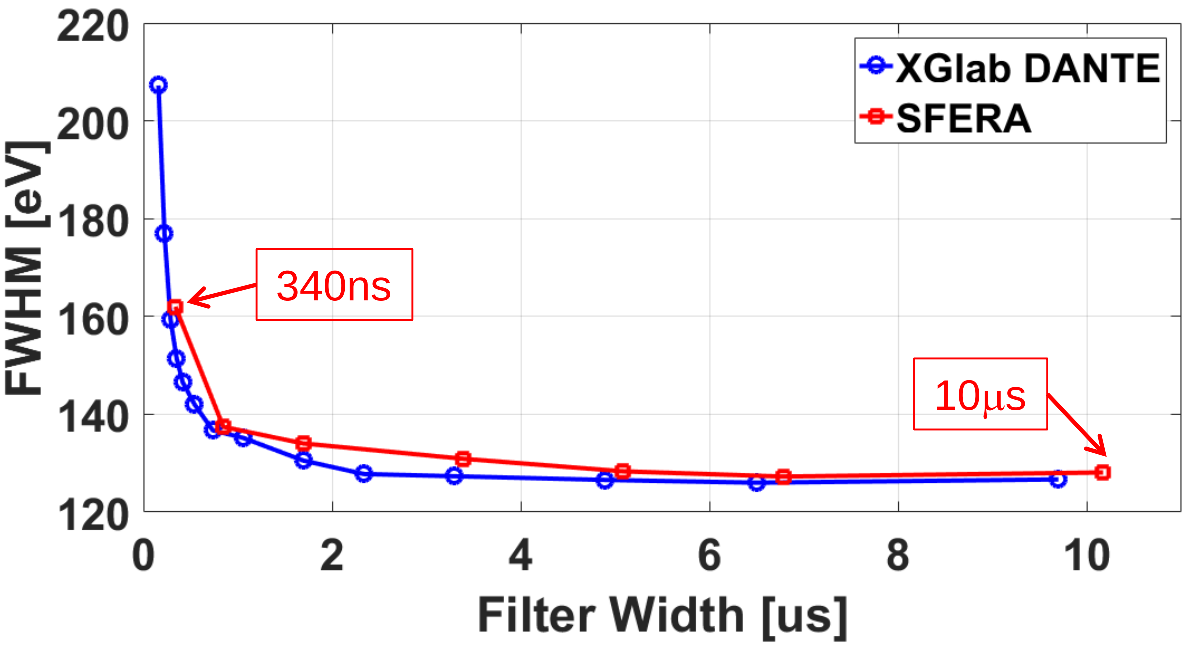
T [°C]	-27
Jleak [pA/cm2]	1
ICR [kcps]	2



Measurements (4):
A comparison between DPP and ASIC (same pulse width)

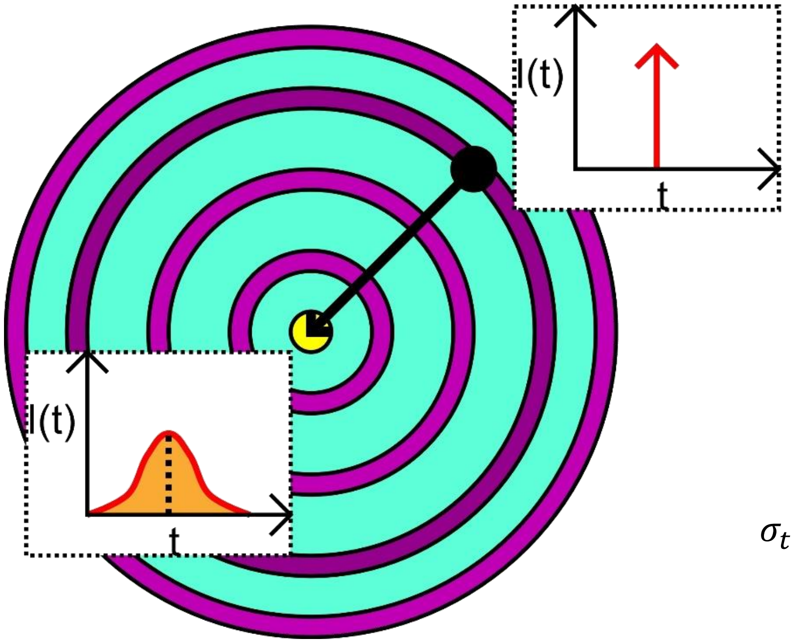


Trapezoid
$t_W = 2 \cdot t_R + t_{FT}$
Semigaussian IX order (width at 1% peak amplitude)
$t_W \cong 1.7 \cdot t_{peak}$



Comparison of energy resolution between DANTE and SFERA at corresponding pulse width

Preliminary Studies (1)
Ballistic Deficit Simulation (1)



- Spectra Broadening due to Ballistic Deficit Effect limits maximum Channel Size
- Simulations were needed to find out what is the maximum allowed channel size
- Simple analytical model is used to estimate charge pulse anode FWHM

$$\sigma_t = \left(\sqrt{\frac{2k_b}{q_e}} \cdot \sqrt{\frac{T_0}{\mu_0 V_{dep}^3}} \cdot L_0^2\right) \cdot \left(\frac{L}{L_0}\right)^2 \cdot \left(\frac{T}{T_0}\right)^{|Coeff_\mu|+0.5} \cdot \sqrt{\frac{d}{L}}$$

- Pulse Gaussian like waveform is convolved with filter pulse response. Convolution peak is signal at the end of readout chain.

$$v = max_\tau \left\{ \left[\left(\frac{Q}{\sqrt{2\pi\sigma_t}} \cdot e^{-t^2/2\sigma_t^2} \right) * h(t) \right]_\tau \right\}$$

- This is used to simulate random inpinging photons with all equal energy so to make a spectrum.