Technonolgies for the CLIC tracker

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on behalf of the CLICdp collaboration

12th Trento Workshop on Advanced Silicon Radiation Detectors
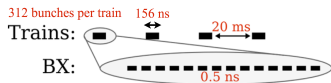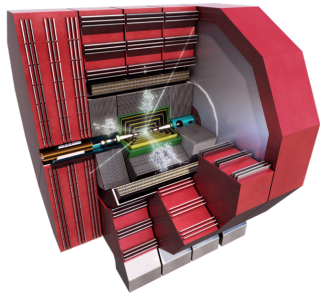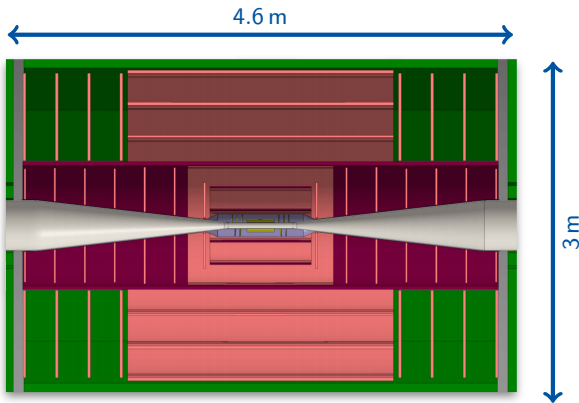Trento, Italy
20. − 22. February 2017

Outline

- CLIC tracker requirements, detector layout
- Investigated monolithic technologies
- Examples of ongoing analyses
  - ALICE investigator HR CMOS test chip
  - Cracow SOI chip

Detector requirements - experimental conditions

- All-silicon tracker, $1\,\%X_0 - 1.5\,\%X_0$ per detection layer
- Good momentum resolution, $\sigma_{p_T}/p_T^2 = 2 \times 10^{-5}\,\text{GeV}^{-1}$
  - 4 T field, 1.5 m tracker radius
  - 7 µm single point resolution
- No trigger, full readout of 156 ns bunch train
- Beam induced background:
  - High rate - 3 $\gamma\gamma \rightarrow$ hadron events per bunch crossing at 3 TeV
  - Requires high readout granularity
  - Requires precise timing ≤ 10 ns
- Relaxed radiation environment:
  - 10^{-4} LHC levels

312 bunches per train   156 ns
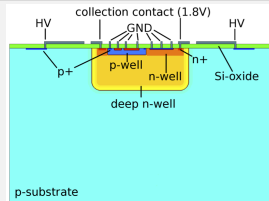
Trains: 20 ms

BX: 0.5 ns

Tracking detector layout

- ▶ Barrel: 3 inner, 3 outer layers
- ▶ Endcaps: 7 inner (6 short strips, 1 pixel), 4 outer discs per side
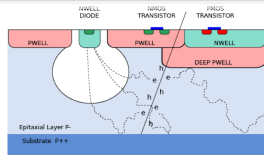- ▶ $\sim 100\,\text{m}^2$ active area $\rightarrow$ monolithic detector advantageous

Technology options under study

HV-CMOS

- Large deep n-well for signal collection
- PMOS transistors embedded in n-well
- Drift and diffusion
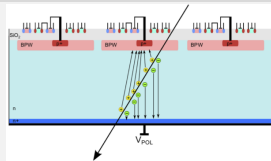- $\rightarrow$ Covered in previous talk by D. Hynds

HR-CMOS

W. Snoeys et al.

- Small n-well for signal collection
- PMOS/NMOS transistors embedded in n/p-wells
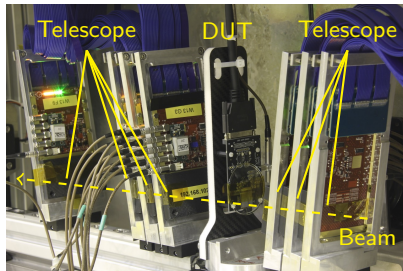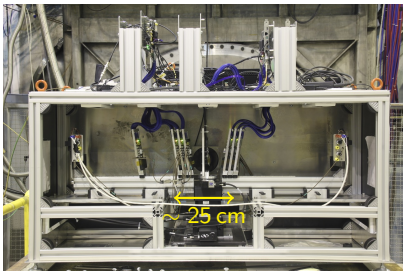- Recent process modification $\rightarrow$ full-depletion possible

SOI

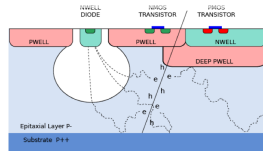- High-resistivity sensor wafer, CMOS electronics separated by oxide layer
- Full depletion

Timepix3 Telescope

- Operated in H6 beamline at CERN SPS, 120 GeV pions
- 7 planes of Timepix3 assemblies (300 μm thick, 55 μm pitch, p-in-n sensors) for reference tracking
- Spatial resolution: $\sim 2\,\mu m$ on DUT
- Timing resolution: $\lesssim 1\,ns$ on DUT, each pixel hit is time tagged with 1.56 ns clock
- Rate: $\sim 1 \times 10^6$ Tracks/s

ALICE Investigator

- TowerJazz 180 nm High-Resistivity CMOS
    - 15 µm to 40 µm thick / 1 kΩ cm to 8 kΩ cm epitaxial layer
    - Full CMOS: n-wells shielded by deep p-wells
- ALICE Investigator analog test chip
    - 134 pixel matrices, each 8×8 pixels
    - Pixel sizes: 20x20 µm^2 to 50x50 µm^2
    - Access to time resolved waveform directly after the first amplifier
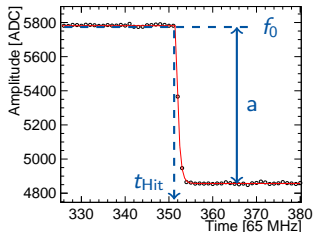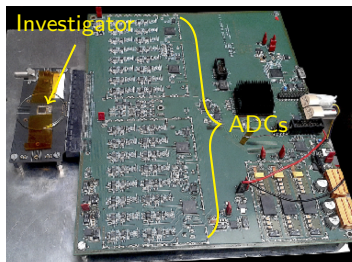   - Select one matrix, readout of each pixel with external sampling ADCs

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ALICE Investigator

NIM A 765 (2014) 177

Event reconstruction
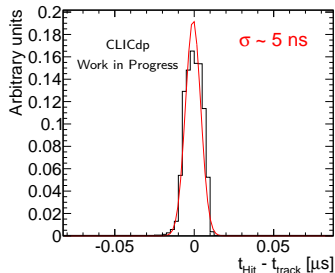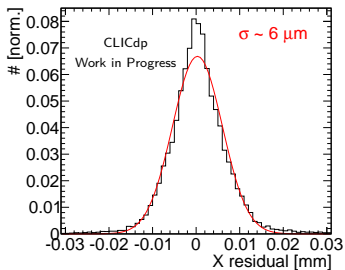
- Readout designed by ALICE
- 64 external sampling ADCs, one per pixel
- 1024 samples/frame/pixel, 65 MHz sampling
- Readout is triggered, if at least one pixel passes a predefined threshold
- Synchronized to telescope data stream
- Fit waveform to extract signal, absolute time and rise time

$$f(t) = \begin{cases} f_0 & t < t_0 \\ f_0 + a \left(\exp(-\frac{t - t_{\text{Hit}}}{\tau}) - 1 \right) & t \geq t_0 \end{cases}$$
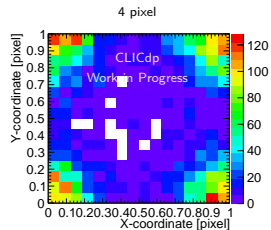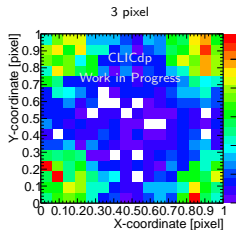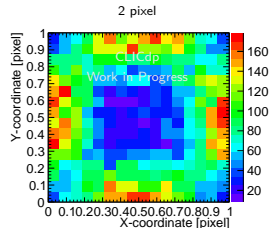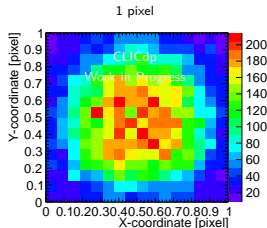
Resolution in space and time

▶ 28 μm pixel size, 6 V bias, modified process

CLICdp Work in Progress — X residual [mm], σ ~ 6 μm

CLICdp Work in Progress — $t_{Hit} - t_{track}$ [μs], σ ~ 5 ns

▶ Compare extrapolated track impact position to reconstructed position

▶ Spatial resolution ∼ 6 μm, telescope resolution not unfolded

▶ Compare extrapolated track time to reconstructed time

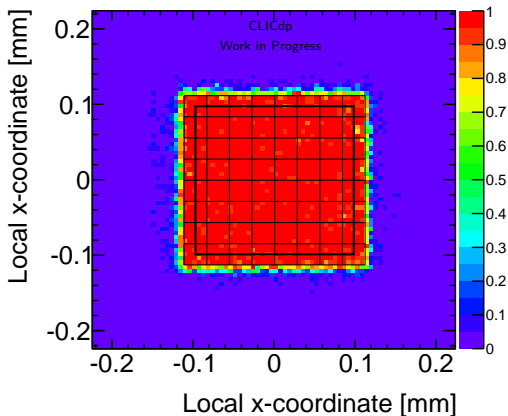▶ Timing resolution ∼ 5 ns, dominated by the 65 MHz sampling of the readout

Cluster size

- 28 μm pixel size, 6 V bias, modified process
- Good pointing resolution of the telescope allows for sub-pixel resolved studies
- Track intercept in pixel cell for different cluster sizes
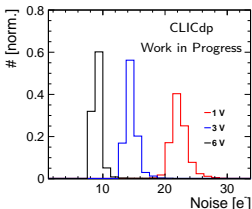- Charge sharing to neighboring pixels at the edges and corners of the pixel cell

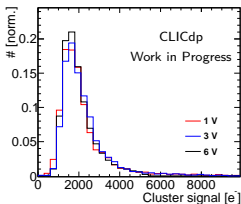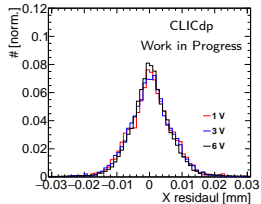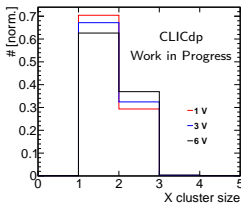# Efficiency

- 28 µm pixel size, 6 V bias, modified process
- Detection efficiency within the active time-period of the pixel matrix: 99.3 %
- Safety margin to the edges of 0.5 pixels to avoid edge effects
- Threshold: S/N>8

Bias dependence
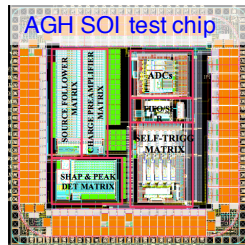
- 28 μm pixel size, modified process

- Cluster size only slightly affected by bias voltage

- Calibrated cluster signal unchanged

- Spatial resolution unchanged

- Noise is decreasing with bias voltage, S/N is increasing
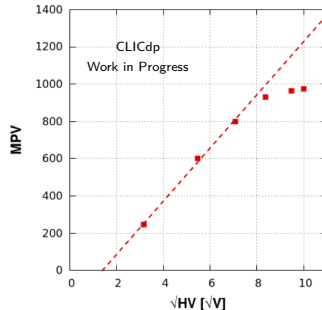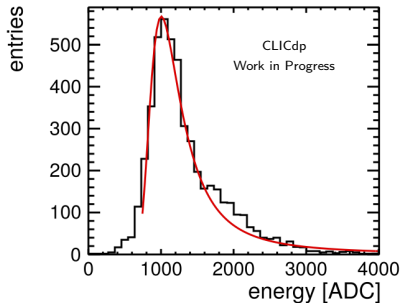
Cracow SOI chip in Lapis 200 nm SOI

- ▶ CMOS sensor on Silicon On Insulator (SOI) wafers
- ▶ Electronics on low resistivity wafer, separated by buried oxide from fully depleted high-resistivity sensing layer
- ▶ Technology allows to fabricate thin sensors - down to 50 µm

- ▶ Test-chip from AGH Cracow
  - ▶ Different pixel sizes ($\geq$ 30 x 30 µm^2) and readout techniques (source follower, charge preamp., self-triggering, ...)
- ▶ In this study focus on source follower matrix on FZ-n wafer
- ▶ Rolling shutter readout (integration time for one frame: 150 µs)

AGH SOI test chip

SOI results

▶ FZ-n, 500 µm thick, source follower matrix, 30 µm pixel size
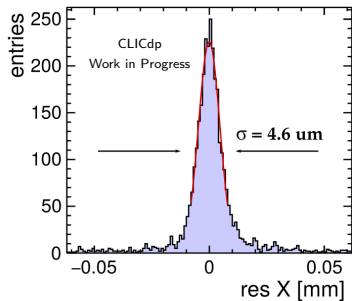

CLICdp
Work in Progress

CLICdp
Work in Progress

▶ Full depletion around 80 V

▶ Energy spectrum after clusterization

▶ All hits, no track matching

SOI results

▶ FZ-n, 500 μm thick, source follower matrix, 30 μm pixel size

▶ Spatial resolution $\sim 4.6\,\mu m$ at 90 V, telescope resolution not unfolded

▶ Benefit from charge sharing in thick sensor

▶ Resolution is improving, as sensor volume gets depleted

Summary & outlook

- Investigating various fully integrated CMOS technologies for the CLIC tracker
    - HV-CMOS studied in capacitively coupled devices ($\rightarrow$ talk by D. Hynds)
    - ALICE Investigator HR-CMOS test chip
    - SOI pixel prototype chip
- Ongoing: comparative study for a chip design focused on the CLIC tracker, aim is to find a suitable technology and design for a monolithic prototype chip
- In parallel: new SOI prototype with larger and more uniform matrix has been fabricated and will be tested in beam later this year
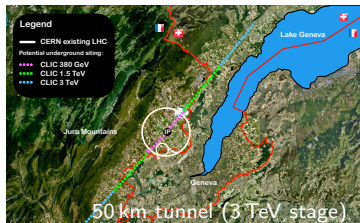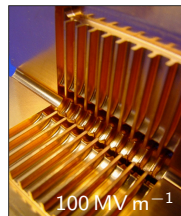
Backup

CLIC

- ► CLIC (Compact LInear Collider): linear e^+e^- collider proposed for the post HL-LHC phase
- ► Energy range from a few hundred GeV up to 3 TeV, staged construction
- ► Physics goals:
  - ► Precision measurements of SM processes (Higgs, top)
  - ► Precision measurements of new physics potentially discovered at 14 TeV LHC
  - ► Search for new physics: unique sensitivity to particles with electroweak charge
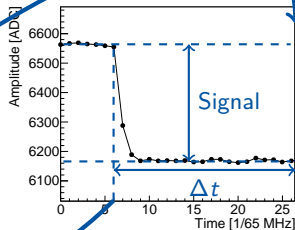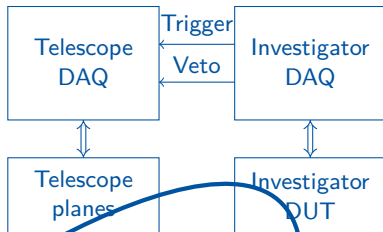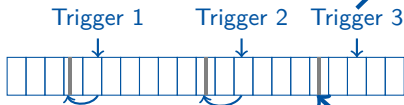
Possible layout near Geneva

50 km tunnel (3 TeV stage)

CLIC accelerating structure

100 MV m^{-1}

ALICE investigator: Telescope integration

- 1024 samples/frame/pixel, 65 MHz sampling, self-triggered readout

- Readout is triggered, if at least one pixel passes a predefined threshold

- Synchronization of clock domains not easily possible

- Timetag triggered frame via trigger pulse fed to telescope TDC at the end of frame

- Use TDC packet in tel. data stream + relative time in investigator frame to assign exact time to hit

Trigger 1   Trigger 2   Trigger 3

Cracow SOI chip: Telescope integration

- Source follower matrix investigated in testbeam, rolling shutter readout, 150 µs integration time

- SOI DAQ takes clock and T0, marks begin of readout frame

- Hit can end up in the current or the next frame, depending on its position relative to the rolling shutter

- Analysis copies several frames overlaid into each telescope event