OKMETIC

Novel MCz-silicon material and application for the radiation detection community

Alexandra Junkes, Jenni Honkanen, Jari Paloheimo, Janne Pekuri

12th Trento Workshop – February 22nd 2017

Content

- Okmetic
- Advanced-MCz
- Okmetic Applications

Okmetic: leading supplier of high-performance silicon wafers

Key figures	2016
Net sales	75.7 MEUR
Operating profit*	7.9% of net sales
Personnel	377

• 2016 are preliminary and have not yet been approved by the Board or audited by an external auditor.

Vantaa plant, Finland

- Crystal growing
- Discrete&Analog wafers: 150-200 mm
- Sensor wafers: 100-200 mm
- SOI wafers 100-200 mm
- Capacity: 250 kpcs/month

Fab lite capacity

- Umesato, Japan
- Ferrotec, Shanghai
- GlobalWafers / SST, Shanghai
- GlobalWafers, Japan
- Capacity: 300 kpcs/month

Silicon wafers for 100 – 200 mm volume manufacturing

Wafer platforms:

- SSP (single side polished) wafers
- DSP (double side polished) wafers
- SOI (Silicon-On-Insulator) wafers, large product family

Application examples:

- MCz-NTD wafers for IGBT manufacturing
- High resistivity wafers up to and beyond 5 kOhm cm
- Low resistivity wafers below 1 mOhm cm
- Silicon substrates for GaN applications

Complete set of 100-200 mm wafers for Sensor and Discrete&Analog markets

OKMETIC

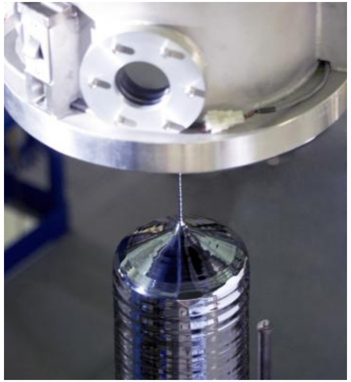
Okmetic's Magnetic Czochralski Silicon

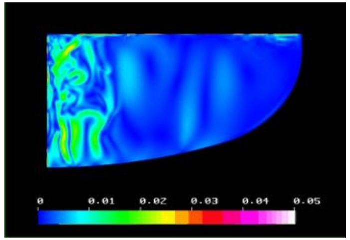
2016 A-MCz process

2003 CERN radiation hard particle detectors on Okmetic MCz

1991 – MCz for MEMS

1983 -1989 – First MCz demonstrations





MCz advantages

- Enables high resistivity by lower Oxygen concentration compared to standard Cz
- Availability of large diameter and <111> oriented ingot
- Better slip resistance and mechanical properties compared to FZ
- Radiation tolerance compared to FZ

Ultra low O_i-MCz for high resistivity wafers

MCz: p-type resistivities up to 5000 Ωcm

- Improved thermal stability of resistivity compared to regular Cz
- Thermal donor generation creates challenge for some sensor fabrication processes

Advanced MCz: resistivity up to 10000 Ωcm and beyond

- New level of resistivity for MCz
- Still better slip resistance and radiation hardness compared to FZ
- Thermal donor generation largely suppressed
- Enables completely new designs and capabilities for device designers

Oxygen in High Resistivity Silicon – Resistivity Control

- **High Resistivity MCz Silicon contains** oxygen
  - Coming from quartz crucible used in the crystal puller
  - > below 10 ppma for typical MCz ingots
- At elevated temperatures (T > 400 °C) **Oxygen atoms become mobile** and diffuses in the lattice.
- Between 400 °C < T < 500 °C the probability for **dimer or oxygen cluster formation** is very high
- Clusters of oxygen atoms can become electrically active → **thermal donors (n type doping)**

520 Handbook of Semiconductor Silicon Technology

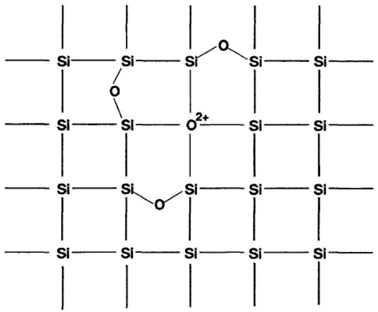
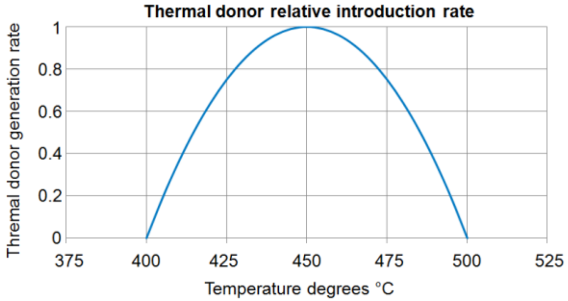


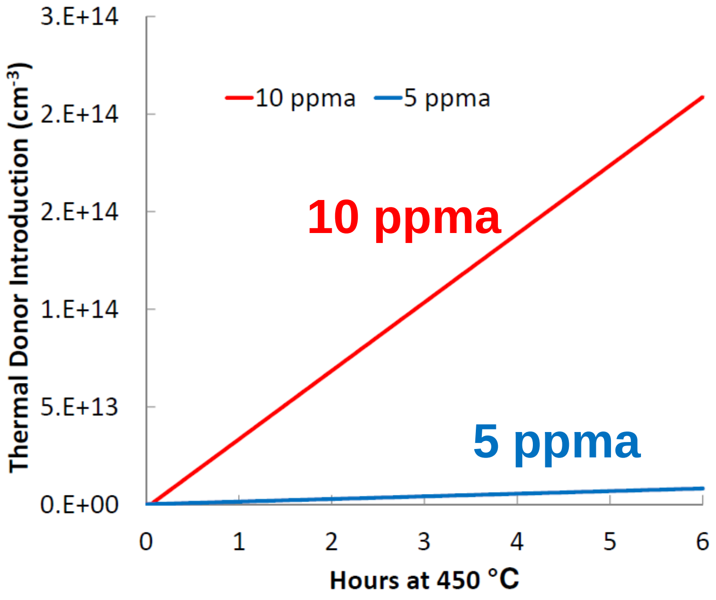
Figure 33. Structural model for the oxygen thermal donor (after 97).



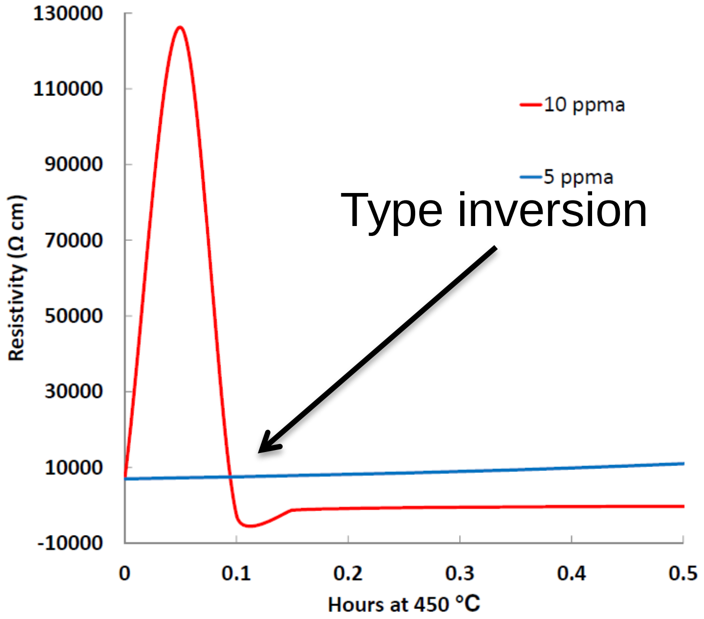
OKMETIC

Worst-Case-Scenario: Resistivity Shift at 450 °C

TD introduction at 450 °C

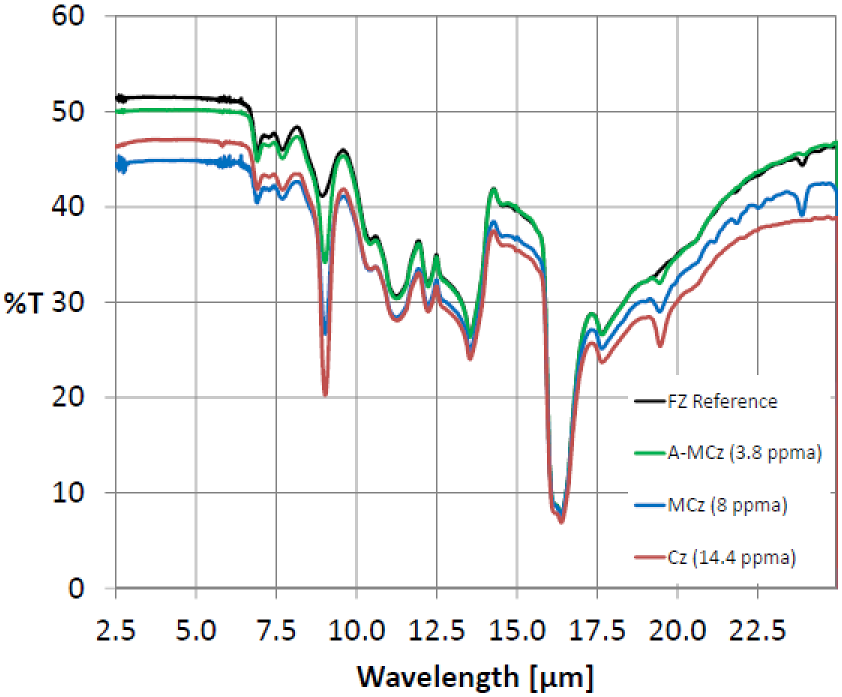


Resistivity shift at 7 kΩ cm



OKMETIC

FTIR Transmittance vs. O_i-Content



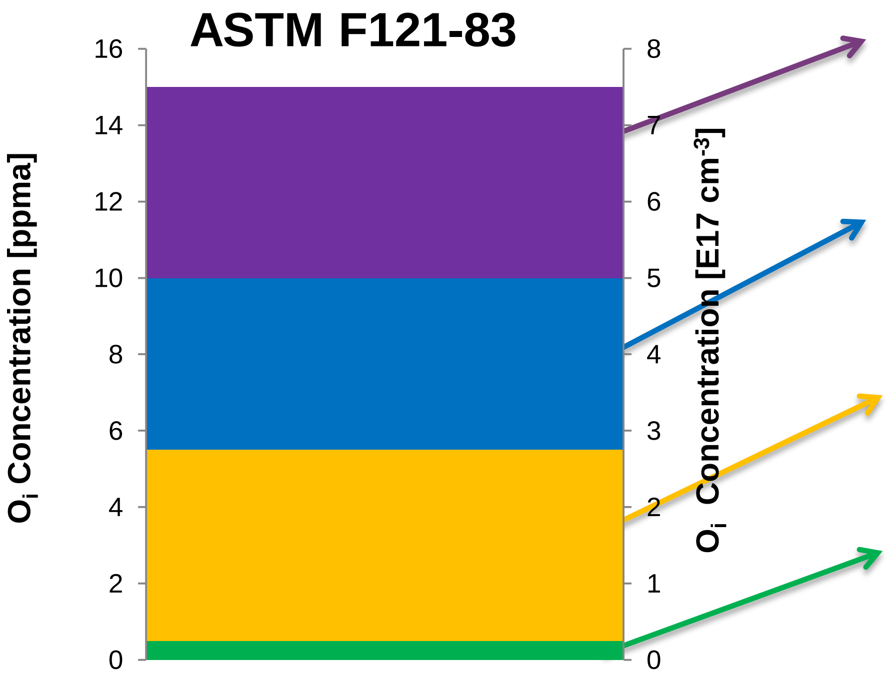
Influence of O_i visible at 9 um
Low Oxygen MCz similar to FZ

Ingot resistivities:

1. High Resistivity for FZ, A-MCz and MCz
2. Cz: 1-10 Ω cm

OKMETIC

Selecting Si-ingot material for each application



Standard Cz
- Good slip resistance and radiation hardness
- Suitable for internal gettering
- Good for standard and low resistivity

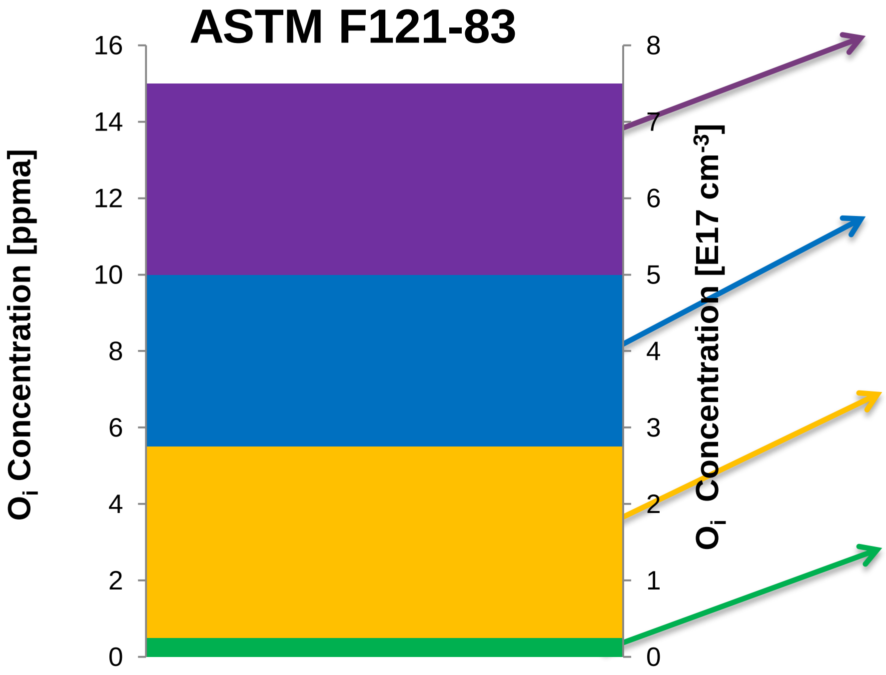
MCz
- Good slip resistance and radiation hardness
- Suitable for high resistivity
- Low Oi, Low BMD counts

Ultra low Oi A-MCz
- Better slip resistance and radiation hardness compared to FZ
- Suitable for ultra high resistivity
- Very low Oi. No BMDs.

FZ
- Poor slip resistance and radiation hardness
- No BMDs.
- Suitable for ultra high resistivity
- High cost and limited availability especially in 200 mm

OKMETIC

Selecting Si-ingot material for each application



Standard Cz
•Good slip resistance and radiation hardness
•Suitable for internal gettering
•Good for standard and low resistivity

MCz
•Good slip resistance and radiation hardness
•Suitable for high resistivity
•Low Oi, Low BMD counts

Ultra low Oi A-MCz
•Better slip resistance and radiation hardness compared to FZ
•Suitable for ultra high resistivity
•Very low Oi. No BMDs.

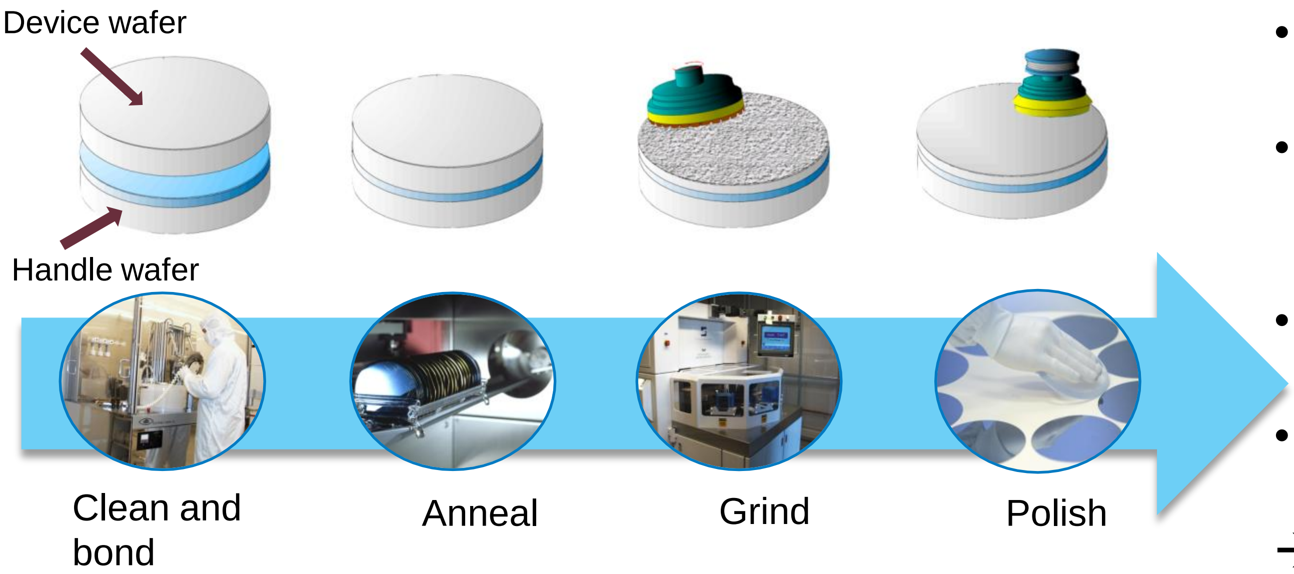
Optimal for HL-LHC Sensors

FZ
•Poor slip resistance and radiation hardness
•No BMDs.
•Suitable for ultra high resistivity
•High cost and limited availability especially in 200 mm

OKMETIC

Applications

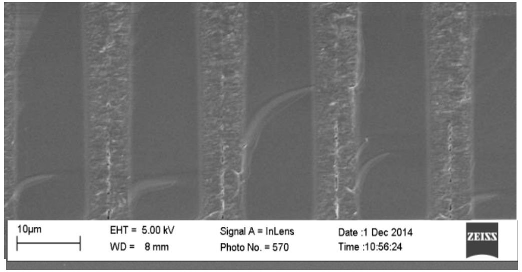
Sensors from SOI Wafers



- Thin active device layers possible
- Handle wafer electrically isolated from device wafers
- Handle can be etched, ground…
- Wafers fully CMOS compatible

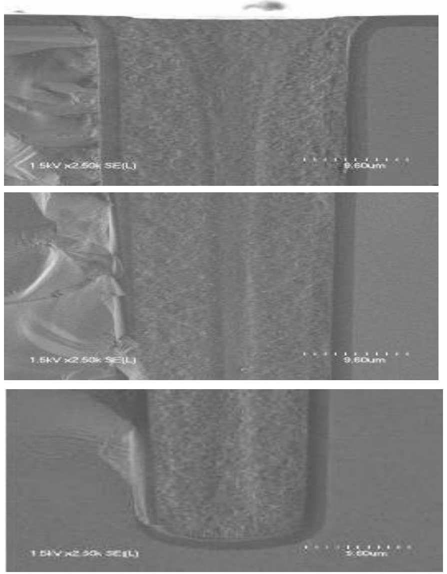
→ Applicable also for HV applications

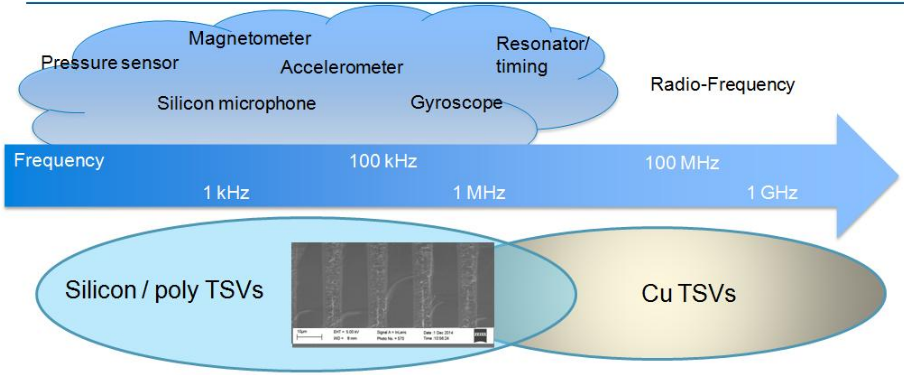
Wafers with Through-Silicon Vias (TSV)



Interconnect characteristics achieved with the etched via with doped polysilicon filling

- Capacitance of <1 pF
- Resistance of a few tens of Ohms
- Breakdown voltage in excess of 100V
- Leakage current below 5 pA@100V





OKMETIC

Summary

Advanced MCz is a very good match for particle sensor applications

Contact us

www.okmetic.com

sales@okmetic.com

communications@okmetic.com

Okmetic Oy
P.O.Box 44, FI-01301 Vantaa, Finland
Piitie 2, FI-01510 Vantaa, Finland
Telephone +358 9 502 800
Fax +358 9 5028 0500

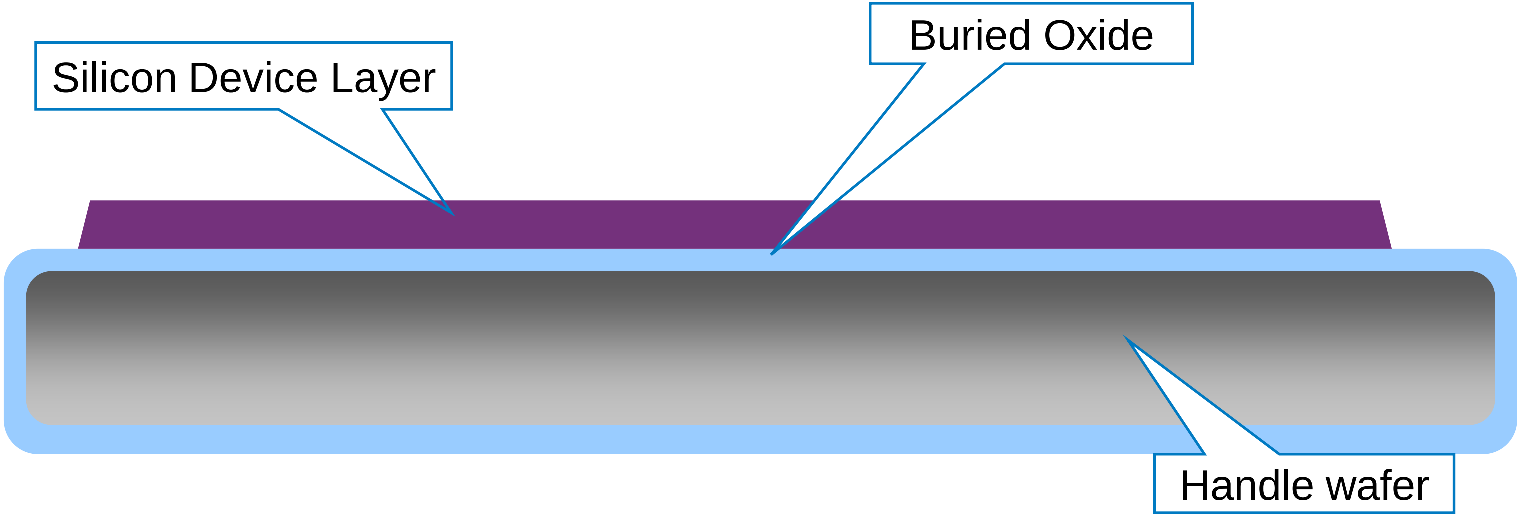
Okmetic Inc.
307 South Jupiter Road, Suite 210
Allen, TX 75002, USA
sales.usa@okmetic.com

Okmetic K.K.
Sunrise Mita 8F 3-16-12,
Shiba Minato-ku, Tokyo
105-0014 Japan
Telephone +81 3 3798 1400
Fax +81 3 3798 1402

Okmetic Ltd.
Level 3 A, Causeway Corner
18 Percival Street, Causeway Bay,
Hong Kong
Telephone +852 3656 7858
Fax +358 9 5028 0200

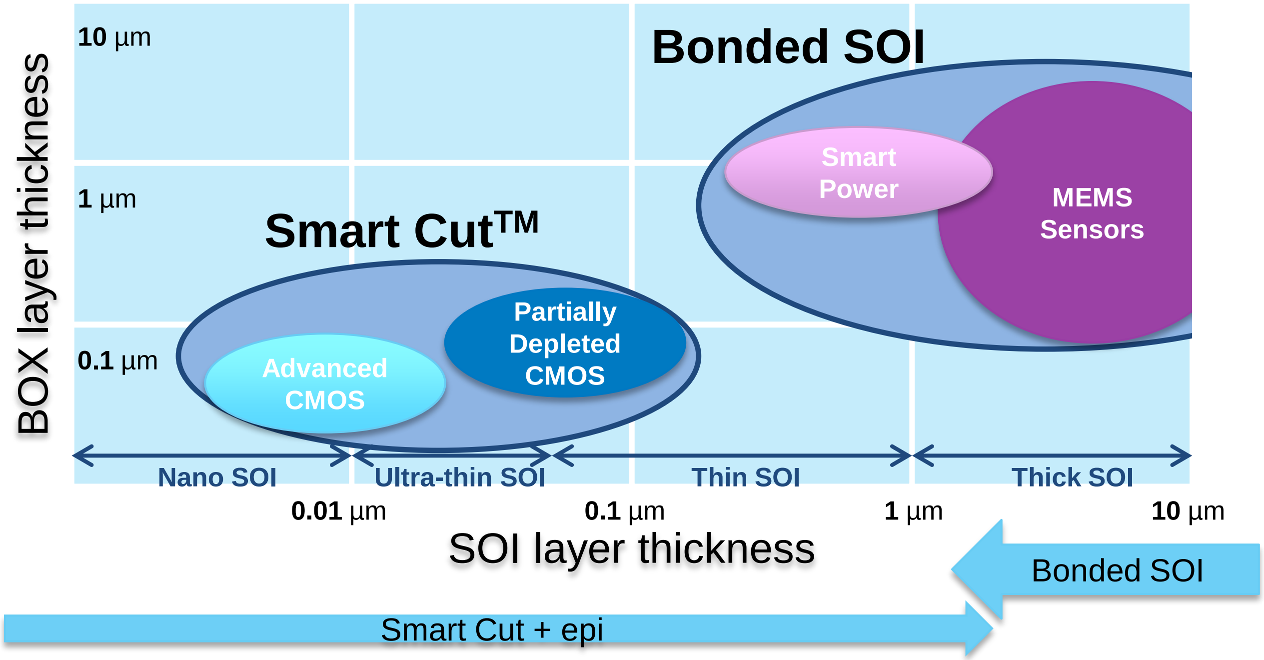
SOI Wafers (Silicon On Insulator)

- Improved electric properties
- Advanced design of sensors



OKMETIC

SOI applications grouped by production method (Smart Cut vs. Bonded SOI)



Redrawn from MEMC's original

OKMETIC

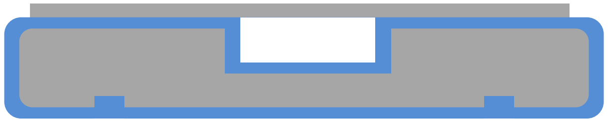
Okmetic's Bonded SOI (BSOI) Product Family

BSOI

Fully customizable with starting materials from in-house crystal growth and wafering

C-SOI

Wafers with pre-etched cavities



0.3-SOI

Improved device layer thickness tolerance ±0.3 µm

BSOI

E-SOI

Enhanced uniformity wafers with device layer thickness tolerance ±0.1 µm

D-SOI

Two device and buried oxide layers with different thicknesses

L-SOI

Low resistivity SOI device layers

Typical SOI Wafer Specifications

Growth method:	**Cz, MCz**
Crystal orientation:	<100>, <111>, <110>
Diameter:	100, 150, 200 mm
Type & Dopant:	P: boron N: antimony, arsenic, phosphorous
Resistivity:	< 0.0015 to > 1000 Ohmcm
Thickness:	*SOI layer:* from 2 µm to > 200 µm, tolerance ±0.5µm, standard BSOI tolerance ±0.3µm, 0.3-SOI tolerance ±0.1µm, E-SOI *Handle wafer:* from 300 µm to 950 µm, typical 380 µm back surface polished or etched
Buried oxide:	Type: thermal oxide Thickness: from 500 nm to 4 µm