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TOFFEE a fully custom readout ASIC for timing applications with UFSD

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Time tagging is becoming a fundamental tool for the future of High Energy Physics, where the high luminosity will introduce hundreds of overlapping events (pile-up) making really tricky to take and analyse data. This is the case of the high luminosity LHC, where the expected number of events per bunch crossing is ˜150-200. A possible strategy for pile-up mitigation consists in exploit time tagging to distinguish events overlapping in space but separated in time by few tens of picoseconds. For this reason, the so called Ultra Fast Silicon Detectors (UFSD) and a fully custom readout ASIC have been developed. The ASIC is called TOFFEE and is designed in a standard 0.11 μm CMOS technology. The chip has been optimized for the readout of signals produced by UFSD 50 μm thick sensors to cope with the CMS-TOTEM Precision Proton Spectrometer (CT-PPS) time resolution requirement of 30 ps per detector plane. TOFFEE consists of 8 independent channels, each with a charge sensitive amplifier (CSA), a single threshold discriminator, a stretcher and a LVDS driver. The readout chain has been designed to work with the High Precision TDC (HPTDC) which requires a minimum pulse width of 5 ns. This talk reports the design and the first measurement results of TOFFEE.

TRACK

Electronics

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