Development of HV-MAPS detectors at the University of Liverpool

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Aim and collaboration

- **R&D of HV-MAPS detectors** for the HL-LHC ATLAS upgrade and other future HEP experiments

- Many people from many different institutes are involved:
  - BNL → F. Lanni
  - CERN
  - IFAE → R. Casanova, E. Cavallaro, F. Förster, S. Grinstein, S. Terzo
  - KIT → R. Blanco, F. Ehrler, R. Leys, I. Peric
  - RD50 collaboration
  - University of Bern → M. Weber
  - University of Geneva → M. Benoit, F. Guezzi Messaoud, G. Iacobucci
  - University of Heidelberg → A. Schöning
  - University of Liverpool → M. Buckland, G. Casse, L. Meng, S. Powell, E. Vilella, J. Vossebeld, S. Wonsak, C. Zhan
**HV-CMOS chips**

**H35DEMO - Features:**
- ams 0.35 µm HV-CMOS (H35)
- Different matrices (2 CCPD and 2 monolithic) and test structures
- Pixel size is 50 µm x 250 µm (for compatibility with FE-I4)
- Resistivities: 20 Ω·cm, 80 Ω·cm, 200 Ω·cm and 1k Ω·cm
- Delivered in December 2015 (eng. run)

**Features:**
- LFoundry 150 nm HV-CMOS
- Contributions from IFAE, KIT, Uni. Geneva and Uni. Liverpool
- Different matrices (1 CCPD and 5 monolithic) and test structures
- Resistivities: 100 Ω·cm, 500-1.3k Ω·cm, 2k-2.5k Ω·cm and 3.6k-3.9k Ω·cm
- Submitted in August 2016 (MPW)
- ASICs just delivered

**Features:**
- ams 180 nm HV-CMOS (H18)
- Different matrices (1 CCPD and 3 monolithic, it includes MuPix8), CLICpix and test structures
- Submitted in January 2017 (eng. run)
- ASICs will be delivered in ~April 2017
LFoundry HV-MAPS chip

Areas from top to bottom:

1) Test structures
   - TCT/e-TCT
   - sensor capacitance measurement
   - very fast measurements

2) Non-ATLAS matrix

3) Matrix of HV-MAPS pixels with FEI3-like readout
   - 40 rows x 78 columns of pixels
   - pixel area is 50 µm x 50 µm
   - analog and digital readout electronics are embedded inside the pixel area
   - analog readout electronics → preamplifier, shaper and discriminator
   - digital readout electronics → electronics to process the output of the discriminator,
     2 8-bit DRAM memories to store the TS and
     1 8-bit DROM memory to store the pixel address
   - The FEI3-like readout was designed to study very small pixels with all the readout electronics integrated inside the pixel area and to qualify this technology for the HL-LHC upgrade
   - No backside biasing option
   - Detector thickness is 280 µm
LF2 - Pixel cross-section

- The sensing diode is a p-substrate/DNWELL junction
- The DNWELL can be isolated from NWELLs/PWELLs thanks to the PSUB layer
- Therefore, it is possible to have fully CMOS electronics inside the pixel area
- In our case, we have multiple NWELLs and PWELLs:
  - 1 NWELL/PWELL for the CSA and the shaper
  - 1 NWELL/PWELL for the CMOS discriminator
  - 1 NWELL/PWELL for the digital readout
  - 1 NWELL for the pMOS transistors of the sensor bias circuit (this NWELL is connected to the DNWELL)
- The DNWELL is biased through an n⁺/NWELL/NISO structure
The analog readout is based on a biasing circuit, CSA, low-pass/high-pass filters and discriminator. The CSA is a single folded Cascode with pMOS input transistor. It has a constant value $C_{FB}$ (1.2 fF) and programmable discharging current. The baseline (BL) voltage and low-pass/high-pass filters are adjustable. The discriminator has a local 4-bit DAC to compensate for offset variations. The signal amplitude is between ~50 mV (for 600 e⁻) and ~600 mV (for 6000 e⁻). The gain is 105 e⁻/µV. The rise time is ~20-30 ns and fall the time is ~100-600 ns (depending on feedback capacitor type and collected charge). Total power consumption per pixel is ~27 µW (pre-amplifier current is <10 µA).
LF2 - Pixel flavours

with MIM capacitance

with diffusion-type capacitance
The **digital readout** is based on:

- **Two 8-bit DRAM memories** that continuously store two time stamps (Leading Edge, Trailing Edge)
- **One 8-bit ROM memory** to store the pixel address
- **Electronics (edge detector)** to process the output of the discriminator and tell when the LE and TE have to be stored

- Pixel receives an 8-bit Gray encoded TS running at 40 MHz
- Hit flag register to avoid processing new events until the current one has been read
- Priority encoding → Pixel with asserted flag and lowest address has the highest priority
- One matrix with **4 different pixel flavours** (with MIM/diffusion feedback capacitance, with linear/enclosed transistors) → For comparison purposes
- Configuration of global DACs and pixels is done via registers
- Possibility to inject a test pulse to each pixel
- Test features → Output of each pixel SF and discriminator can be monitored (one pixel at a time)
- Pixel output is sent to EOC via bus and read out using CU (running at 640 MHz) and LVDS pad
- Test set-up development is on-going
**LF2 - Test structures**

A) TCT/e-TCT
3 x 3 matrix of 50 µm x 50 µm
HV-CMOS pixels without electronics

B) TCT/e-TCT
2 x 3 matrix of 75 µm x 75 µm
HV-CMOS pixels without electronics

C) Fast measurements (with a laser)
3 x 3 matrix of 50 µm x 50 µm
HV-CMOS pixels

D) Sensor capacitance measurement
1 single pixel with 50 µm x 50 µm
1 single pixel with 75 µm x 75 µm

E) 2 avalanche photodiodes for I-V measurements
LF1 and ams 180 nm - Test structures

A) TCT/e-TCT → 3 x 3 matrix of 50 µm x 50 µm HV-CMOS pixels without readout electronics
B) TCT/e-TCT → 3 x 3 matrix of 75 µm x 75 µm HV-CMOS pixels without readout electronics
C) Fast measurements → 3 x 3 matrix of 50 µm x 50 µm HV-CMOS pixels
D) Sensor capacitance measurement
   1 single pixel with 50 µm x 50 µm
   1 single pixel with 75 µm x 75 µm
E) 2 avalanche photodiodes for I-V measurements

A) TCT/e-TCT → 3 x 3 matrix of 33 µm x 125 µm HV-CMOS pixels without readout electronics
B) Sensor capacitance measurement → 1 single pixel with 33 µm x 125 µm (simple pixel)
C) Sensor capacitance measurement → 1 single pixel with 33 µm x 125 µm (pixel with TW compensation)
D) Fast measurements → 3 x 3 matrix of 33 µm x 125 µm HV-CMOS pixels
Main features:
- ams 0.35 µm HV-CMOS (H35)
- submission through an engineering run
  - submission in October 2015
  - wafer production finished in December 2015
- different substrate resistivities to improve SNR
  - 20 Ω·cm (standard), 80 Ω·cm, 200 Ω·cm, 1k Ω·cm

Areas (from top to bottom):
- standalone nMOS matrix
  - digital pixels with in-pixel nMOS comparator
  - standalone readout
- analog matrix (2 identical arrays)
  - different flavours
- standalone CMOS matrix
  - analog pixels with off-pixel CMOS comparator
  - standalone readout
- All pixels are 50 µm x 250 µm for compatibility with FEI4
H35DEMO - e-TCT measurements

No circuitry or metal layers on top of the sensing diodes

Central pixel

Measured results:

ρ=80 Ω·cm, d~35 µm @ -170 V
ρ=200 Ω·cm, d~45 µm @ -140 V

e-TCT set-up:
H35DEMO - e-TCT measurements

- Samples of the **H35DEMO in the 1k Ω·cm resistivity** were **backside processed**:
  - thinning to 100 µm
  - backside p⁺ implantation with boron
  - thermal annealing
  - backside metallization

  to allow backside biasing and achieve a **stronger, more uniform electric field in the sensing volume**
H35DEMO - e-TCT measurements

No circuitry or metal layers on top of the sensing diodes

Central pixel

e-TCT set-up:

Measured results:

Backside biasing
Fully depleted @ -40 V !!

Sensor surface

ρ=1k Ω·cm, d~100 µm @ -40 V

Topside biasing

ρ=1k Ω·cm
<table>
<thead>
<tr>
<th>Test structure</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test structure 1</td>
<td>Simple CMOS capacitors to study oxide thickness</td>
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<tr>
<td>Test structure 2</td>
<td>10 x 10 matrix of very small pixels with passive readout</td>
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<tr>
<td>Test structure 3</td>
<td>10 x 10 matrix of very small pixels with 3T-like readout</td>
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<tr>
<td>Test structure 4</td>
<td>Small matrix of pixels for TCT, e-TCT and TPA-TCT measurements</td>
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<td>Test structure 5</td>
<td>Single pixels for sensor capacitance measurements</td>
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<td>Test structure 6</td>
<td>...</td>
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</tbody>
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**Design effort:**

*IFAE*
- R. Casanova
- *Uni. Barcelona*
- O. Alonso

*Uni. Liverpool*
- S. Powell
- E. Vilella
- C. Zhang

Scope for further design contributions...
Summary

- Several HV-CMOS submissions in 2016:
  - 10 mm x 10 mm HV-MAPS ASIC in LFoundry 150 nm via MPW
  - 5 mm x 5 mm HV-MAPS ASIC in LFoundry 150 nm via MPW
  - 21.3 mm x 22.6 mm HV-MAPS ASIC in ams 180 nm via engineering run

- The fabricated ASICs are expected during the first quarter of 2017
  - PCBs to design
  - Firmware to write
  - Many many measurements to be done

- H35DEMO measurements are on-going

- Working towards a new HV-MAPS submission within the RD50 collaboration

Thank you for your attention!