Results from CHIPIX65 Prototype of a New Generation Pixel Readout ASIC in 65 nm CMOS for HL-LHC experiments

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12th Trento Workshop on Advanced Silicon Radiation Detectors

Feb 21, 2017 - Trento, Italy
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Goals:

- development of an innovative CHIP for a PIXEL detector at extreme rates and radiation at HL-LHC conditions using a CMOS 65 nm technology for the first time in HEP community
- an efficient propagation across INFN of CMOS 65 nm technology (Bari, Lecce, Milano, Padova, Pavia, Perugia, Pisa and Torino groups)
- close synergy with CERN RD53 international collaboration

Designed to be compliant with the expected requirements of HL-LHC pixel detectors:

- 40 MHz bunch crossing frequency
- 50 \( \mu m \times 50 \mu m \) pixel size, large chips \( \sim 2 \text{ cm} \times 2 \text{ cm} \)
- up to 200 event pile-up, 3 GHz/cm\(^2\) hit rate, 75 kHz/pixel particle rate
- 1 MHz trigger rate, 12.5 \( \mu s \) trigger latency
- low power consumption \(< 0.55 \text{ W/cm}^2\), 10 \( \mu \text{W/pixel}\)
- hit efficiency \(> 99\%\) at 3 GHz/cm\(^2\)
The purpose of the CHIPIX65 demonstrator is to satisfy these requirements as a first intermediate step towards full-scale RD53A prototype:

- 64×64 pixel matrix, embedding two different Analog Front End (AFE) designs working in parallel
  - synchronous architecture (Torino INFN)
  - asynchronous architecture (Pavia INFN)

- design and implementation of a novel 4×4 region-based digital architecture for latency buffering and trigger matching

- FIFO-based readout architecture, SPI-based chip configuration
  - support for triggerless, triggered and scan-chain operations

- integration of available silicon-proven IP-blocks designed for RD53
  - bandgap voltage reference (Pavia INFN)
  - SLVS transmitters/receivers (Pisa INFN)
  - high-speed SER (Pisa INFN)
  - 10-bit biasing DAC (Bari INFN)
  - 12-bit monitoring ADC (Bari INFN)

- usage of the modified CERN rad-hard I/O library
1. 32×64 pixels with synchronous FE architecture
2. 32×64 pixels with asynchronous FE architecture
3. replicated bias cells with current mirrors
4. 10-bit biasing DACs
5. bandgap voltage reference
6. 12-bit monitoring ADC
7. readout/configuration digital block and high-speed serializer at the chip periphery
8. SLVS transmitters/receivers and I/O cells

3.5 mm × 5.1 mm
Synchronous front-end architecture

Torino INFN design group:

- telescopic-cascode CSA with Krummenacher feedback for linear Time-over-Threshold (ToT) charge encoding
- synchronous hit discriminator with track-and-latch voltage comparator
- threshold trimming by means of autozeroing using capacitors
- 40 MHz 4-bit ToT or 5-bit fast ToT counting with latch turned into a local oscillator (100-900 MHz)
- efficient self-calibrations can be performed according to online machine operations
- successfully tested (also after irradiation) using dedicated mini@sic small-prototypes
Asynchronous front-end architecture

Bergamo/Pavia INFN design group:
- folded-cascode CSA with Krummenacher feedback
- fast current comparator
- threshold trimming by means of 4-bit local DAC
- effective 80 MHz 5-bit dual-edge ToT counting at 40 MHz
- successfully tested (also after irradiation) using dedicated mini@sic small-prototypes
Front-end layouts comparison
An innovative region-based digital pixel architecture able to sustain expected data and trigger rates at HL-LHC has been developed for the CHIPIX65 demonstrator:

- pixels arranged into **pixel regions** composed of $4 \times 4$ pixels
- analog front-ends arranged in form of **analog islands** into a **digital sea**
- fully automated synthesis/place-and-route on an entire pixel region (**digital-on-top** approach)
- a common digital logic shared among pixels **stores hits information** for the whole trigger latency, handles the **local configuration**, performs **trigger matching** and sends zero-suppressed hit data to the chip periphery upon a trigger request
All logic design optimizations assessed by means of extensive analytical and physics-driven high-level simulations using the verification environment based on SystemVerilog and Universal Verification Methodology (UVM) classes developed within the RD53 collaboration:

- charge information retrieved by means of ToT encoding using per-pixel 5-bit ripple counters
- unique centralized latency memory shared among 16 pixels (latch-based circular FIFO)
- memory usage optimized without writing unnecessary zeroes according to expected event rates
- data-compression based on priority encoding with ToT words saved for only 6 fired pixels accessing the shared buffer
- binary information always registered for all pixels (hit map)
Digital End-of-Column (EOC)

- **Data readout** based on replicated Macro-Column Drainers (MCDs)
  - generation of **BX timestamp** and **trigger timestamp**
  - implementation of the column-readout protocol
  - buffering of readout data
  - data formatting to high-speed serializer

- **Serial Peripheral Interface (SPI) slave port** for chip configuration and slow control
  - write/read Pixel Configuration Registers (PCR) and Global Configuration Registers (GCR)
  - SER synchronization, ADC and autozeroing control commands

- **Design For Test (DFT) flow** added to readout components
  - scan-chain synthesis for all FSMs
  - scannable shadow-logic inserted around FIFOs (excluded from scan insertion)
all reference voltages/currents required by analogue front-ends in the pixel array internally generated using on-chip programmable DACs
- bias voltages/currents
- global thresholds, calibration

10-bit segmented current-steering DACs
- one global DAC for each analogue voltage/current featuring fine-tuning or programmability requirements

bandgap voltage reference
- well-defined and PVT-independent reference current for current DACs
- on-chip 12-bit ADC for monitoring bias/reference currents and bandgap reference voltage
- all DAC currents are also mirrored and can be probed on a dedicated test pad through multiplexing
  - external high-precision resistor (0.1%, ±25 ppm/°C), 4 different values required
  - 12-bit external ADC and multimeter to calibrate internal ADC
Chip periphery layout
Pre-irradiation test results
Test setup

- chips received back from the foundry at the end of September, 2016
- preliminary tests started in both Torino and Bergamo INFN labs
- fully-digital ASIC/FPGA interface based on FMC
- prototype wire-bonded on a custom test board
- a few test points to monitor global bias voltages/currents
- custom Ethernet/UDP firmware supporting both Virtex-7 and Artix-7 Xilinx FPGA boards
- NI/LabView data acquisition interface supporting all chip operations
Charge-injection characteristics
Calibration DAC

- per-pixel generation of the analog test pulse starting from two well defined DC levels
- charge-injection triggered in selected pixels by a digital switching signal distributed to all pixels
- precise 8 fF per-pixel injection capacitance using MOM cap
- one global 10-bit calibration DAC common to both synchronous and asynchronous pixels
- good agreement between measurements and CAD simulated data
Monitoring ADC

- Calibration voltage fed to monitoring ADC, converted data read back through SPI
- ADC implements a **self-calibration algorithm** to minimize comparator offset (but digital trimming through dedicated configuration registers also supported)
- Linear ADC characteristic, good agreement between measurements and CAD simulated data
- Fully-automated extraction of DNL/INL performance metrics not yet implemented in software
Synchronous FE results
- all pixels tested and fully working
- autozeroing performed each 200 µs
- effective **noise** and **threshold** values determined by means of S-curves
- measurements performed with **charge scans** and **fixed threshold**
- **hit efficiency** recorded for 100 charge-injection pulses
- measured points fitted using an error function (sigmoid)
- noise and threshold values extracted from means and variances distributions
Threshold measurements with autozeroing

- Effective threshold measured for different values of fixed global threshold
- Autozeroing works, residual offset value of about 100 $e^-$ RMS in good agreement with CAD simulations ($\approx 70 e^-$ RMS latch dynamic offset)
- Linear increase as expected
- Threshold-to-charge characteristic from fit
- $\approx 250 e^-$ RMS minimum threshold
Noise measurements

ENC measured for different values of fixed global threshold
- constant behavior with threshold values as expected
- $\text{ENC} \approx 90\,\text{e}^-$ RMS in good agreement with CAD simulations
- low-noise performance assured despite continuous latch and region-logic digital switching activity
Fast Time-over-Threshold (ToT) counting

- very good linearity for the 5-bit fast ToT
- 320 MHz frequency reached for 5 ke⁻
- slope dispersion of about 10% due to mismatches in the analog part, as from CAD simulations
Asynchronous FE results
Untrimmed threshold dispersion and noise

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- **Test setup** just delivered to Bergamo/Pavia INFN group, requiring some firmware modifications to target Xilinx Artix-7 evaluation board (first measurements performed in Torino).
- All pixels tested and fully working.
- \( \approx 450 \text{ e}^- \) RMS untrimmed threshold dispersion, ENC \( \approx 85 \text{ e}^- \) RMS noise before irradiation.
- Good agreement with CAD simulations.
Threshold linearity

- effective threshold measured for different values of fixed global threshold
- linear increase as expected
- threshold-to-charge characteristic from fit
- $\approx 550 \text{ e}^{-}$ RMS minimum threshold
Threshold trimming

- fully-automated calibration procedures for asynchronous pixels not yet supported by DAQ system
- preliminary threshold trimming performed offline
- per-pixel DAC codes extracted from untrimmed S-curves using a set of ROOT macros and then loaded into the chip
- electrical functionality OK, threshold compensation works for all pixels
- $\approx 125$ e$^-$ RMS residual threshold dispersion, still to be optimized (test performed in Torino)
Post-irradiation test results
Irradiation procedure

- irradiation tests performed three weeks ago at the Padova INFN X-rays facility

- prototypes irradiated up to 230 Mrad Total Ionizing Dose (TID)

- irradiation at room temperature

- electronics always biased at nominal operating conditions

- continuous monitoring of chip configuration and operations, charge scans performed at different TID steps (0.2 / 0.4 / 0.6 / 0.8 / 67 and 230 Mrad)
- **chip fully-functional** after 230 Mrad, digital readout and configuration OK
- **3 μs calibration cycles** required for efficient autozeroing after 230 Mrad, still compliant with online LHC machine operations
- **threshold linearity** verified, **no significant threshold variations** observed after irradiation
Noise after irradiation

- ENC constant behavior still present after 230 Mrad TID
- no significant degradation of low-noise performance observed
Conclusions

- **CHIPIX65 demonstrator** submitted in July 2016 using 65 nm CMOS, chips received back from the foundry at the end of September
  - 64 × 64 pixel matrix, 50 µm × 50 µm pixel size

- **full-system integration** with digital-on-top design methodology
  - silicon proven **IP-blocks** developed by INFN for RD53, now used also for RD53A prototype
  - two different **analog front-end designs** working in parallel
  - novel **region-based digital architecture** for latency buffering and trigger matching

- **highly encouraging results** from preliminary tests
  - both synchronous and asynchronous front-end designs, all IP blocks and digital parts are **fully working**, good agreement with CAD simulations
  - low-noise performance (ENC ≈ 90 e− RMS) achieved for both designs despite digital activity
  - **fully-working chip also after 230 Mrad TID** with negligible degradation of analog key parameters

- **next steps**
  - **cold** irradiation tests at the CERN PH-ESE X-rays facility up to 500 Mrad/1 Grad TID
  - completion of DAQ software with some extensions
  - **bump-bonding** with 3D sensors (FBK) and planar sensors (Hamamatsu)
  - final integration of selected CHIPIX65 components into **RD53A prototype** (FE designs, bias network, pixel digital architecture)
Thank you
for your attention

N. Demaria et al., *CHIPIX65: Developments on a new generation pixel readout ASIC in CMOS 65 nm for HEP experiments*. Proceeding of the 2015 IEEE International Workshop on Advances in Sensors and Interfaces (IWASI)


L. Pacher et al., *A Low-Power Low-Noise Synchronous Pixel Front-End Chain in 65 nm CMOS Technology with Local Fast ToT Encoding and Autozeroing for Extreme Rate and Radiation at HL-LHC*. Proceeding of the 2015 IEEE Nuclear Science Symposium and Medical Imaging Conference (IEEE NSS/MIC)


L. Ratti et al., *An asynchronous front-end channel for pixel detectors at the HL-LHC experiment upgrades*. Proceeding of the 2015 IEEE Nuclear Science Symposium and Medical Imaging Conference (IEEE NSS/MIC)


E. Monteil et al., *A synchronous analog very front-end in 65 nm CMOS with local fast ToT encoding for pixel detectors at HL-LHC*. Proceeding of the 2016 Topical Workshop on Electronics for Particle Physics (TWEPP). Submitted to Journal of Instrumentation (JINST)


Backup slides
Autozeroed synchronous discriminator

- Track-and-latch voltage comparator
  - low-gain high-bandwidth differential amplifier, 1 µA bias current
  - class B CMOS latch with reduced kick-back noise
- Front-end analogue signal sampled at nominal 40 MHz clock frequency
  - in-time response below 25 ns always guaranteed for time-stamp assignment
  - no time-walk issues, leading-edge of the hit pulse always synchronized with BX
- Offset compensation performed through Output Offset Storage (OOS)
  - pixel-to-pixel threshold variations minimized without the need of a local DAC
  - SEU-tolerant registers no more required, increased available area for digital part
Latch control logic for fast ToT counting

- **Latch** can be turned into a local oscillator using asynchronous logic as performed in modern high-speed SAR-ADCs.
- High-frequency self-generated clock signals available for fast ToT counting up to GHz in 65 nm CMOS technology.
- Voltage-controlled delay line used to tune the latch oscillation frequency in the 100-900 MHz range.
- Up to 8-bit ToT digitizations achievable in less than 400 ns if requested.
autozeroing scheme suitable to fit **LHC machine online operations**

- \( f_{RF} = 40 \text{ MHz} \), \( \lambda_{RF} = 0.75 \text{ m or } 2.5 \text{ ns} \)
- bunches spaced by 25 ns or 10 buckets, 72 bunches = 1 batch
- injection of 2, 3, or 4 batches
- a 119-bunches long **bunch abort gap** is available every \( \approx 3 \mu s \)
- main **beam abort gap** every 90 \( \mu s \)
- perform autozeroing during available discontinuities within the bunch-train pattern
Synchronous FE operations

10 ke input charge and 1 ke threshold
20 nA feedback current

same front-end configuration with latch turned into a local oscillator
≈ 100 MHz self generated clock
latch dynamic offset **underestimated** in the first submitted design

**significant improvement** of autozeroing performance in the **second version** with a **residual offset** of \( \approx 70 \text{ e}^- \) RMS

offset **efficiently compensated** up to \( \approx 100 \mu\text{s} \) before irradiation
Mini@sic post-irradiation results

- **Average values** tracked as a function of TID
- **Pulse amplitude** shows small variations with radiation
- **Peaking time** increases for TID $> 100$ Mrad
- **Recovery effects** observed after 3-days annealing at room temperature
- **noise slope** increases after irradiation
- ENC linearity with input capacitance still present after 600 Mrad TID
- **latch oscillation frequency** decreases with radiation, partial recovery after 3-days annealing at room temperature