INFN
Istituto Nazionale
di Fisica Nucleare

3D sensors measurements with FEi4 read-out chips

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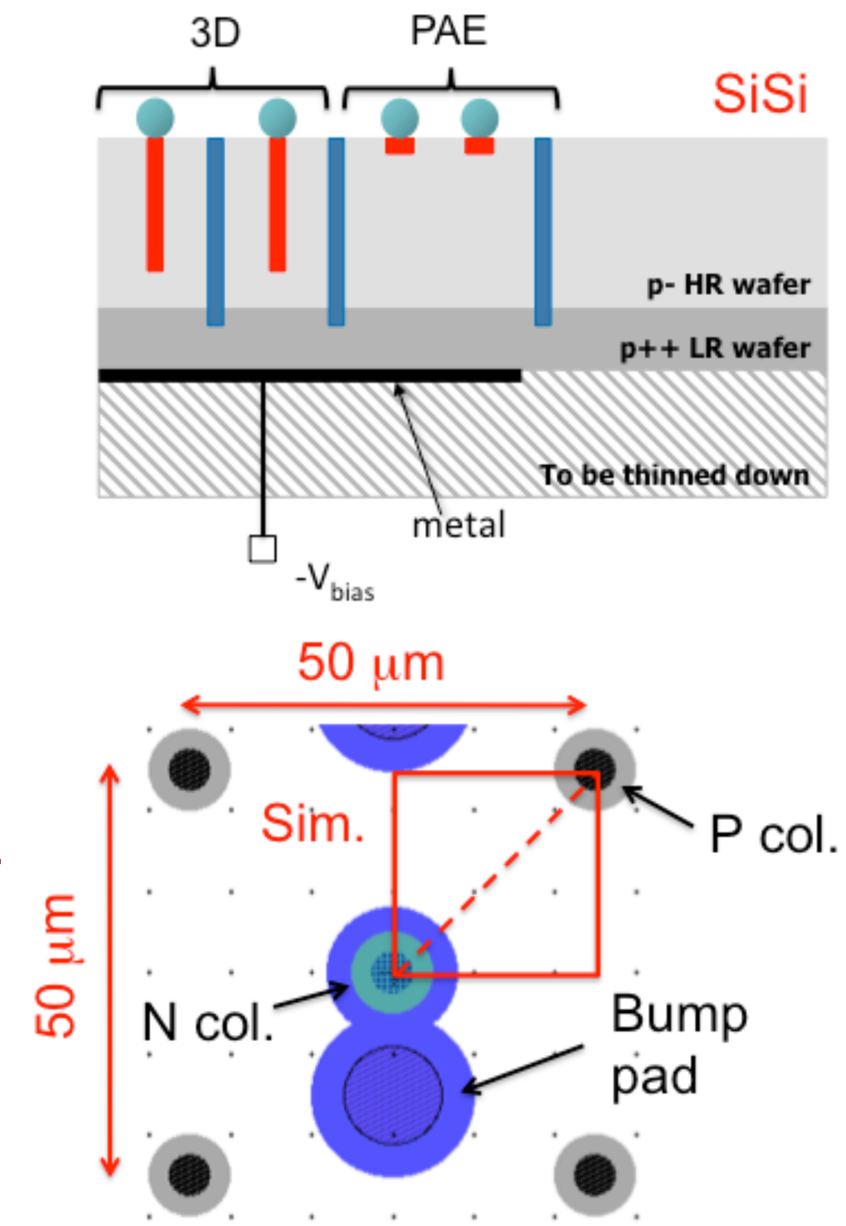
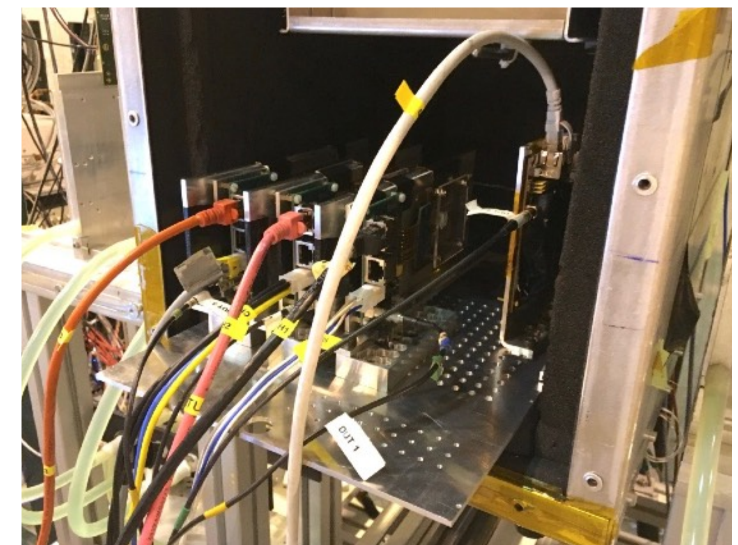
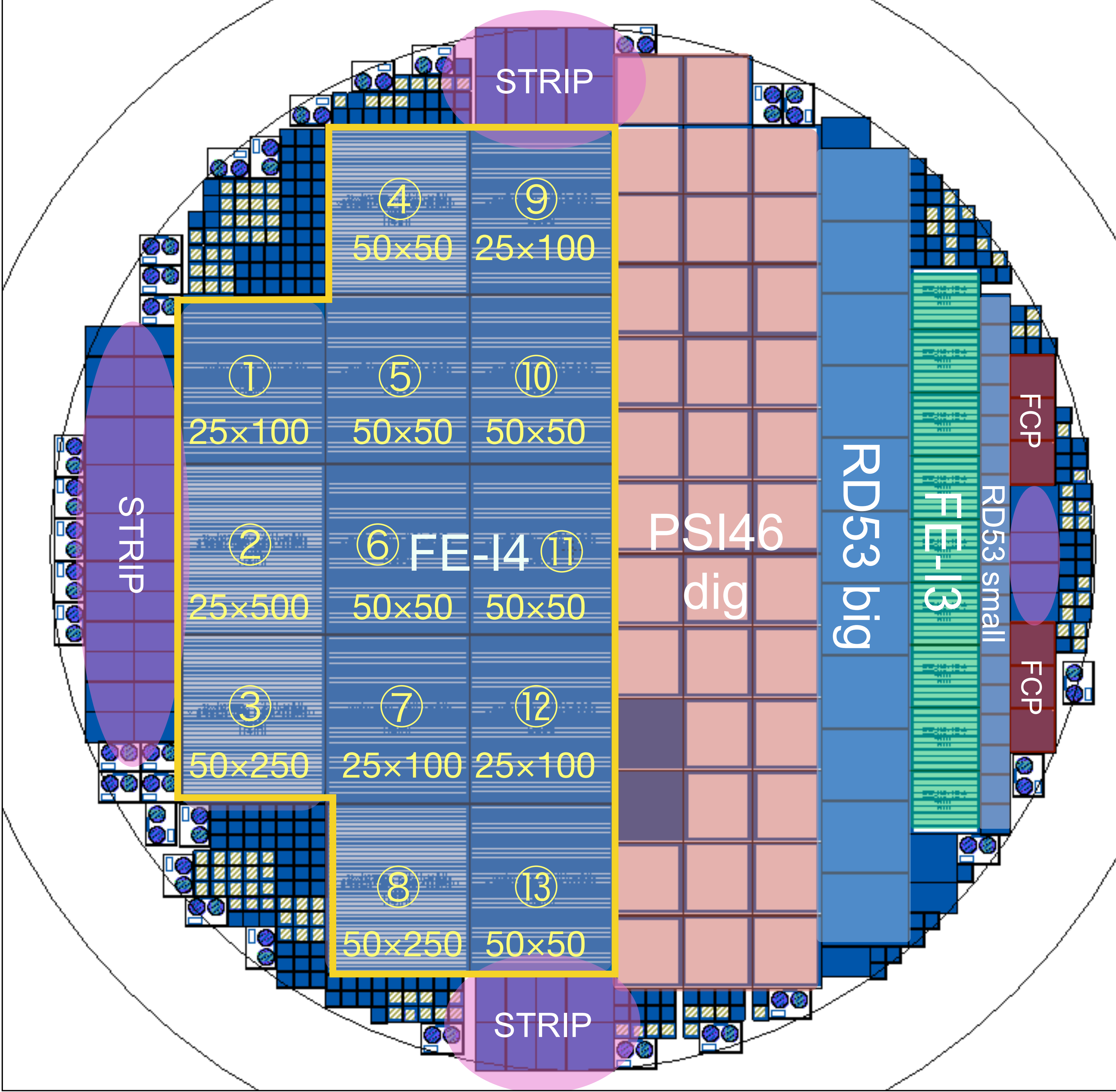
Talk Outline

- New thin 3D pixel sensors on 6” p-type wafers at FBK.
  - Work carried out within INFN RD_FASE2 and AIDA2020 projects.
  - Targetted irradiation of **$\Phi = 2\mathrm{x}10^{16}\ n_{eq}/cm^2$** (regarding **innermost pixel layers in HL-LHC**).
  - Layout compatible with **FEI4** (for testing) and **RD53** chips.
  - Similar design layout to CNM 3D sensor prototypes (David’s talk).
- A first batch (9 wafers) produced in 2016.
  - Active thickness (**130 μm or 100 μm**) / Presence of poly-caps / ..
- FEI4-compatible sensors of a 130μm-thick wafer bump-bonded at **Leonardo** (previously known as **Selex**).
  - Multiple pixel layouts. including: { **250x50** μm^2 (2E), **50x50** μm^2 (1E), **100x25** μm^2 (1E) } (but not only).
- Tests and Results
  - Basic characterisation at the Genova lab.
  - The first test beam of **non-irradiated** 3 modules in CERN SPS H6A.





The wafer layout



- FE-I4
  - 50x250 (2E) — std.
  - 50x50(1E)
  - 25x100(1E and 2E)
  - 25x500 (1E)

13 sensors in total

- FE-I3
  - 50x50 (1E)
  - 25x100 (1E and 2E)
- PSI46dig
  - 100x150 (2E and 3E) — std.
  - 50x50 (1Eand2E)
  - 50x100, 100x100 (2E and 4E)
  - 50x100, 100x150 (2E and 6E)
  - 25x100(1E and 2E)
- FCP
  - 30x100 (1E)
- RD53
  - 50x50(1E)
  - 25x100 (1E)
  - 25x100 (2E)
- Other test structures

W76 - 130 µm thickness, w/ poly-Cap - Sensor Breakdown

3DSS_15 - W76

FEI4_grid included_total current

I [nA]

1E+08
1E+07
1E+06
1E+05
1E+04
1E+03
1E+02
1E+01
1E+00
1E-01

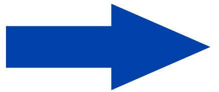
0 10 20 30 40 50 60 70 80

V_rev [V]

F4_25x100_1E-gr_1
F4_25x500_2
F4_50x250_3
F4_50x50_450L_4
F4_50x50_gr_5
F4_50x50_gr_6
F4_25x100_1E-gr_7
F4_50x250_gr_8
F4_50x50_gr_10

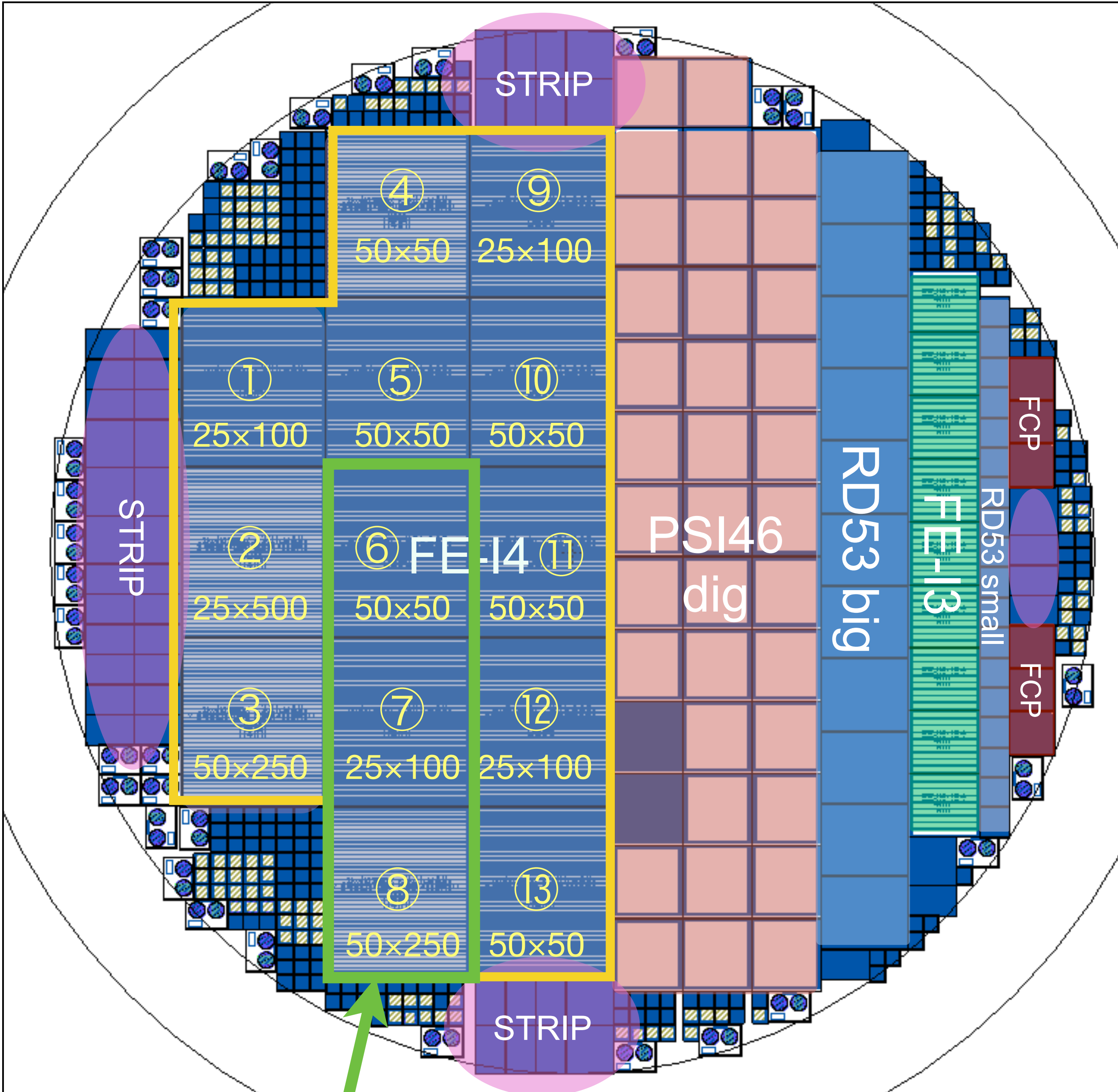
9 sensors in total

* 9,11,12,13: rejected for either early breakdown or too-large I_{leak}



Deposition, cutting and assembly of W76 were done at Leonardo.
9 FE-I4 sensors of W76 were delivered in late July. W78 is ongoing.

Samples for the Test Beam

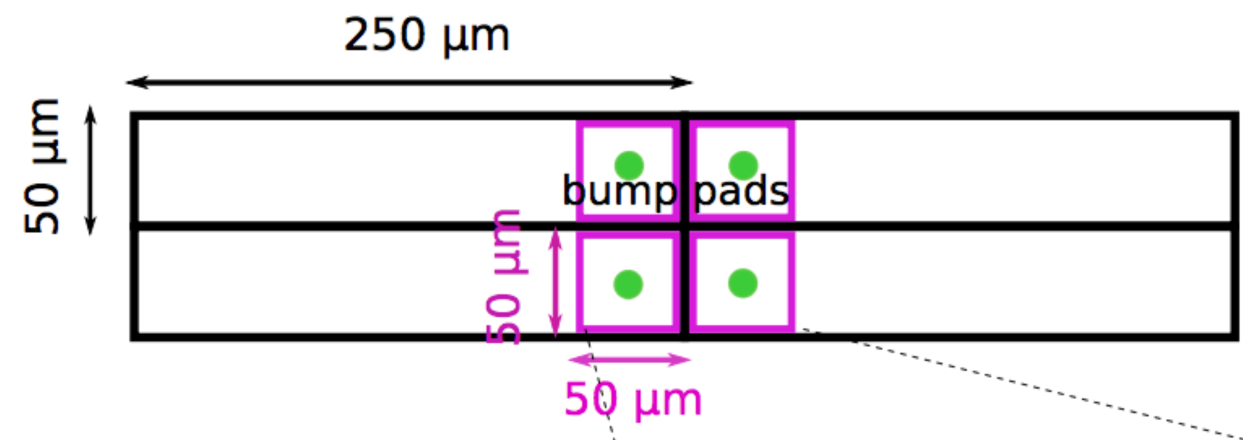


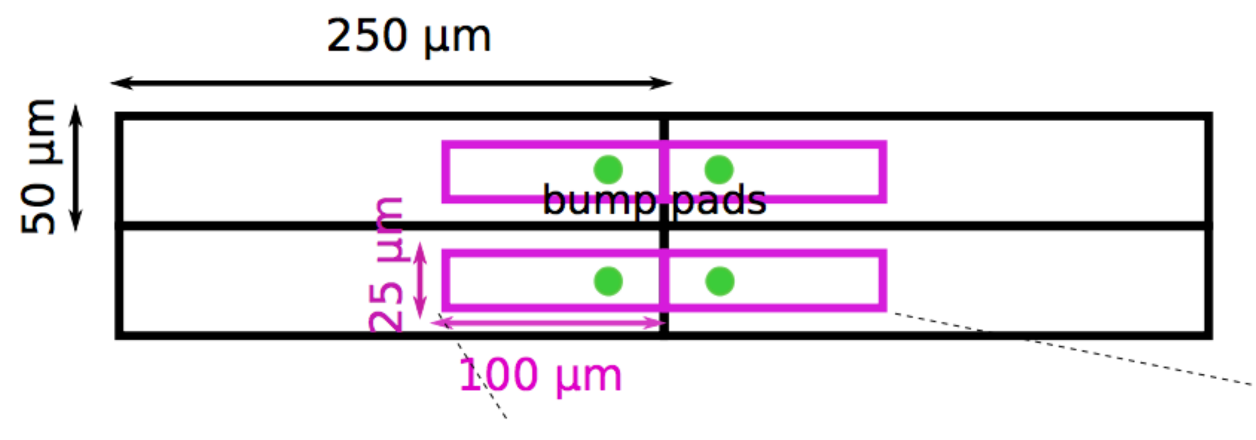
ID	Size	Sensor V_{bd} [V] after assembly	Basic electric qualification
①	25x100	24	N/A
②	25x500	15	N/A
③	50x250	25	N/A
④	50x50	15	GOOD
⑤	50x50	2	Too-low V_{bd}
⑥	50x50	12	GOOD
⑦	25x100	>80	GOOD
⑧	50x250	12	GOOD
⑩	50x50	>80	regulator broken

- This test beam: used 3 sensors
- 50×50(1E), 25×100(1E), 50×250(2E)
- Bump-bonded by Selex
- Non-irradiated

Larger current on some samples observed after assembly wrt. wafer measurement, to be investigated.

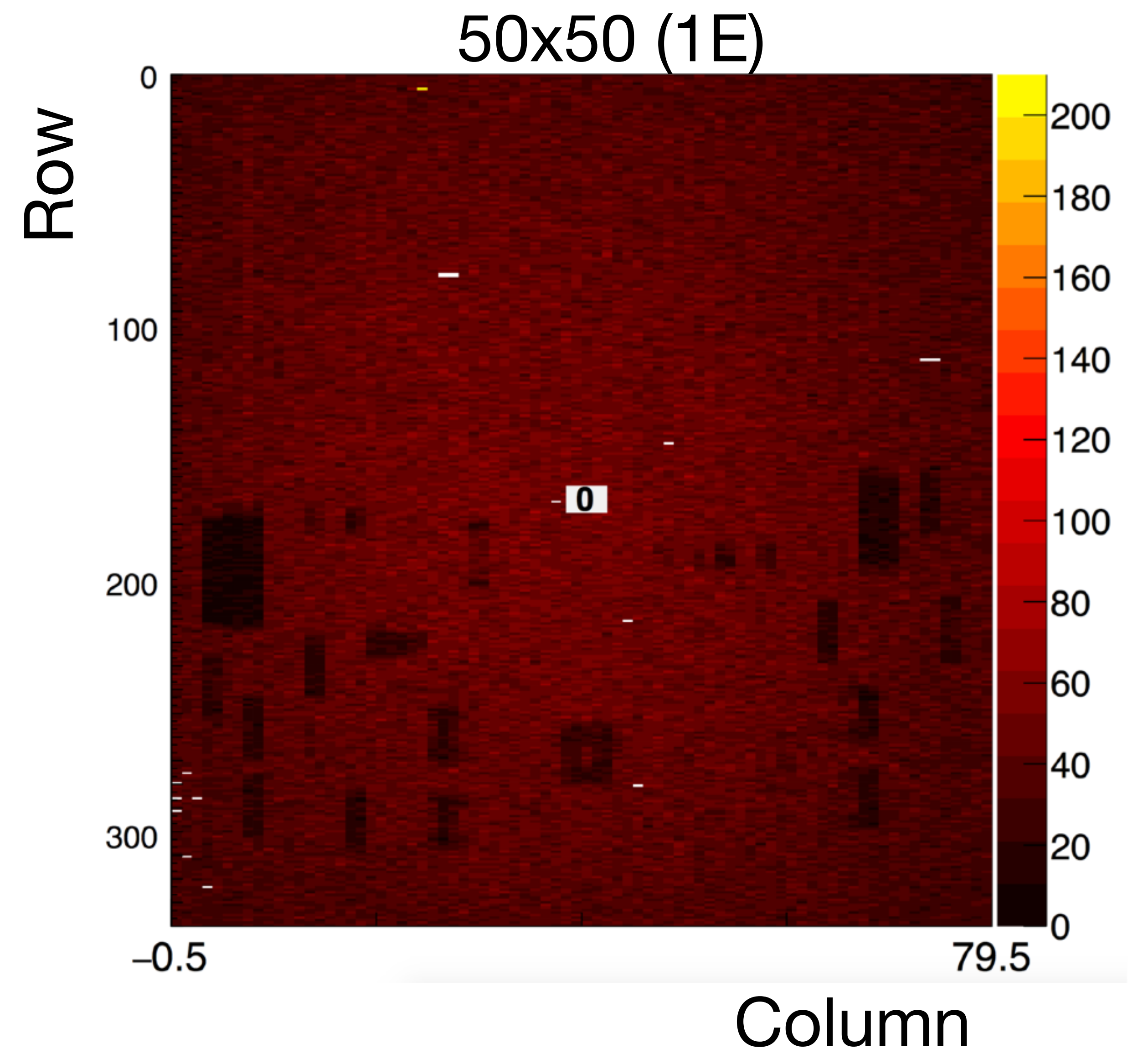
Bump Bonding to FE-I4: Source Scan

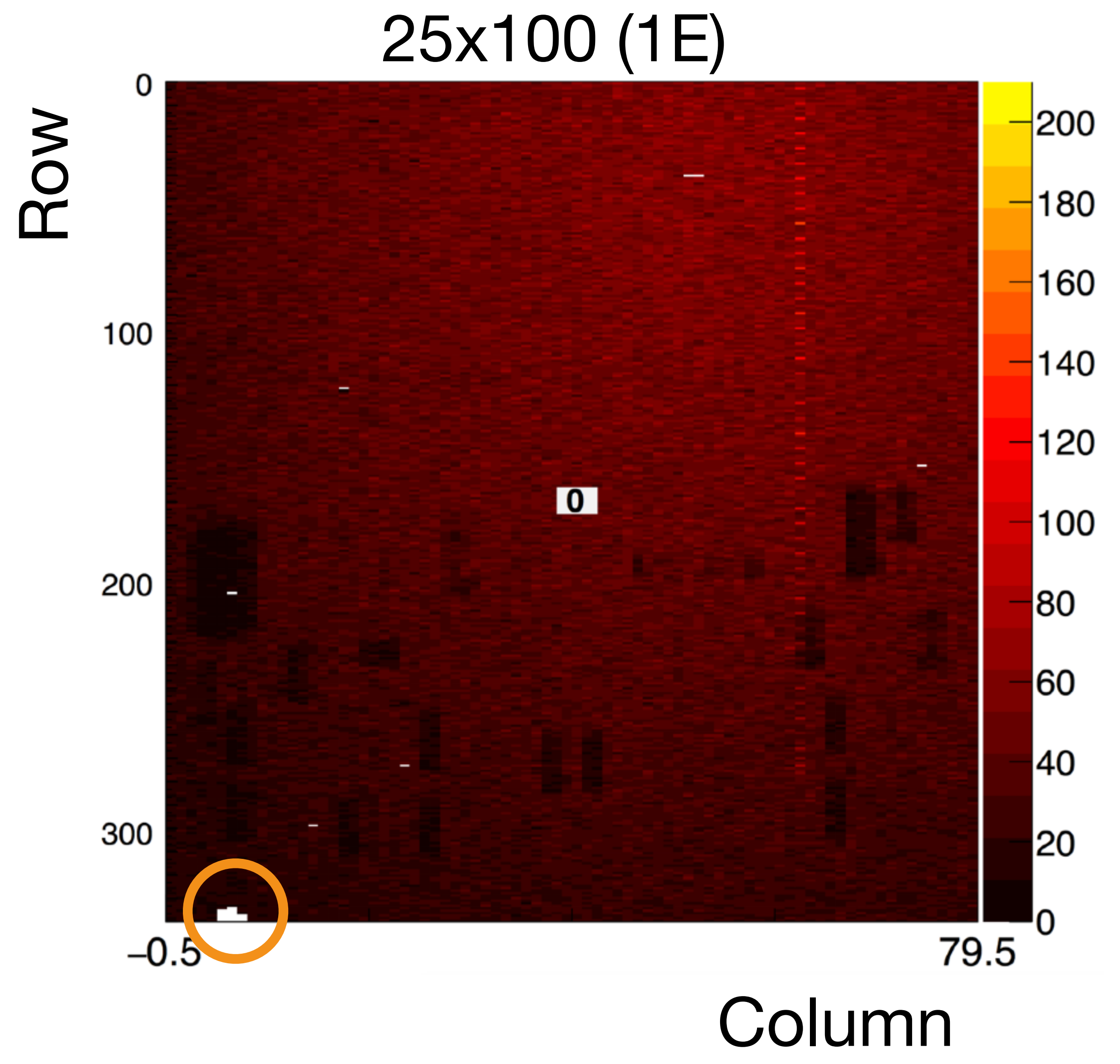




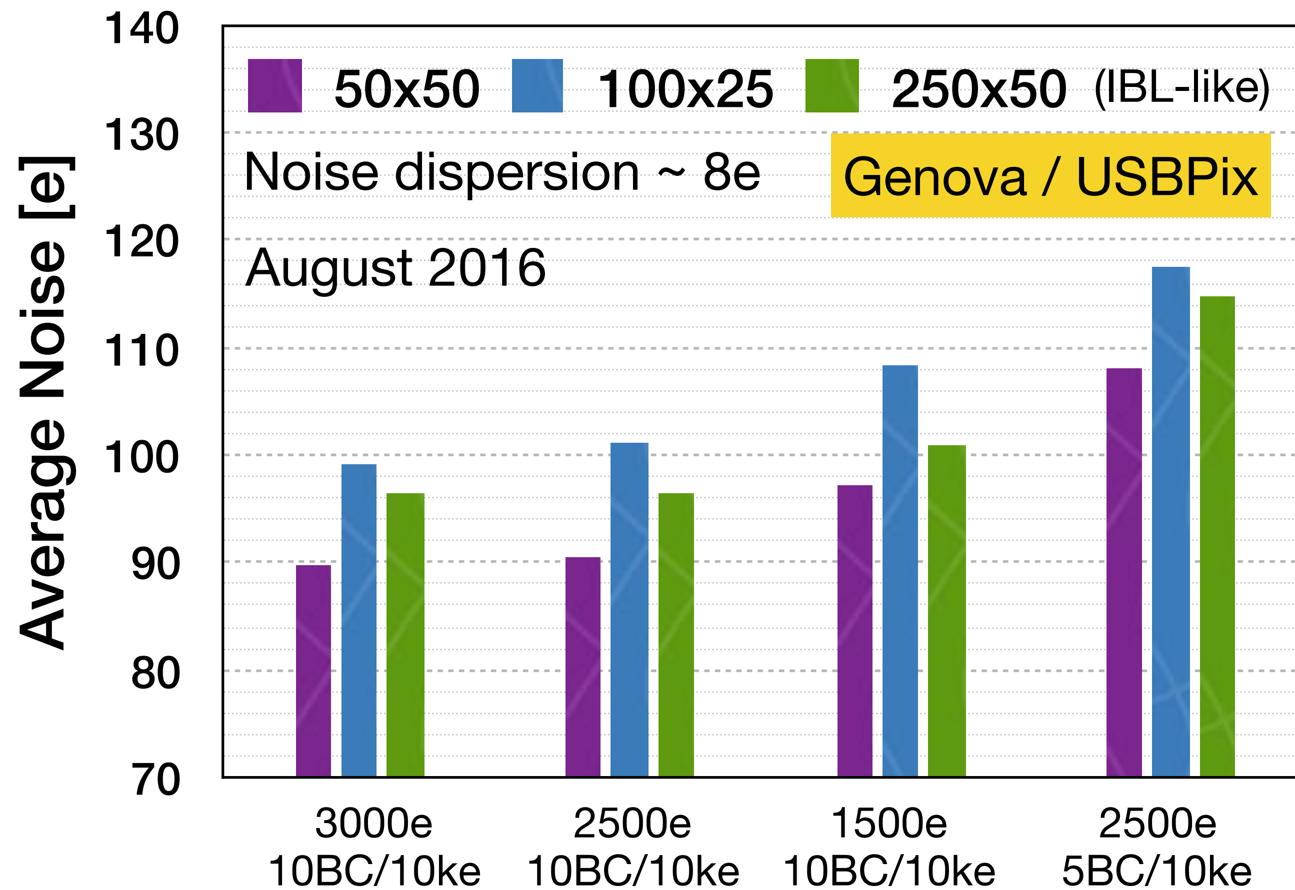
Note, only 20% of the pixels are read out w/ FE-I4.

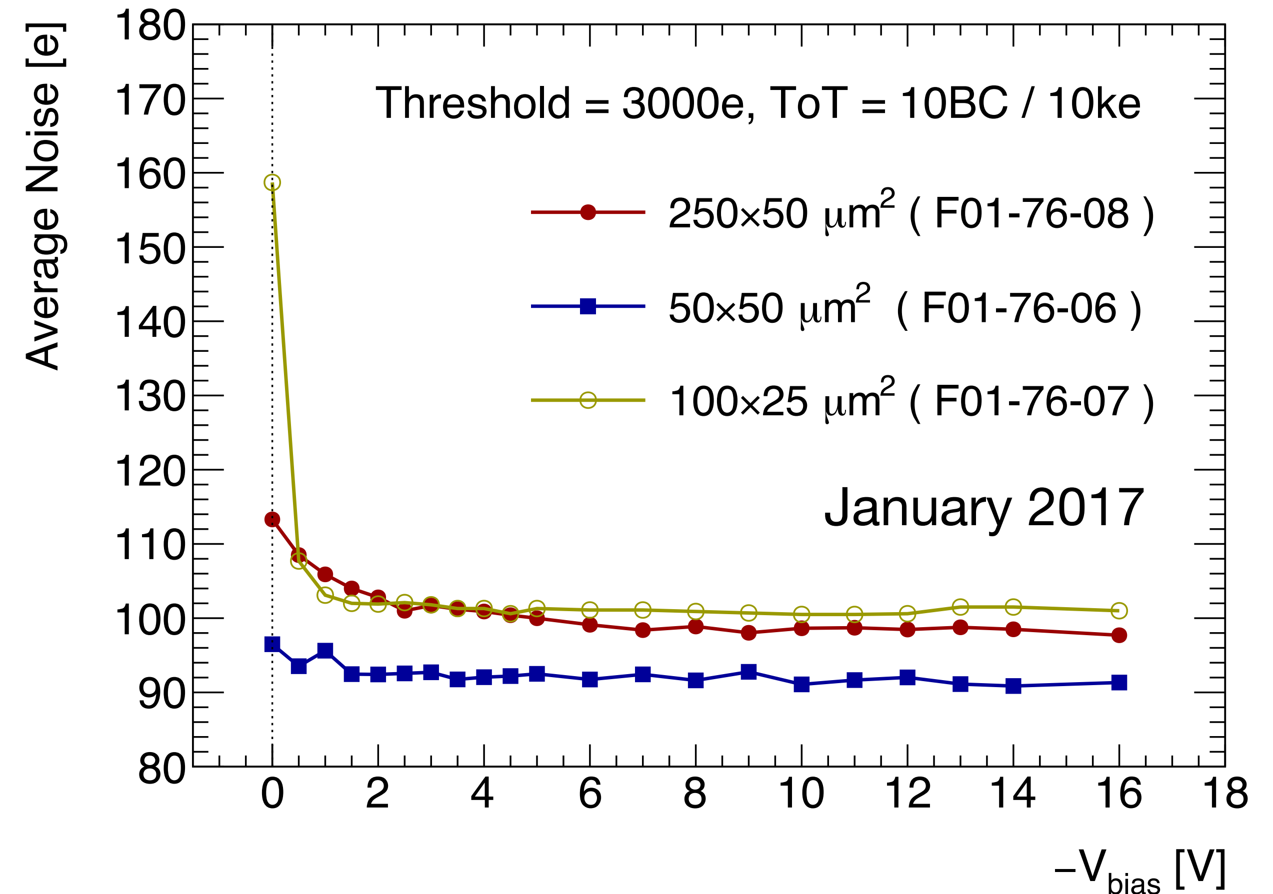
^{241}Am Source Scan@Genova





Noise measurements





- Threshold scan with HV-on.
- Tuning was successful for the 3 modules in the all tuning targets.
- Wrt. 50x250 μm², 50x50μm² gives slightly less noises
  while 25x100μm² slightly more (consistent with each capacitance).

Test Beam Setup - (CERN SPS H6A, Aconite)

Telescope Planes (Front)

Module 3 (50X250)

Module 2 (25X100)

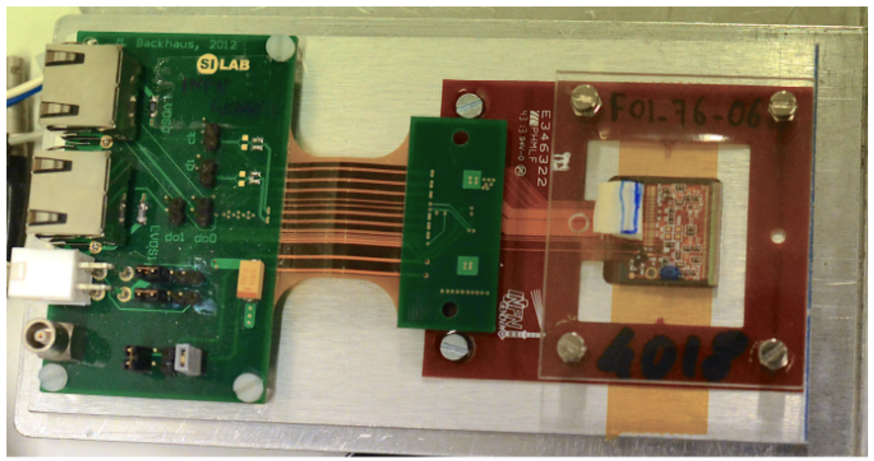
Module 1 (50X50)

Telescope Planes (Back)

Column

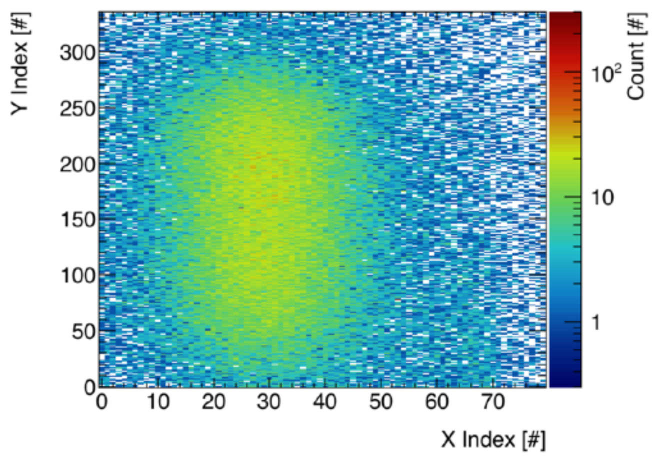
Row

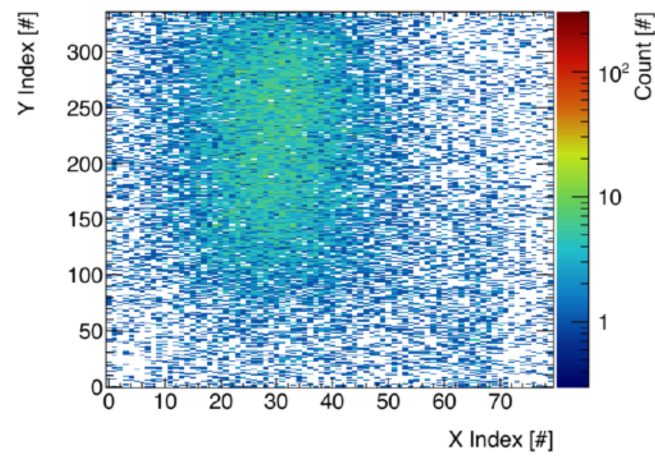
Ref. Module (single planar)

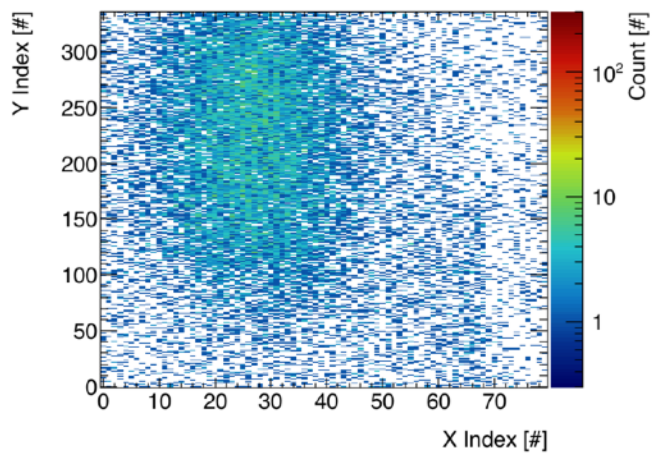


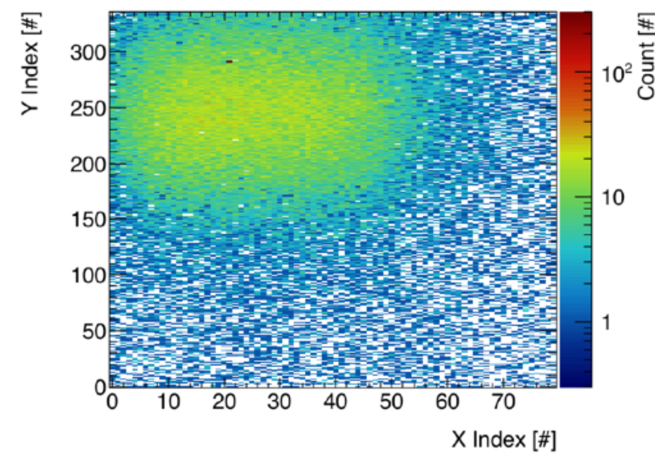
- SPS H6A beam line, Aconite telescope.
- CIS4-W8-4 (single planar) as the reference.
- A tricky mechanical configuration due to the sub-optimal shape of the readout boards - needs improvements in the future.
- Tilt angle is not very accurately controlled (around 5° in row direction)
- Acquired dataset:
  - 2 cycles of HV scan at a fixed tuning (coarse/fine steps)
  - 1 set of tuning variation (threshold, ToT).

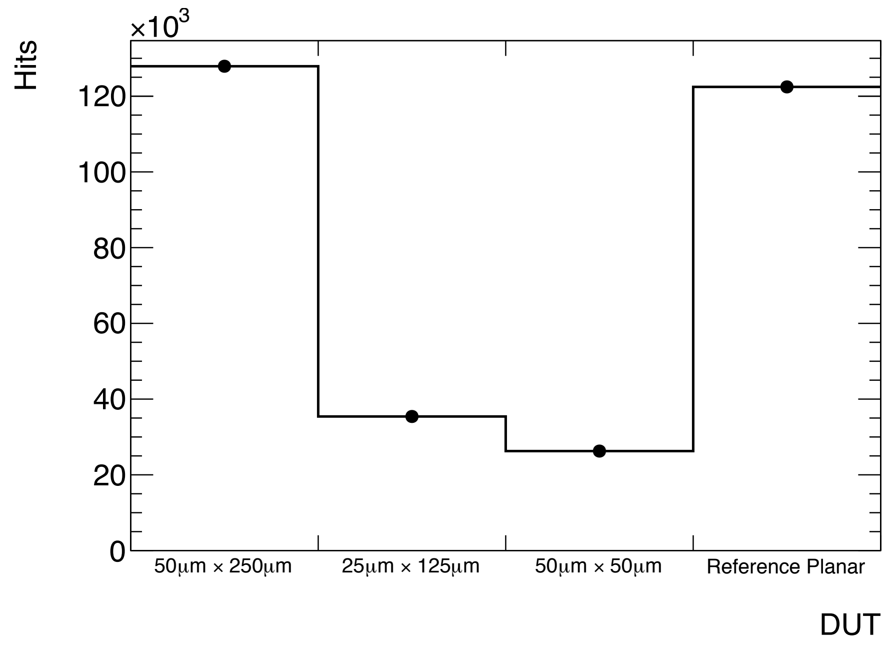
Short notes on data analysis

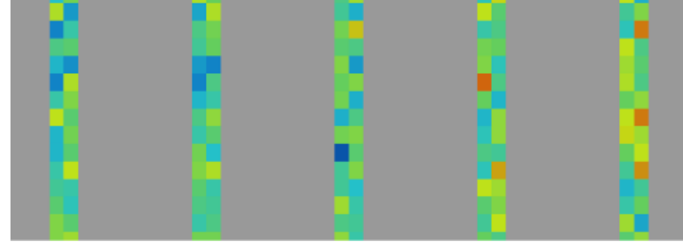


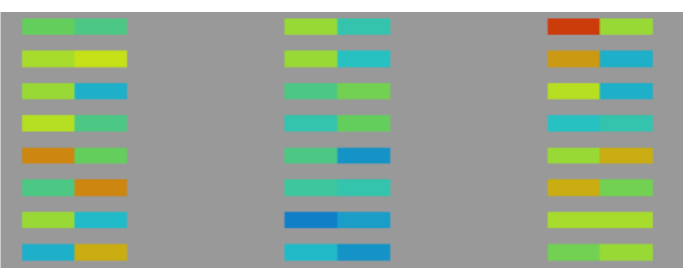


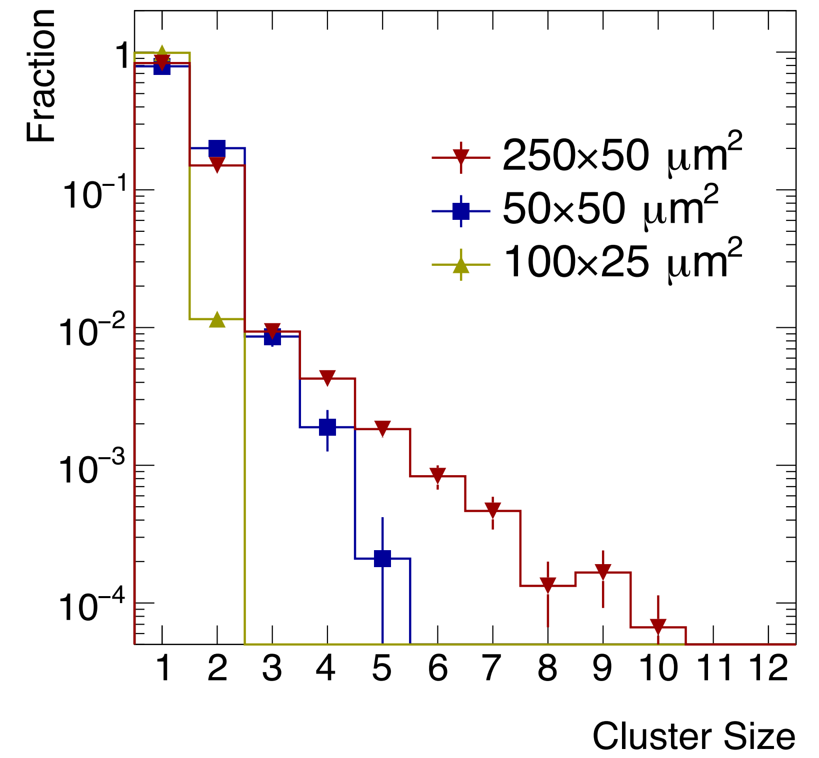






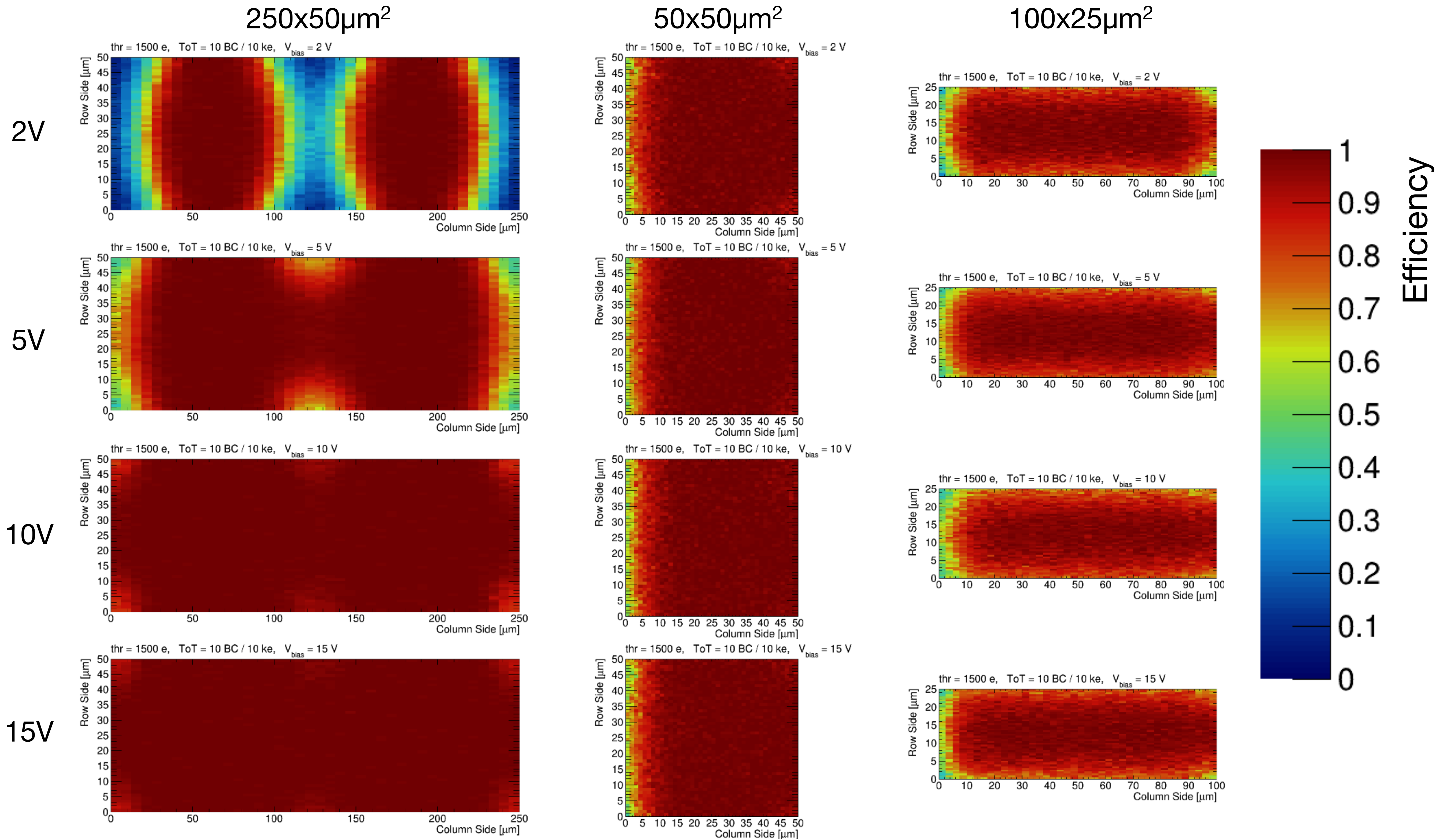






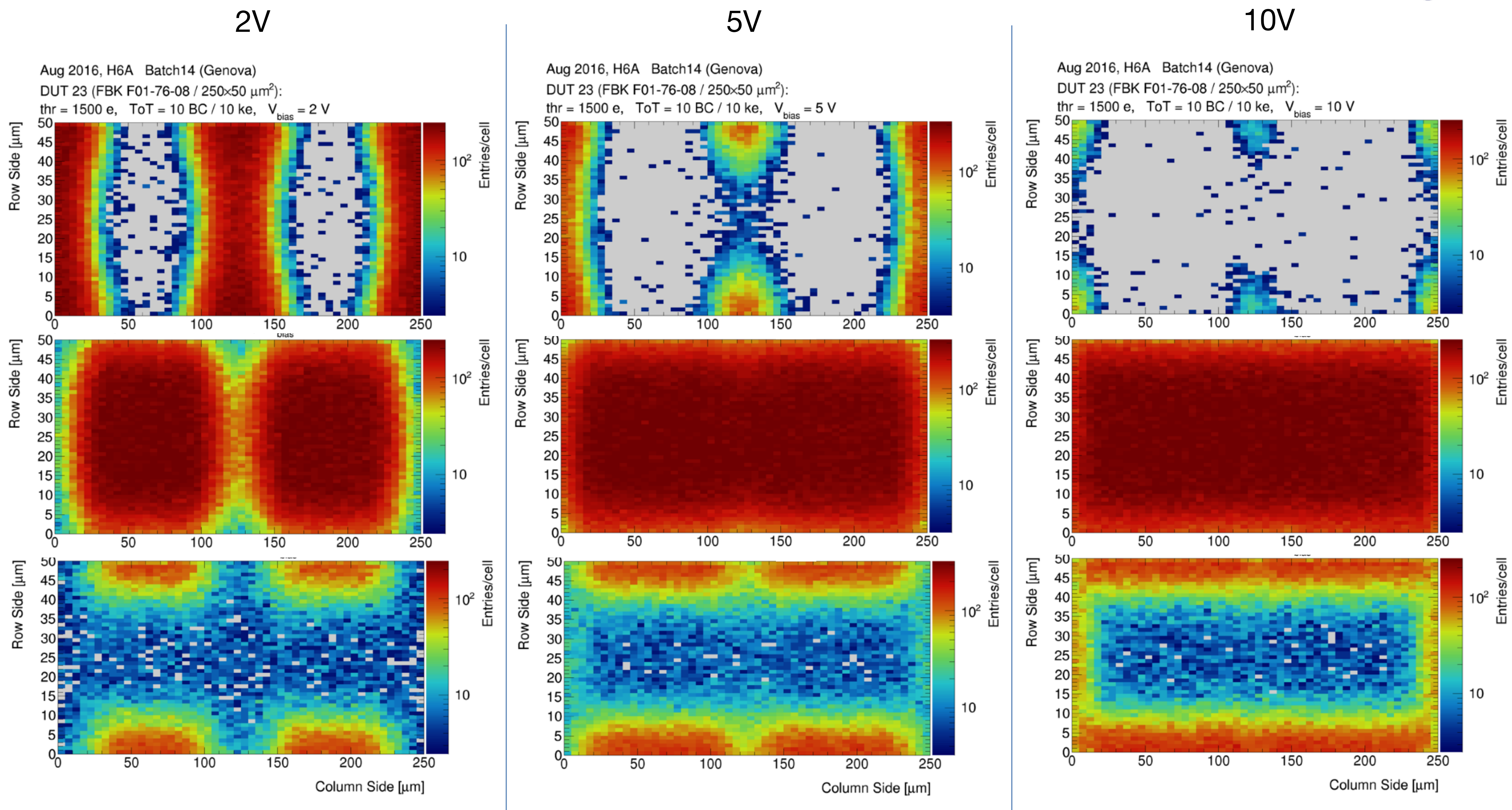
- Sparse readout for 50x50μm^2 and 100x25μm^2 sensors.
  → Customly implemented specialised geometry configurations.
- Acceptance of 50x50μm^2 and 100x25μm^2 is approximately 20%.
- Constraints on the cluster size:
  - 50x50 μm^2: maximum size of 2 in the column direction.
  - 100x25 μm^2: maximum size of 2 (1) in the column (row) direction.

HV Scan: Pixel-internal Efficiency (thr = 1500e, ToT = 10BC / 10ke)



- odd/even columns are folded by mirror flipping (same for the following slides).

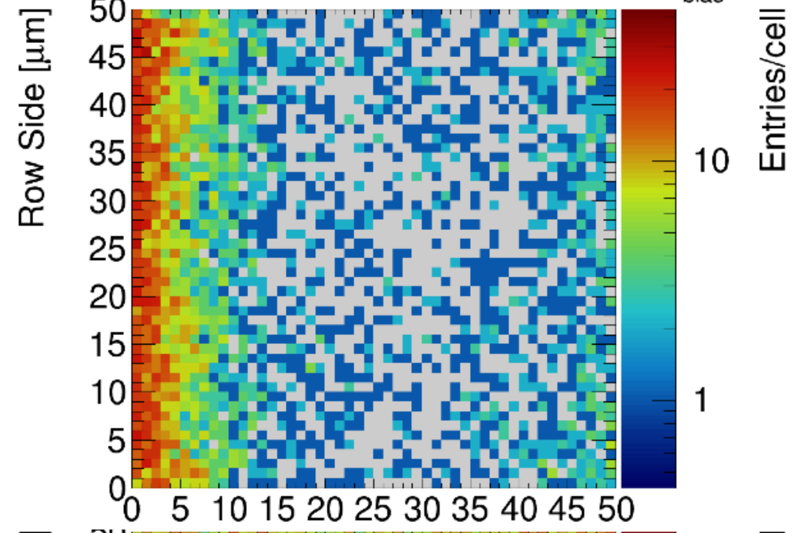
HV Scan: Cluster size vs. Position: 250x50μm^2 (thr = 1500e, ToT = 10BC / 10ke)



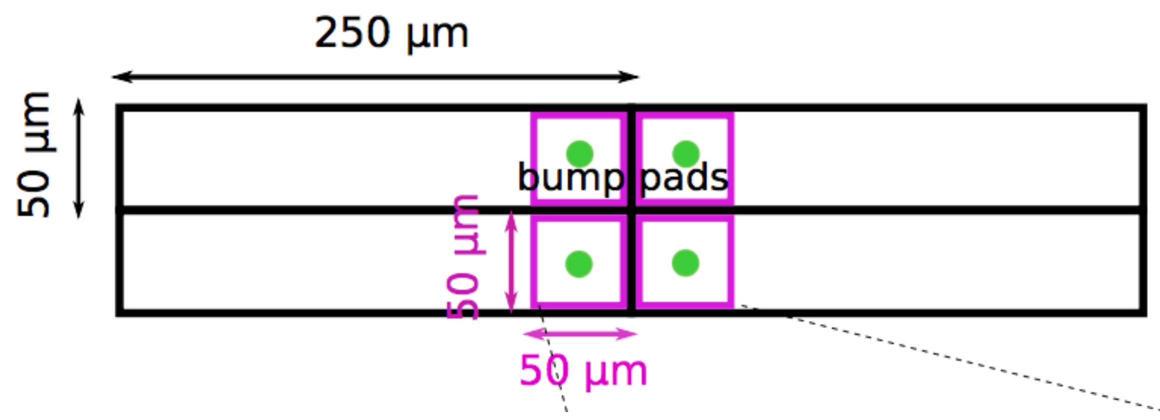
- { inefficient, size=1, size=2 } from top to bottom.
- Clear change of efficient region as a function of bias voltage.

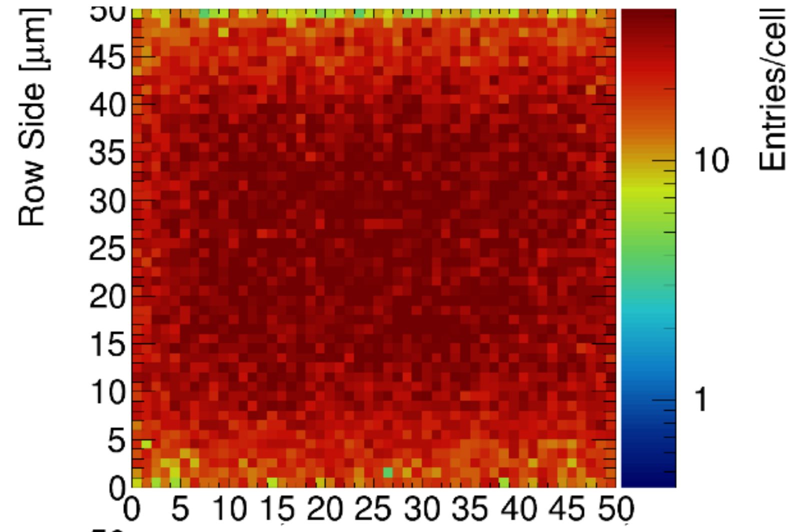
Pixel Hit Map vs. Cluster size — 50x50 (F01-76-06)

Aug 2016, H6A Batch14 (Genova)
DUT 21 (FBK F01-76-06 / 50×50 μm^2):
thr = 1500 e, ToT = 10 BC / 10 ke, V_{bias} = 10 V

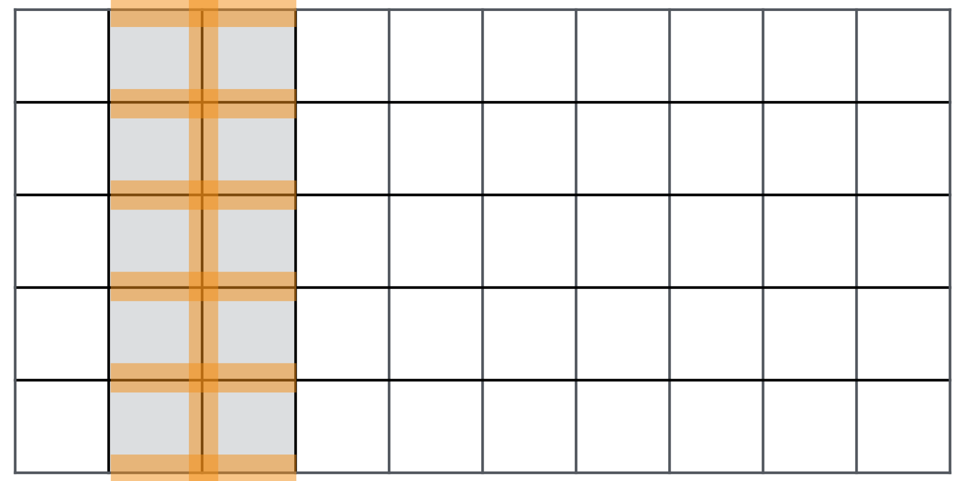


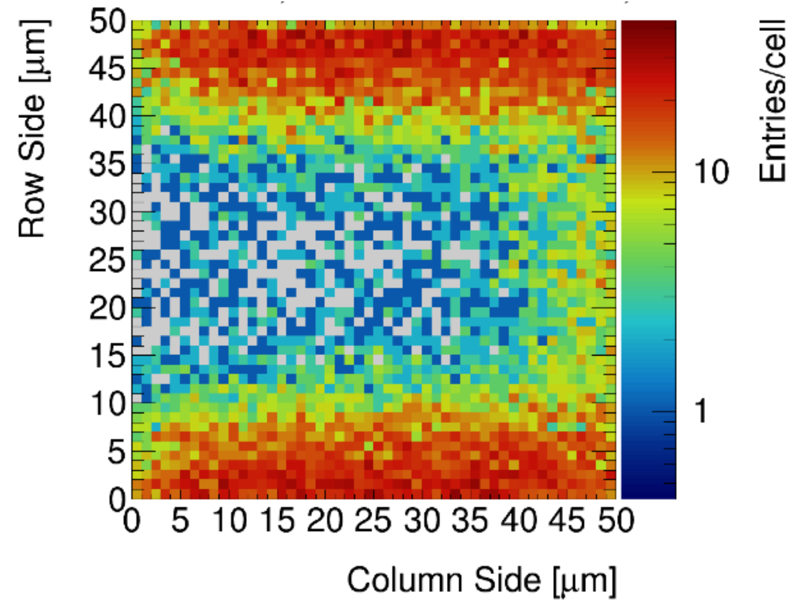
inefficient



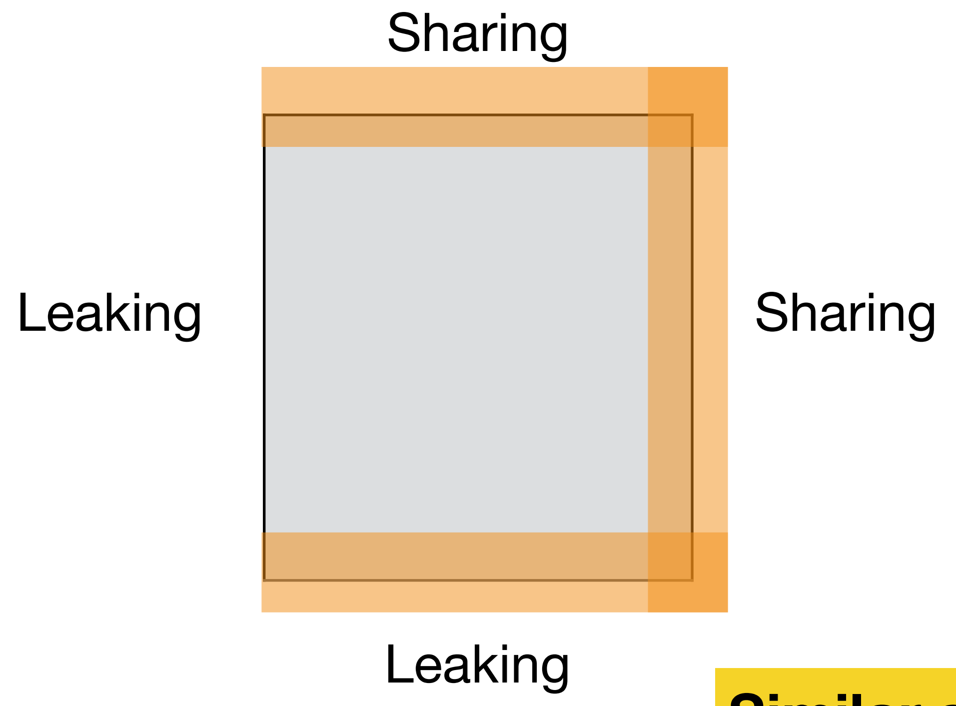


size=1





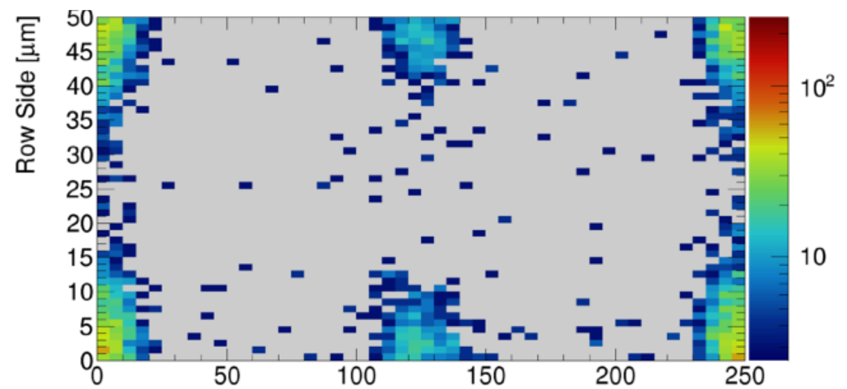
size=2

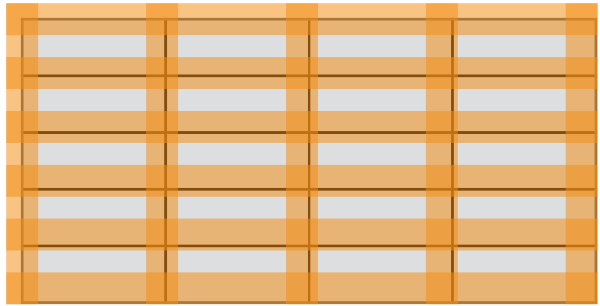


Similar story for 100x25

ROI mask definition for hit efficiency estimation (Tentative)

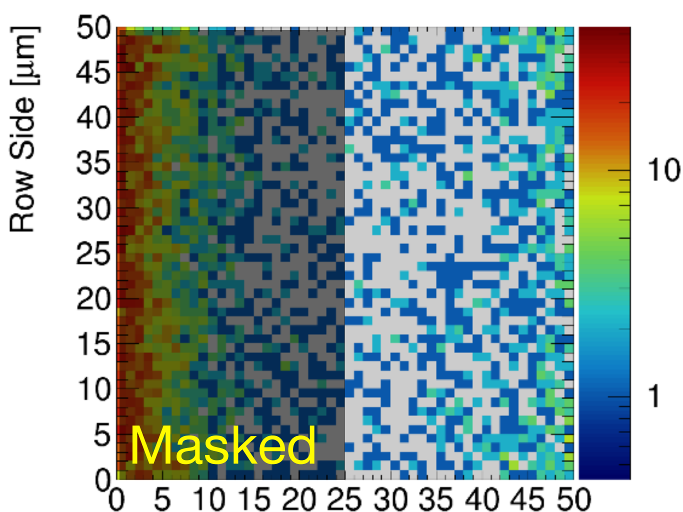
250x50

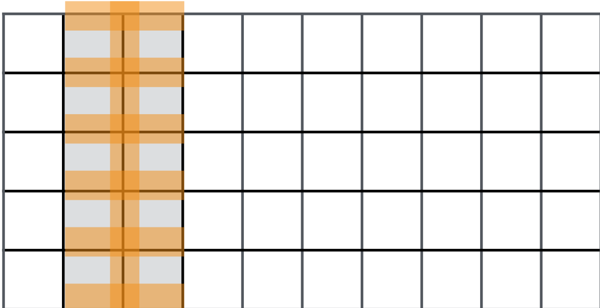


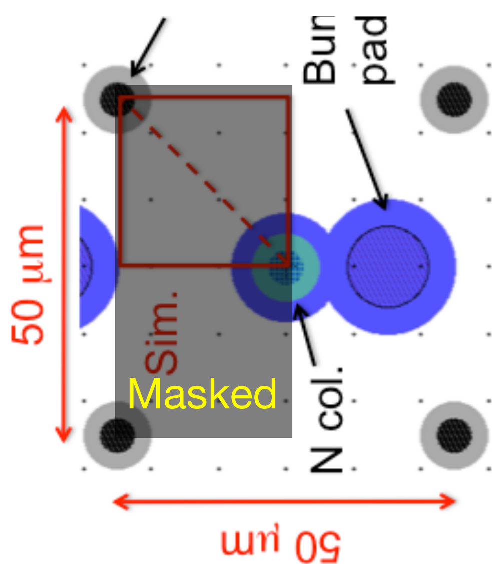


- **250x50: unbiased.**
- **50x50: hypothetically unbiased.**
- **100x25: *inevitably* biased!!**

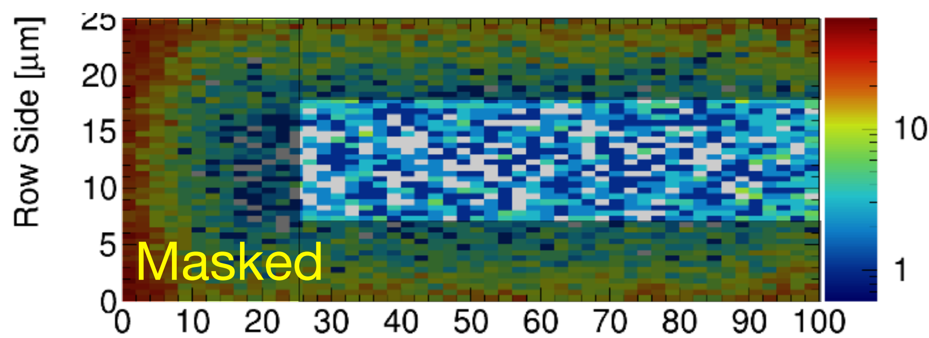
50x50

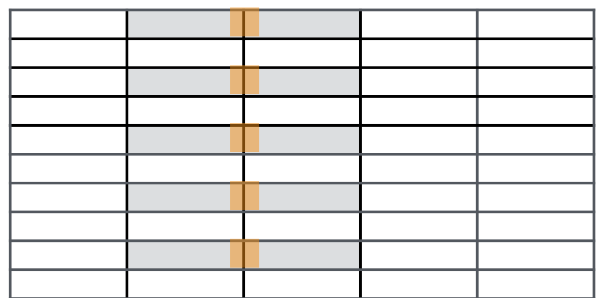


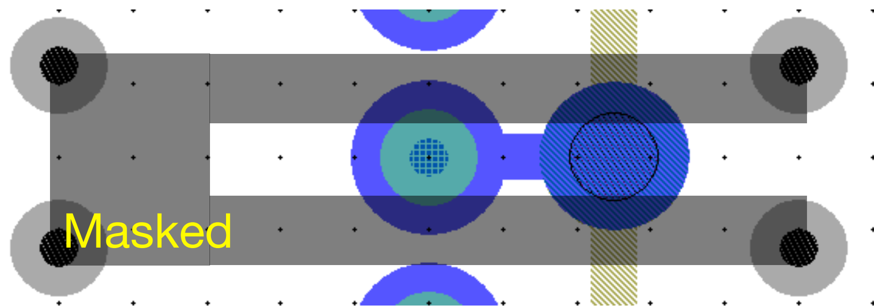




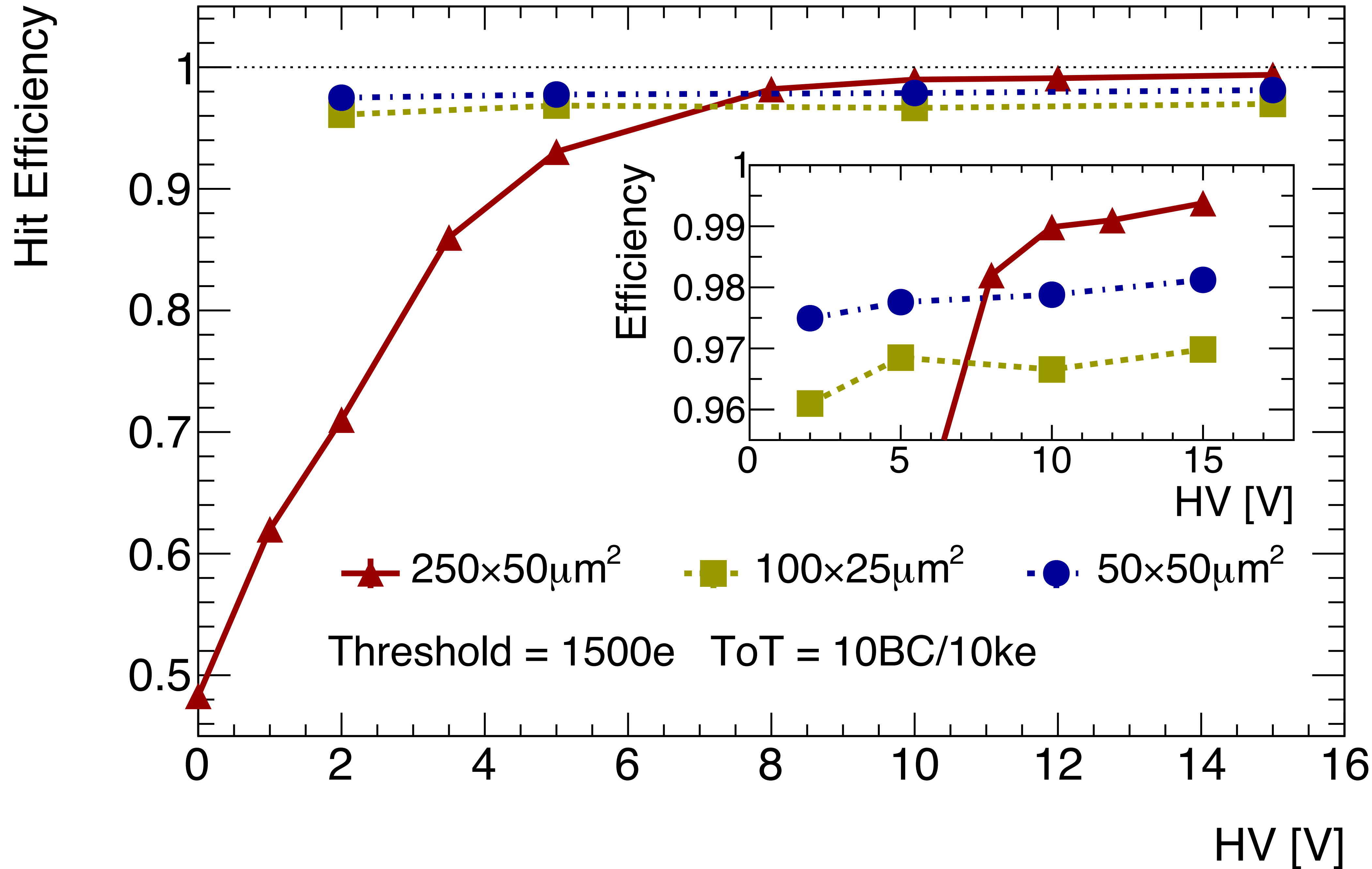
100x25





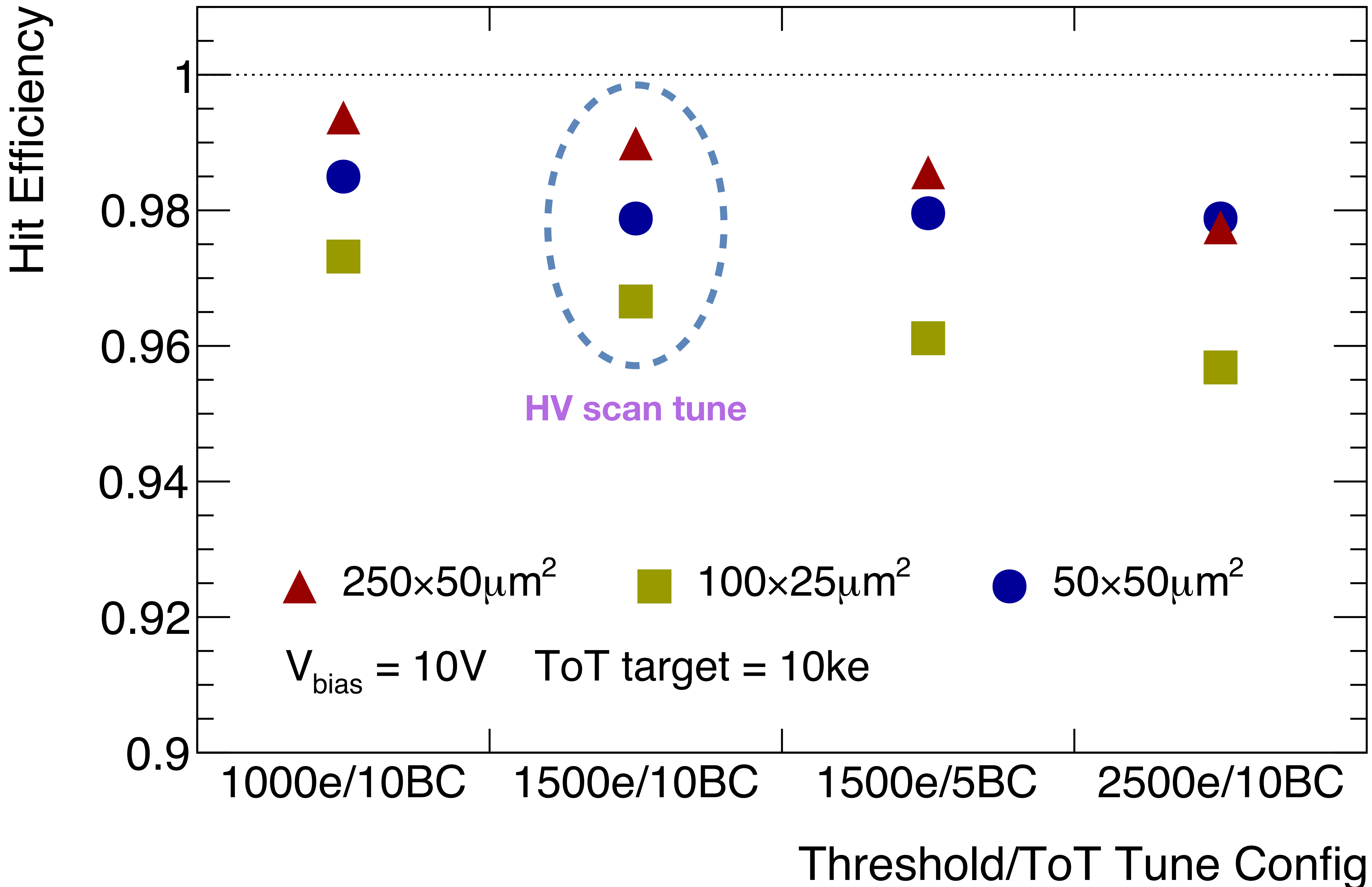


HV Scan: Hit efficiency (after masking)



- $250x50 \mu m^2$: Efficiency is >99% above ~10 V. Ramping up up to ~10 V.
- $50x50 \mu m^2$: Keeping almost flat ~98% efficiency in 2 < HV < 15 V. Slight increasing of ~1%.
- $100x25 \mu m^2$: shown just for reference. Qualitatively similar trend to $50x50 \mu m^2$.

Variation of hit efficiency by tuning (after masking)



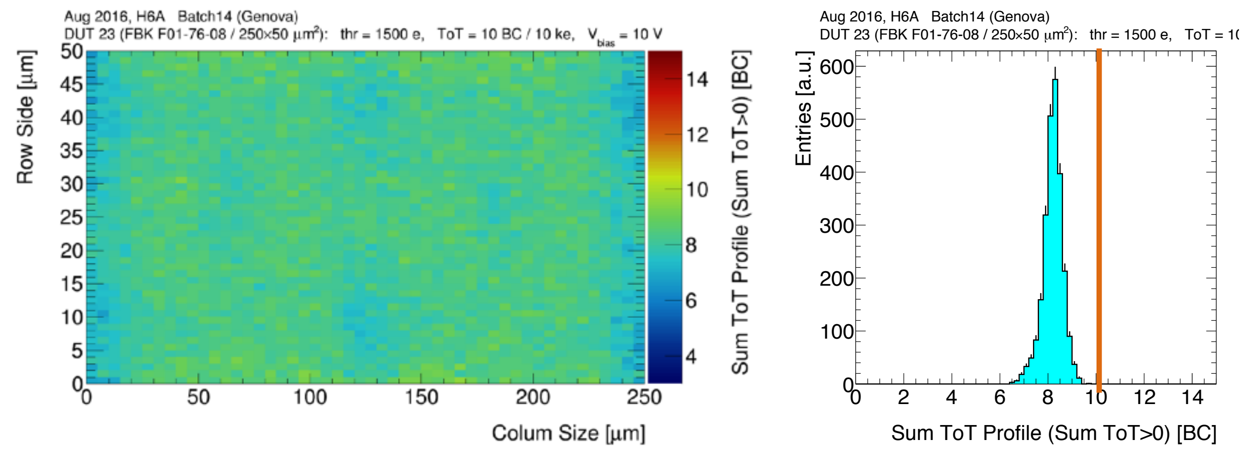
- A reasonable gradual change of efficiency by 1-2% is observed.
- 100x25μm^2: shown just for reference.

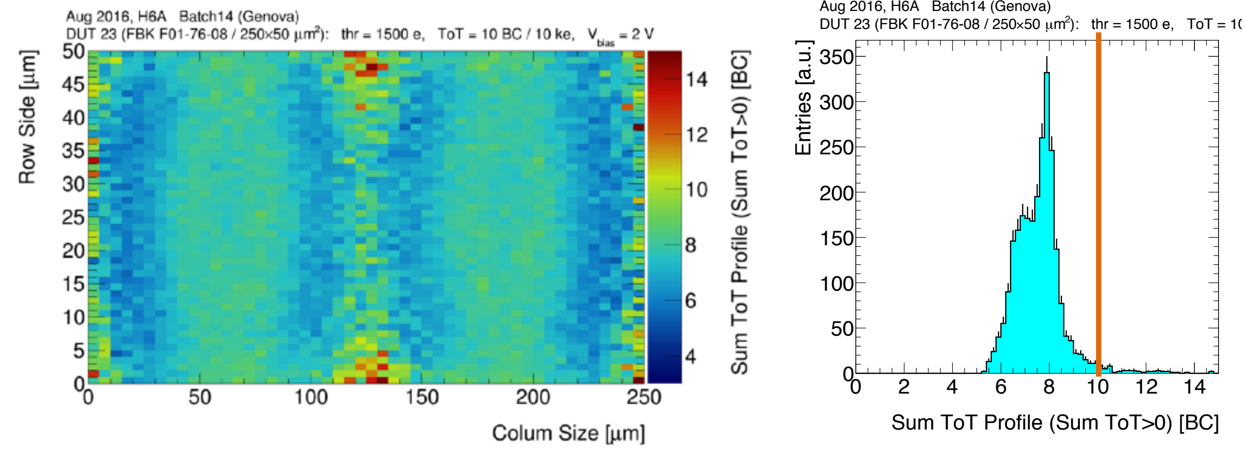
Charge Collection: Cluster Sum ToT Map Profile

10V

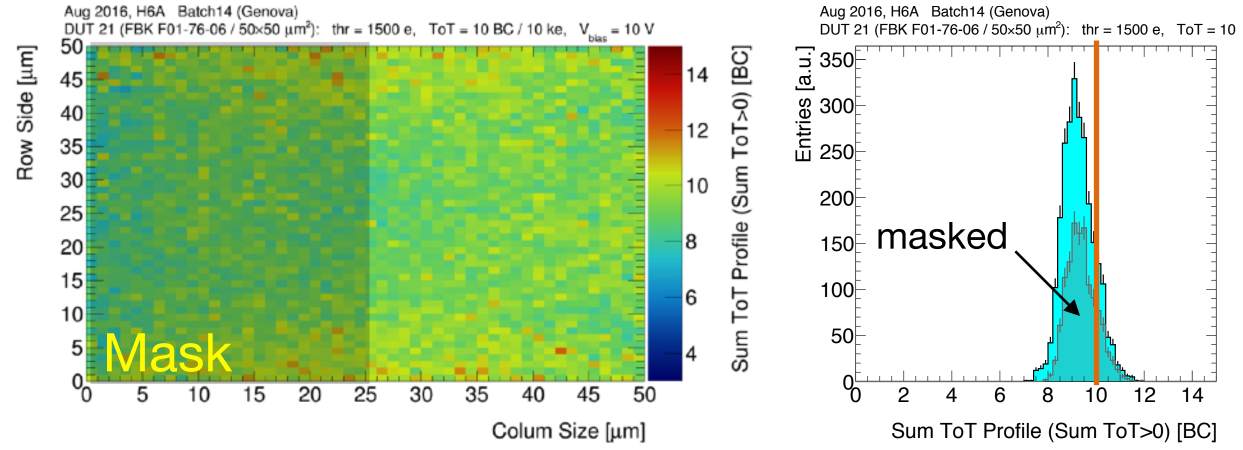
2V

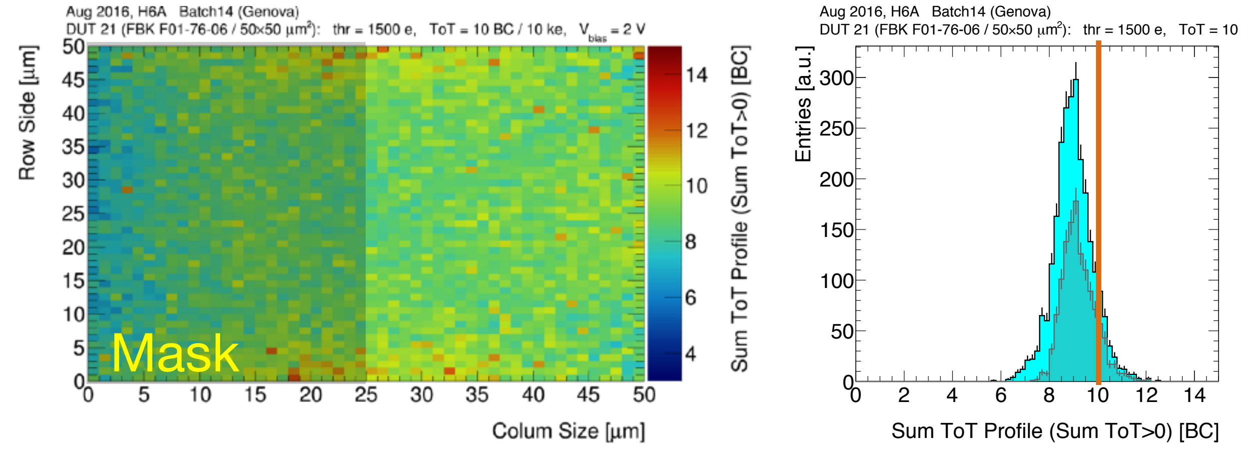
250x50



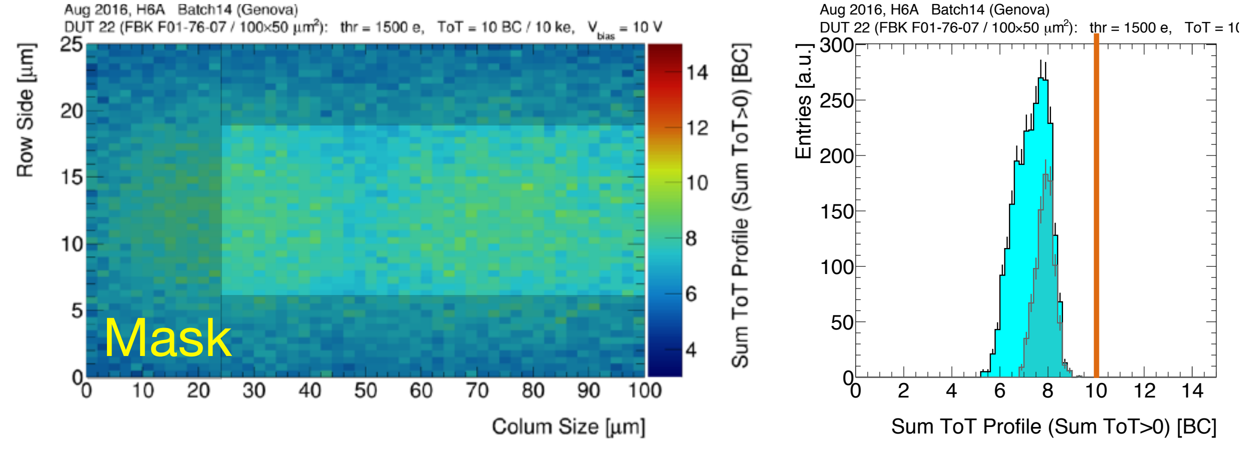


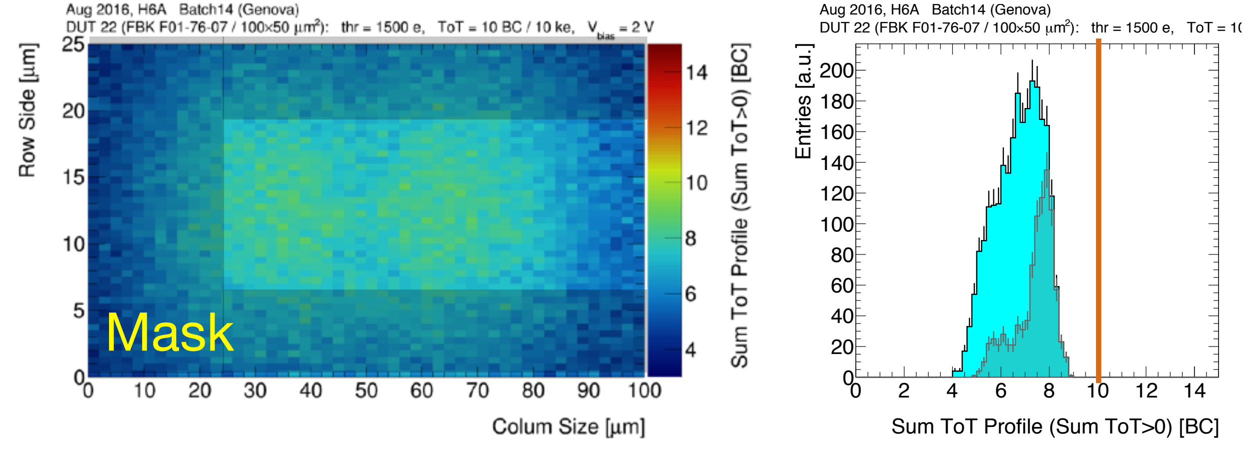
50x50





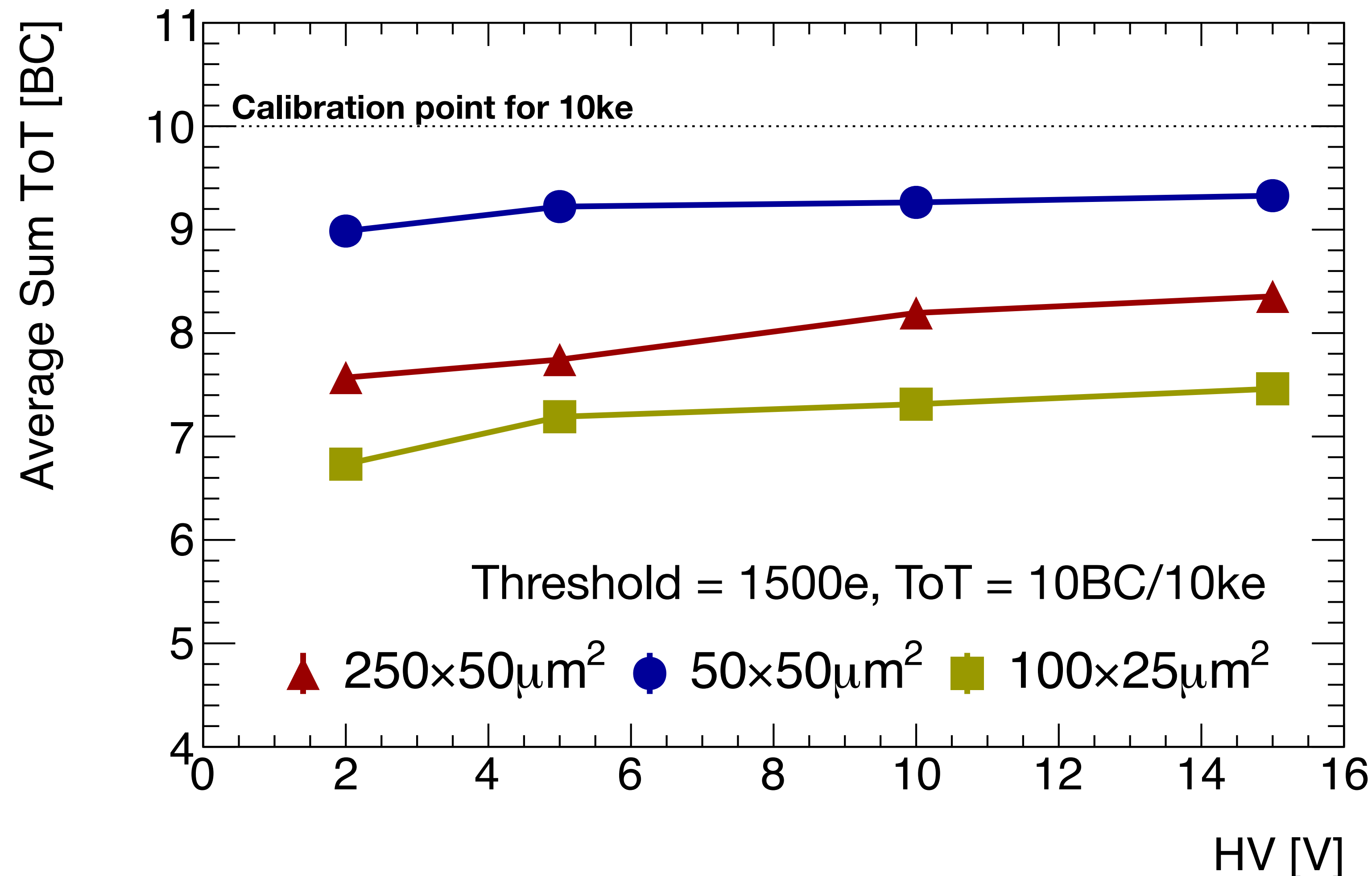
100x25

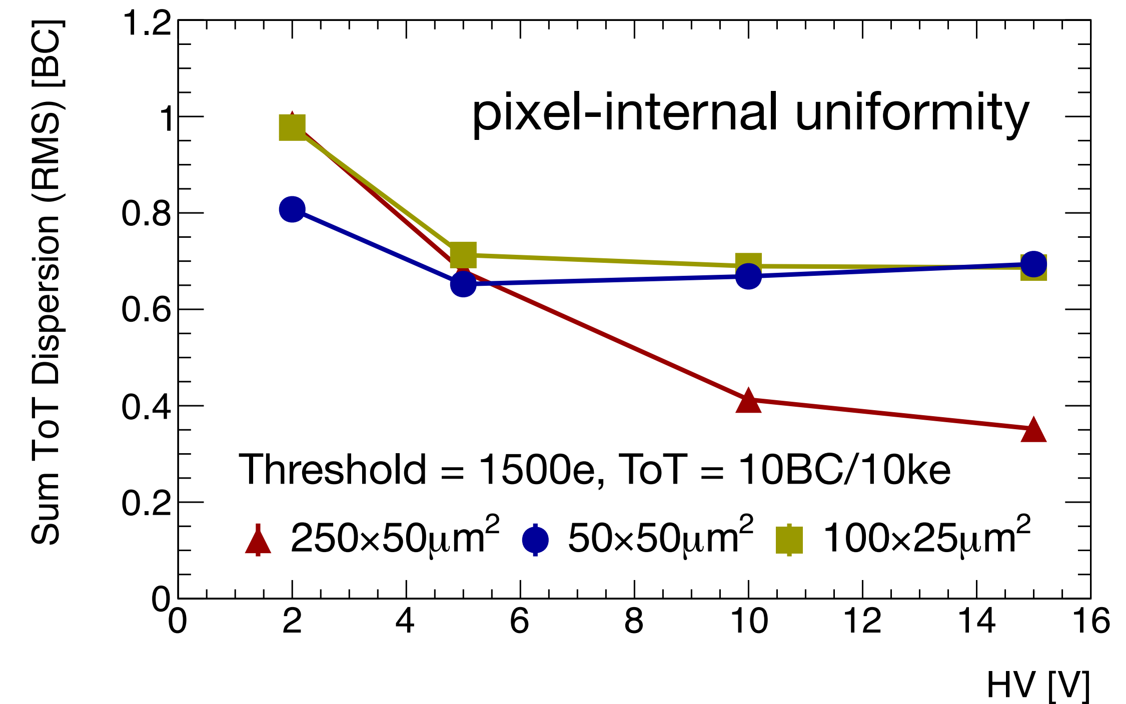




- Showing simple average for each cell (not doing Landau fitting for each cell).

Charge Collection: Cluster Sum ToT — HV dependence





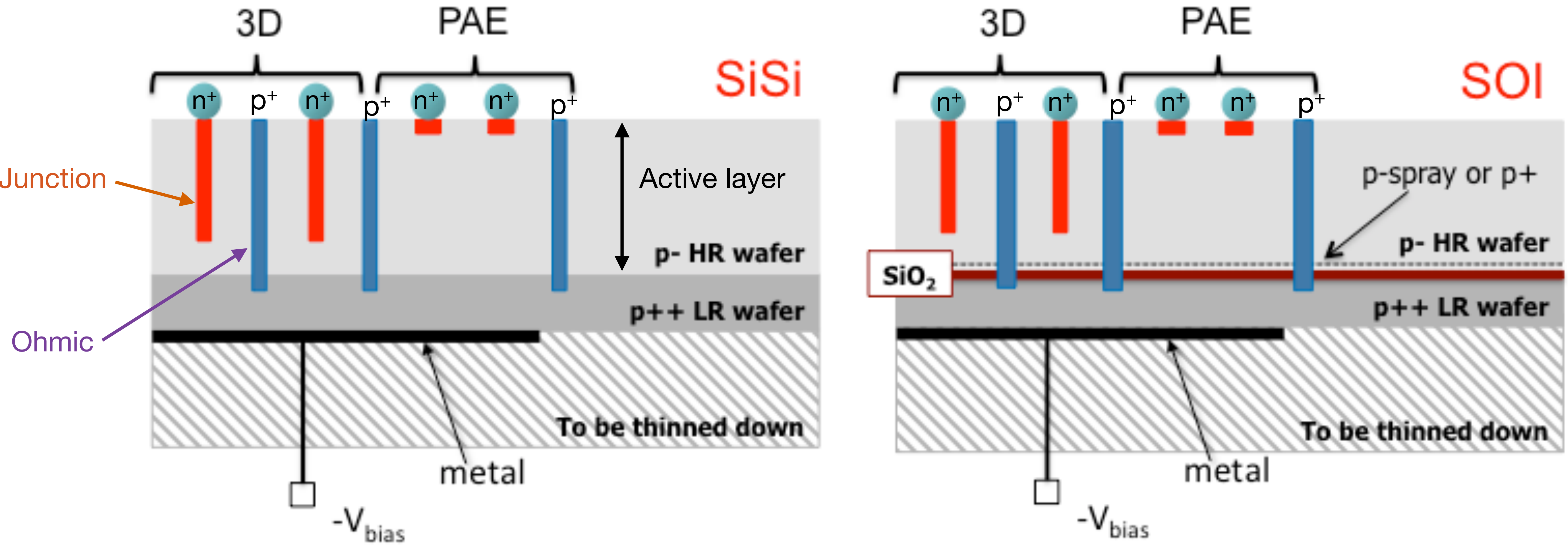
- Average cluster sum ToT gradually increases as a function of HV.
- Somewhat varying by the sensor type.
  - But also need to take into account the sampled readout for 50x50μm^2 and 100x25μm^2.
- Dispersion of 50x50μm^2 does not improve much by masking, and it is larger than 250x50μm^2.

Summary

- A first batch (9 wafers) produced in 2016
- 9 modules from W76 (130μm active thickness) were assembled to FEI4 and checked.
  - IV-curve
  - FE functionality
  - Source Scan (bump bonding check)
- Selected non-irradiated 3 modules of 50x50μm^2 (1E), 100x25μm^2 (1E), 250x50μm^2 (1E) are studied with the test beam dataset.
- Preliminary analysis results are given for:
  - Noise vs. HV
  - Hit efficiency vs. HV and tuning
  - Pixel-internal position dependence of efficiency, cluster size, cluster ToT
- The first look of the test beam results is generally reasonable wrt. expectation.
- Outlook: tests for high-irradiated samples to be carried out (being planned).

Backup

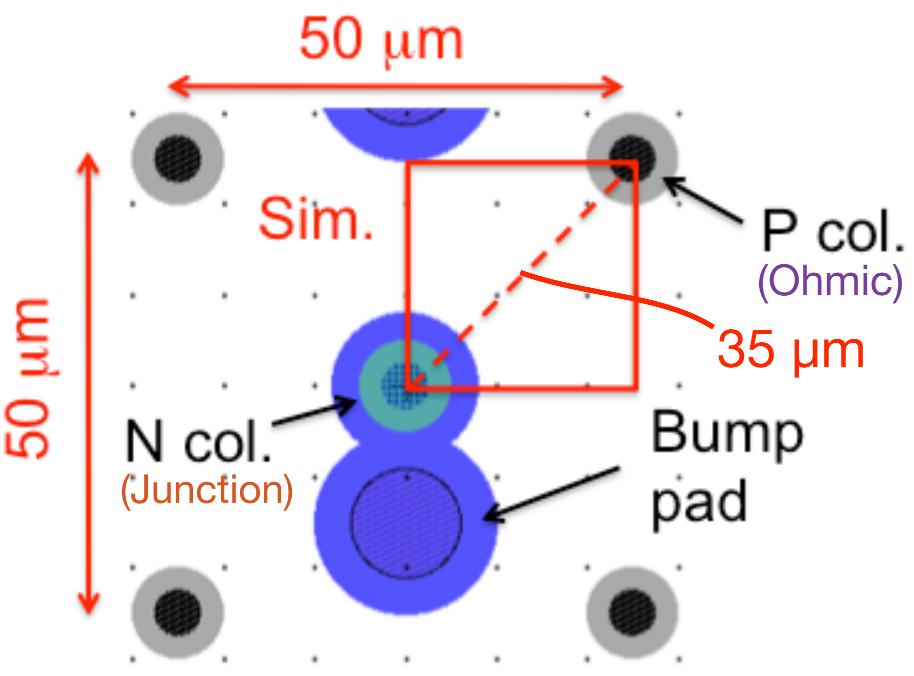
New single-sided approach to 3D + Planar Active Edge

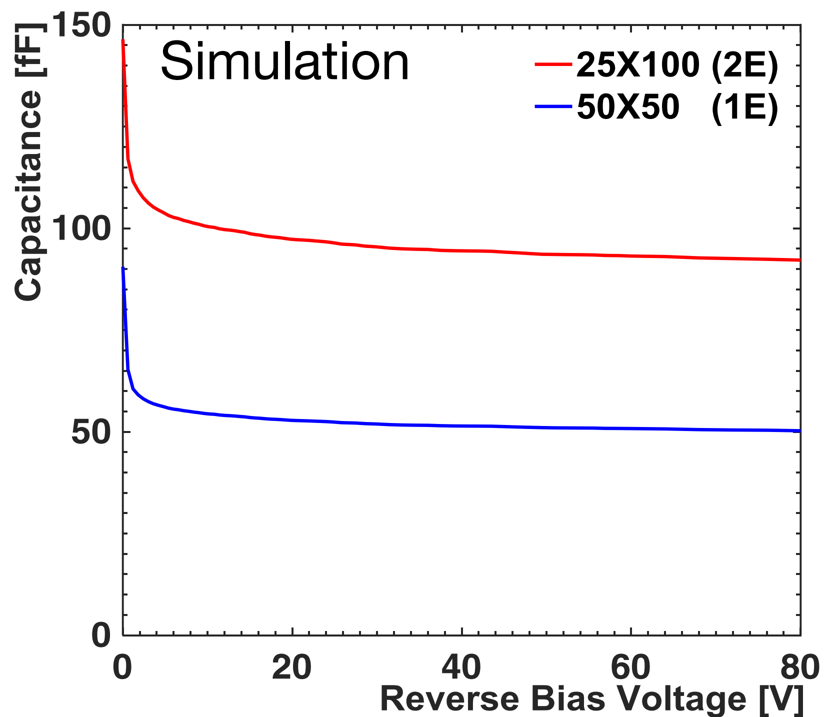


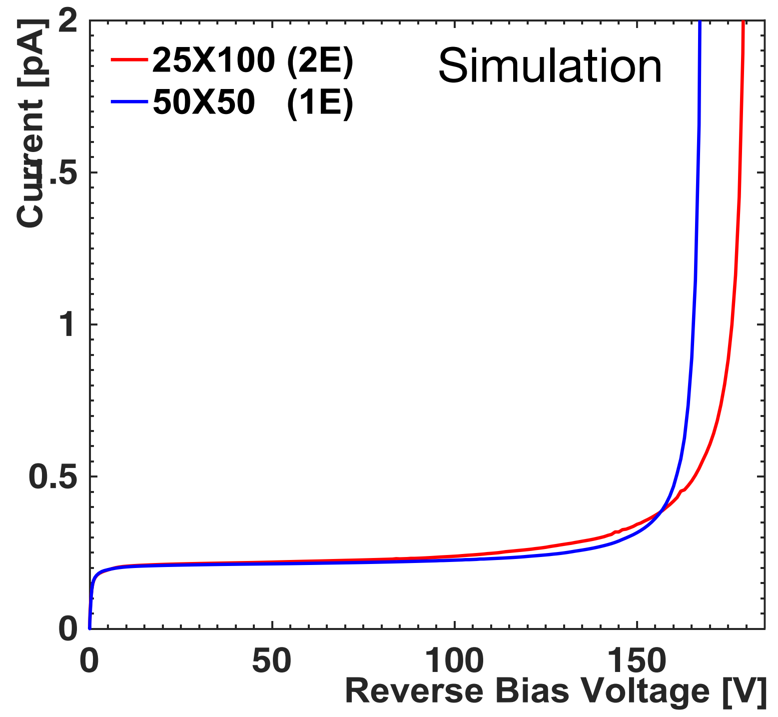
- Single-sided processes from the face is preferred for thin sensros, esp. for 6-inch wafers.
- Thin sensors on support wafer: SiSi or SOI → Substrate qualification
- Process Tests:
  - Ohmic columns/trenches depth > active layer depth (for V_{bias})
  - Junction columns depth < active layer depth (for high V_{bd})
  - Reduction of hole diameters to ~5 μm
  - Holes filled with poly-Si (at least partially)

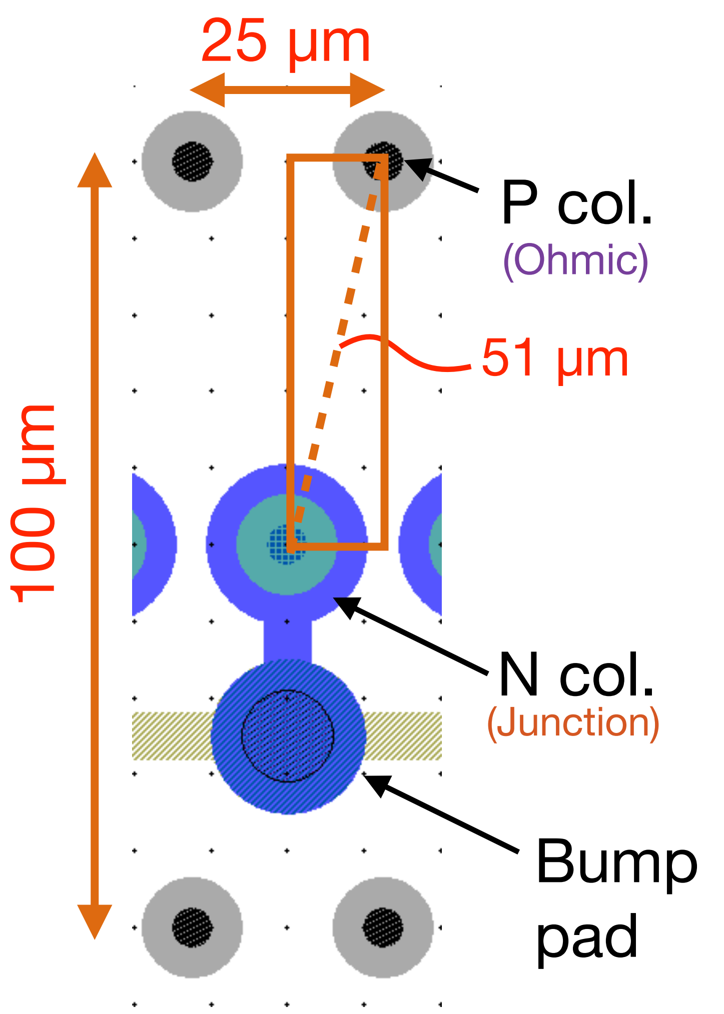
Pixel Layouts (150 μm thickness, 130 μm n⁺-column depth)

Plots by D M S Sultan



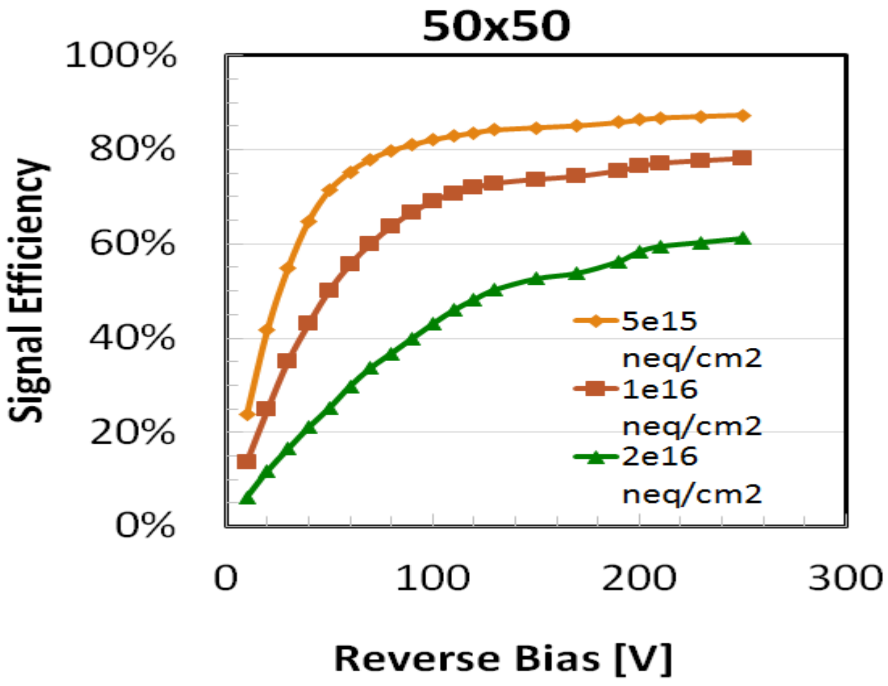


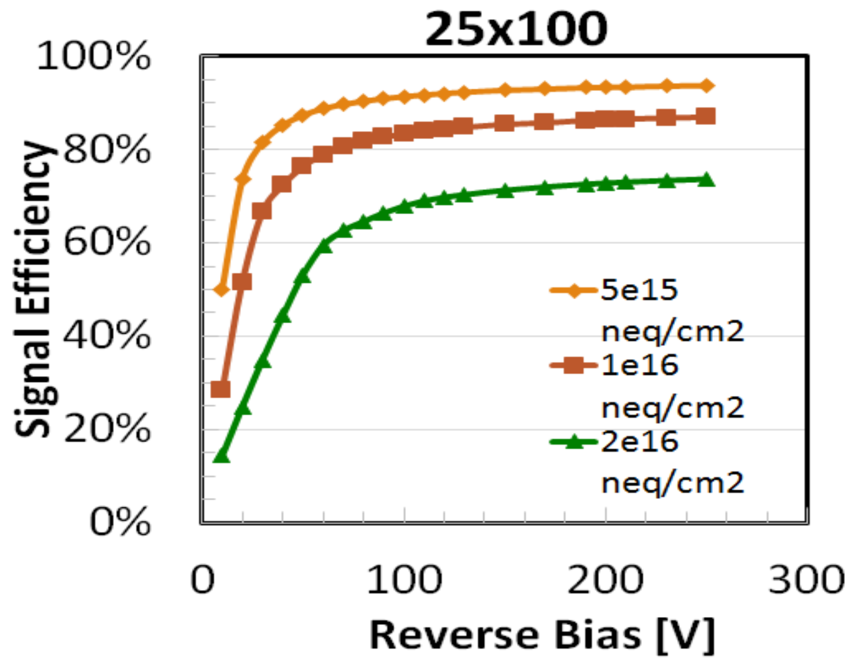




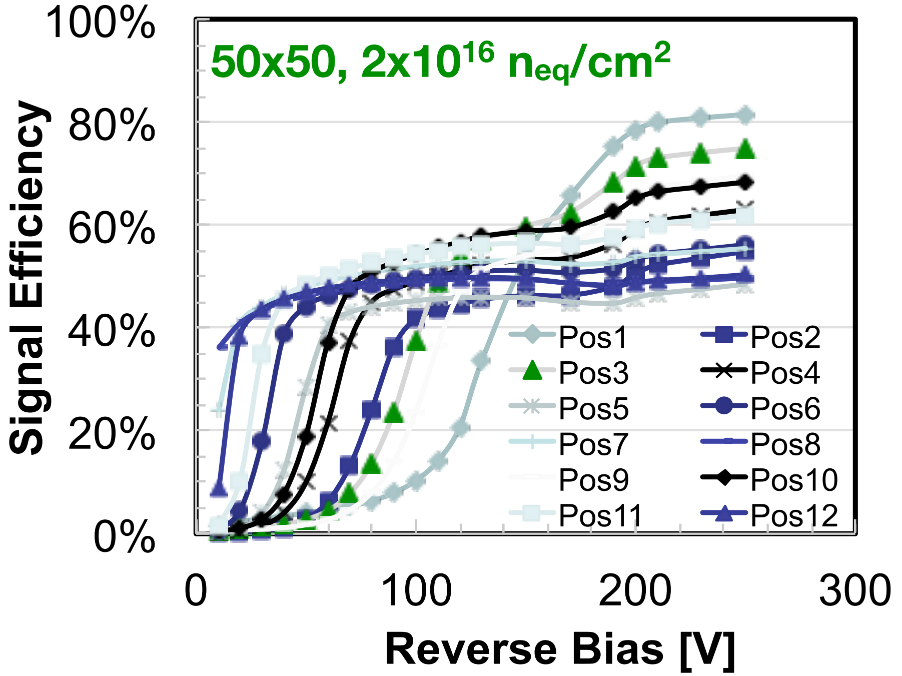
- Two newer pixel dimensions are considered: 50x50 and 25x100 (2E).
- Column diamter of ϕ=5 μm.
- 25x100 is challenging for clearance.
- Simulation calculates the capacitance is compatible with the RD53 specification of 100 fF, and the breakdown is high enough.

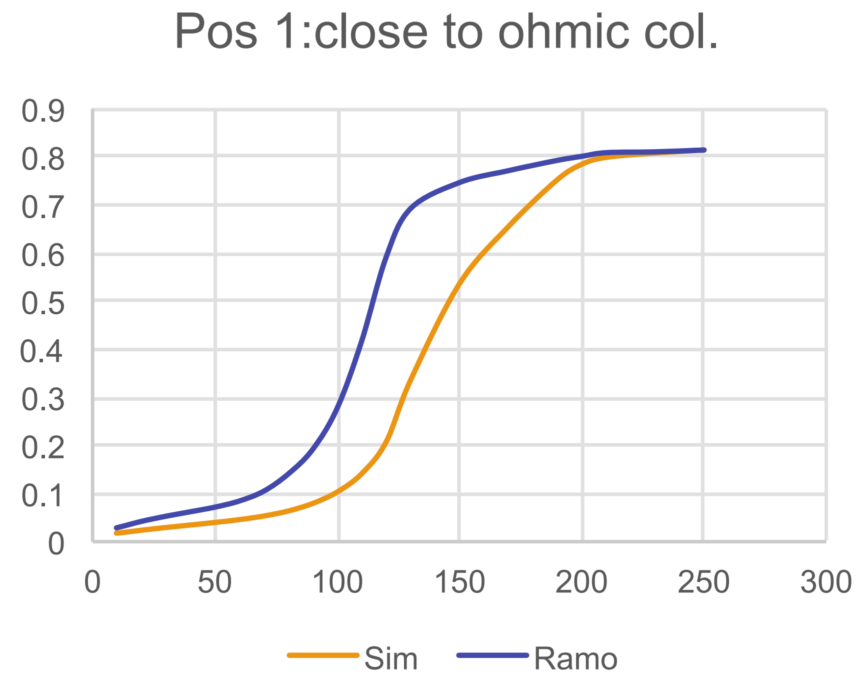
Simulated Performances - Signal Efficiency

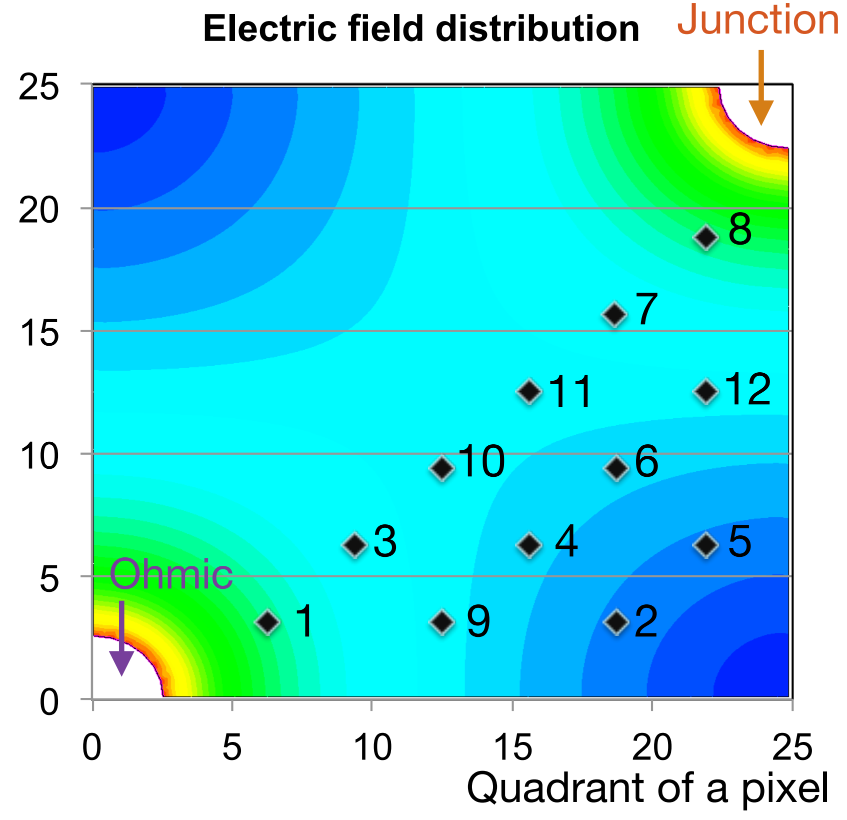




- Very high average signal efficiency.
- True values will be smaller due to pixel edge effects.



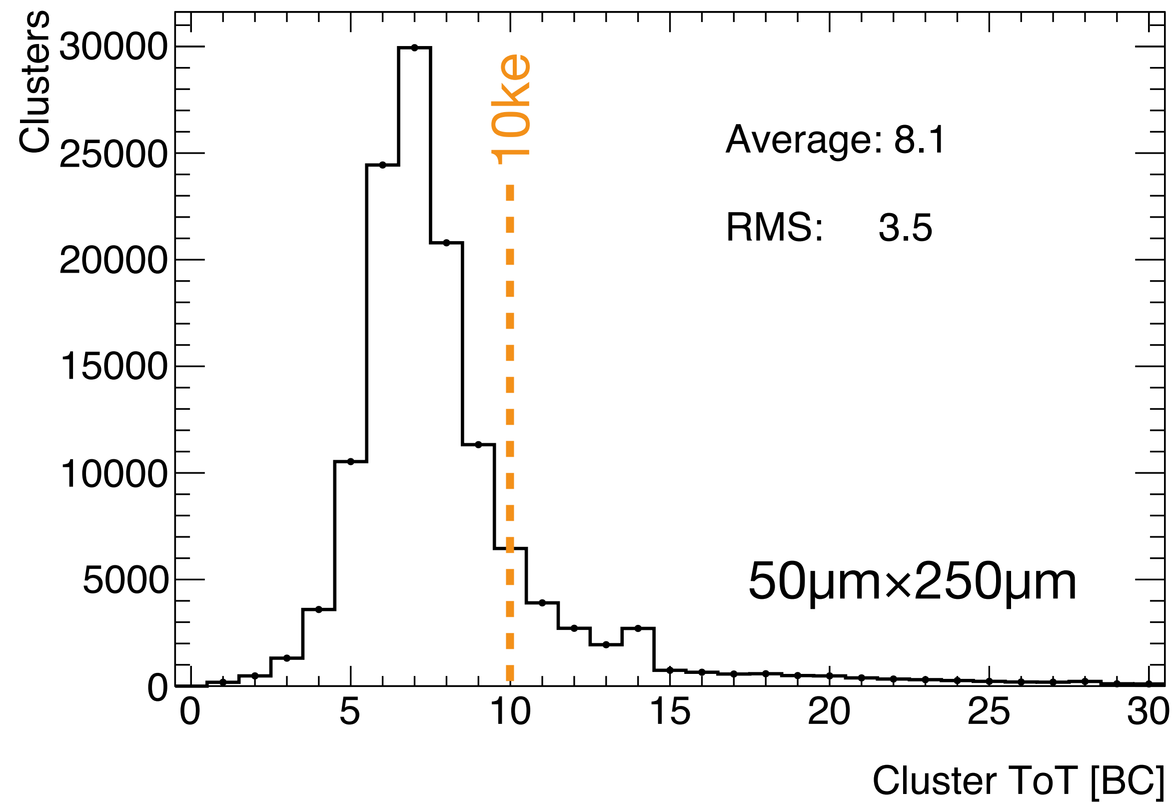


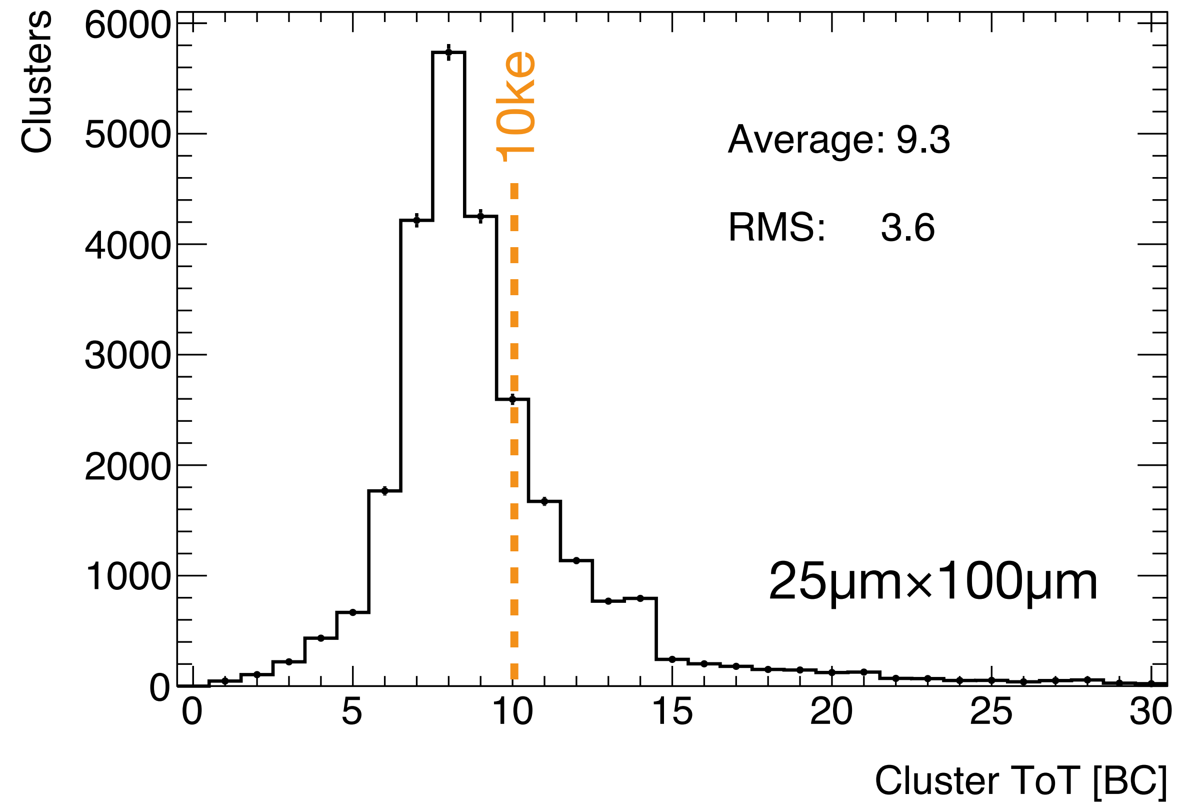


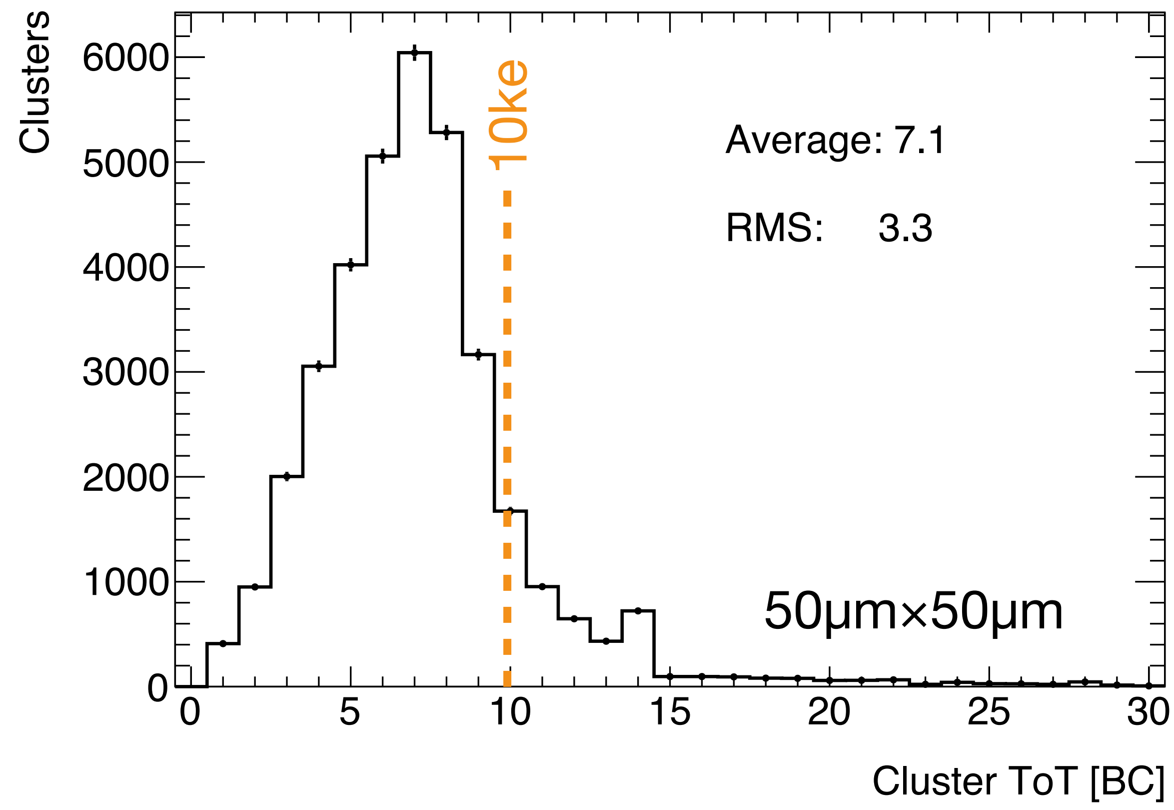
- The signal efficiency depends on the internal position of the pixel; qualitatively explained by Ramo's theorem.

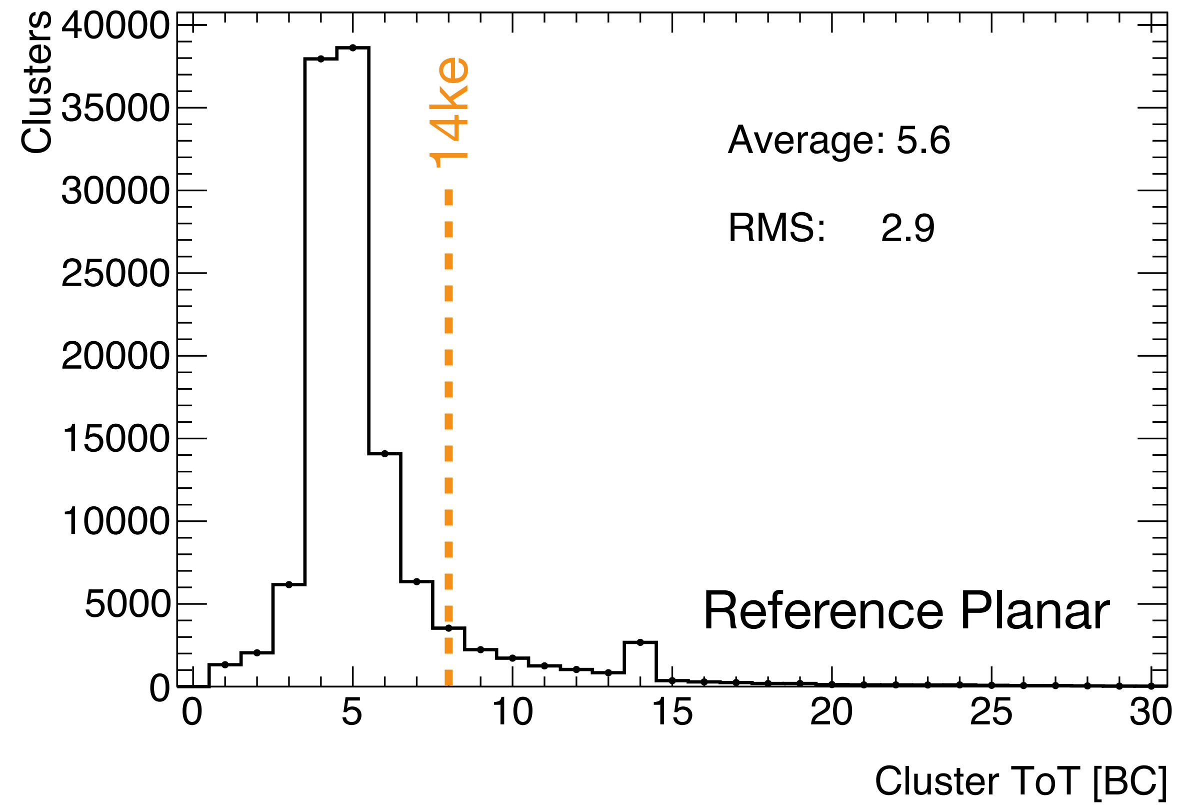
Quick Output (Last August)

1 run in 1500e, 10BC@10ke, 10V

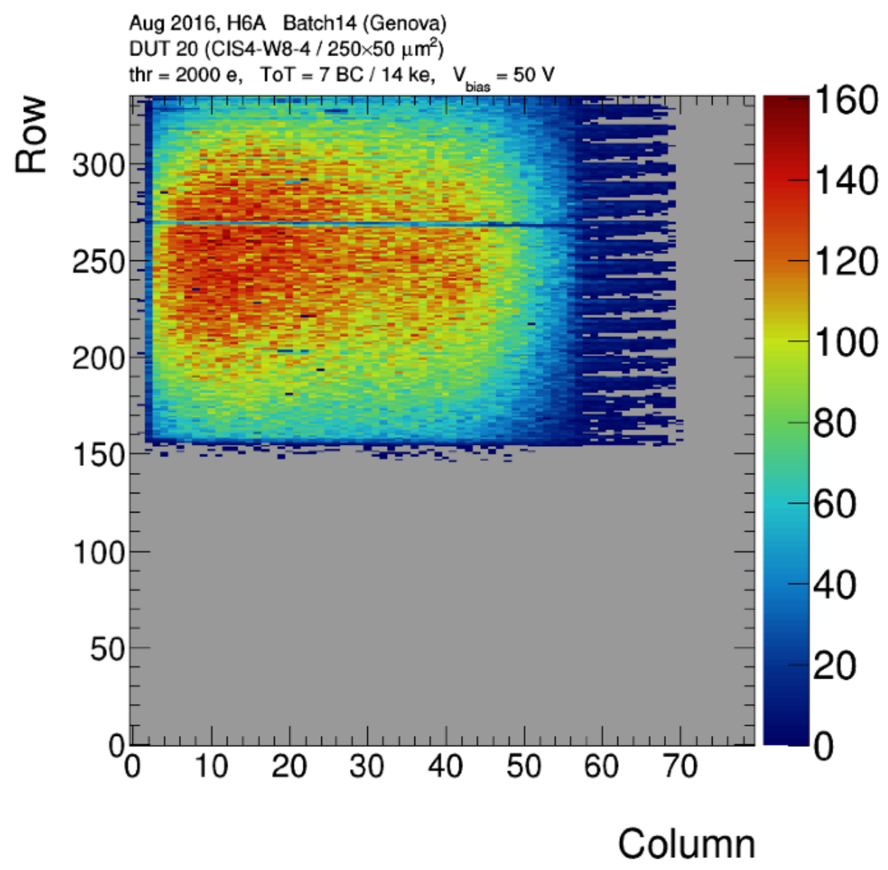


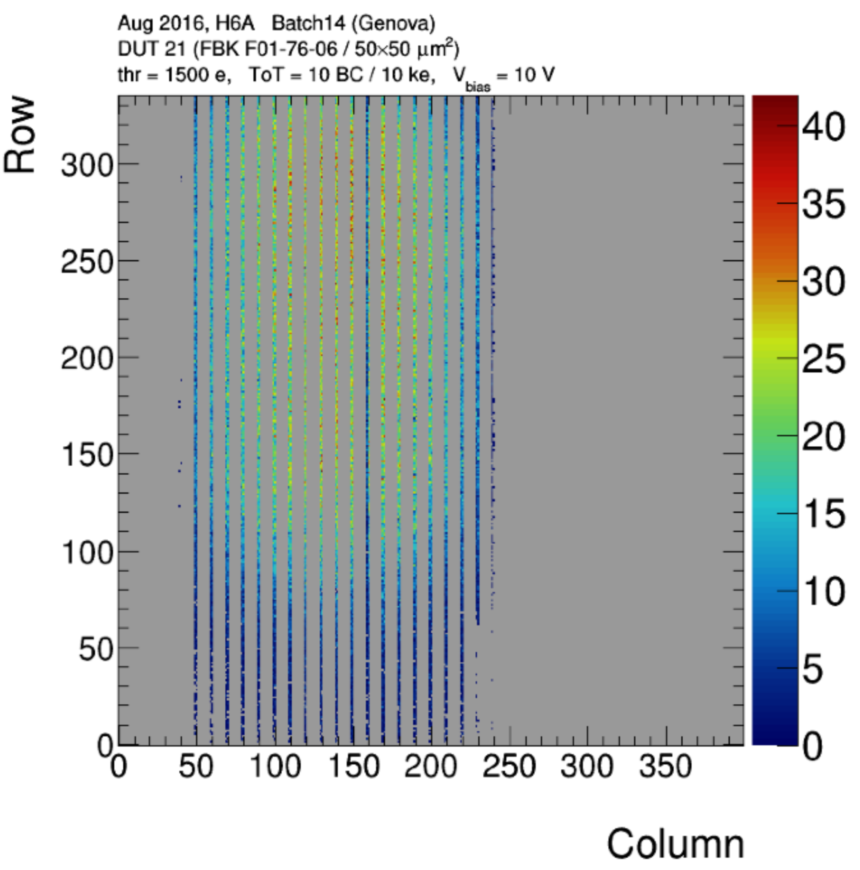




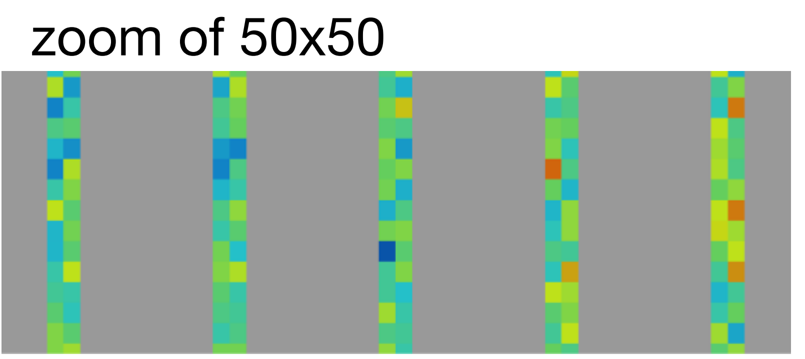


Hit map — adapted to the customised pixel sizes

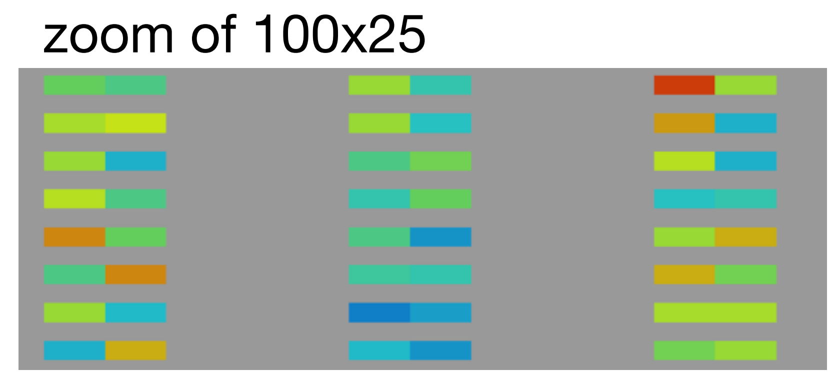


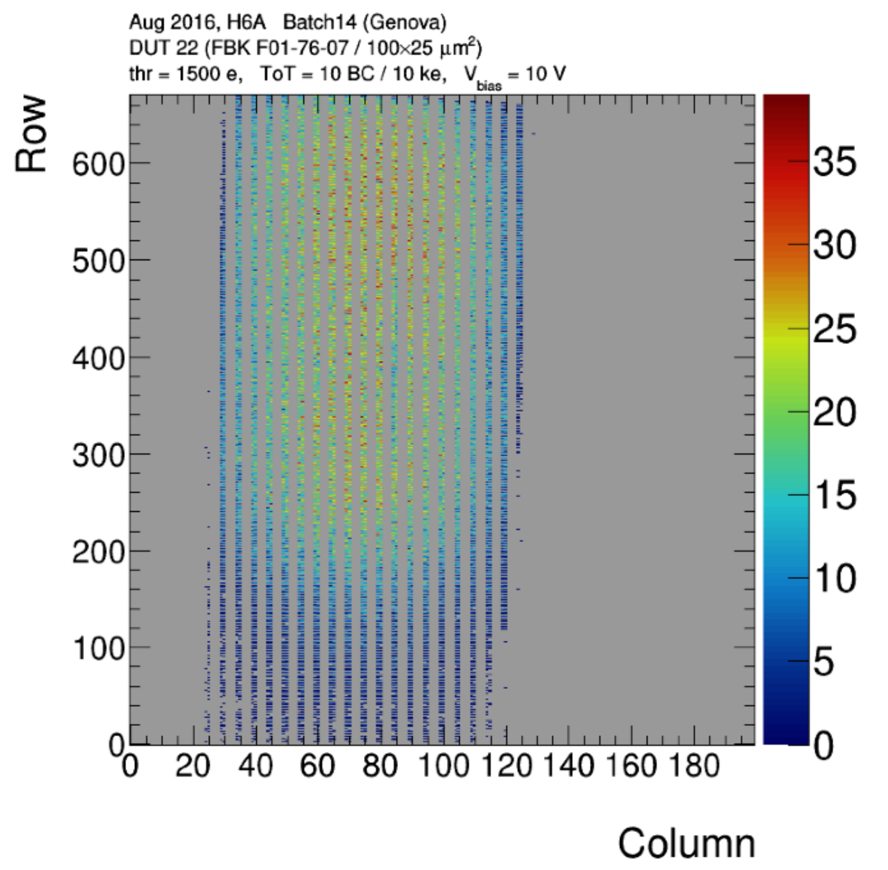


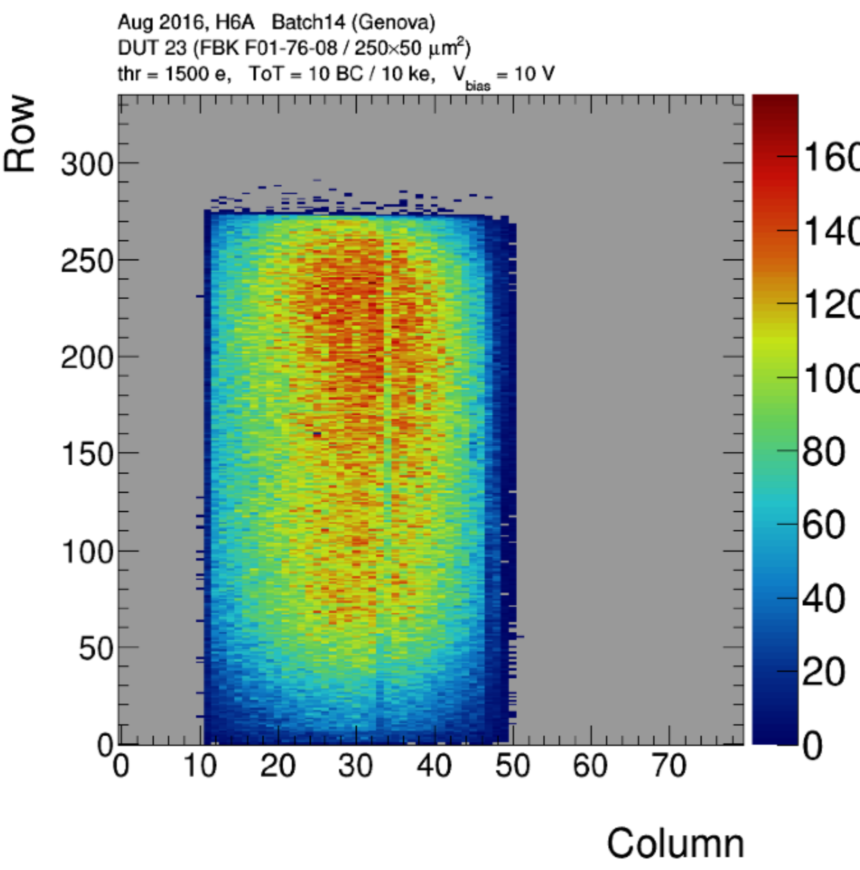
zoom of 50x50



zoom of 100x25







- Interpreting the pixel sensor size properly.
- Clustering is also accurate to take into account of geometries.