3D sensors measurements with FEi4 read-out chips

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New thin 3D pixel sensors on 6” p–type wafers at FBK.
- Work carried out within INFN RD_FASE2 and AIDA2020 projects.
- Targetted irradiation of $\Phi = 2 \times 10^{16}$ n$_{eq}$/cm$^2$ (regarding innermost pixel layers in HL-LHC).
- Layout compatible with FEI4 (for testing) and RD53 chips.
- Similar design layout to CNM 3D sensor prototypes (David’s talk).

A first batch (9 wafers) produced in 2016.
- Active thickness (130 µm or 100 µm) / Presence of poly–caps / ..

FEI4–compatible sensors of a 130µm–thick wafer bump–bonded at Leonardo (previously known as Selex).
- Multiple pixel layouts. including:
  { 250x50 µm$^2$ (2E), 50x50 µm$^2$ (1E), 100x25 µm$^2$ (1E) } (but not only).

Tests and Results
- Basic characterisation at the Genova lab.
- The first test beam of non–irradiated 3 modules in CERN SPS H6A.
The wafer layout

- **FE-I4**
  - 50x250 (2E) — std.
  - 50x50 (1E)
  - 25x100 (1E and 2E)
  - 25x500 (1E)

- **FE-I3**
  - 50x50 (1E)
  - 25x100 (1E and 2E)

- **PSI46dig**
  - 100x150 (2E and 3E) — std.
  - 50x50 (1E and 2E)
  - 50x100, 100x100 (2E and 4E)
  - 50x100, 100x150 (2E and 6E)
  - 25x100 (1E and 2E)

- **FCP**
  - 30x100 (1E)

- **RD53**
  - 50x50 (1E)
  - 25x100 (1E)
  - 25x100 (2E)

- **Other test structures**

13 sensors in total
W76 - 130 µm thickness, w/ poly-Cap - Sensor Breakdown

Deposition, cutting and assembly of W76 were done at Leonardo. 9 FE-I4 sensors of W76 were delivered in late July. W78 is ongoing.

* 9,11,12,13: rejected for either early breakdown or too-large $I_{\text{leak}}$
Samples for the Test Beam

This test beam: used 3 sensors
- 50×50(1E), 25×100(1E), 50×250(2E)
- Bump–bonded by Selex
- Non–irradiated

Larger current on some samples observed after assembly wrt. wafer measurement, to be investigated.

<table>
<thead>
<tr>
<th>ID</th>
<th>Size</th>
<th>Sensor $V_{bd}$ [V] after assembly</th>
<th>Basic electric qualification</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>25x100</td>
<td>24</td>
<td>N/A</td>
</tr>
<tr>
<td>2</td>
<td>25x500</td>
<td>15</td>
<td>N/A</td>
</tr>
<tr>
<td>3</td>
<td>50x250</td>
<td>25</td>
<td>N/A</td>
</tr>
<tr>
<td>4</td>
<td>50x50</td>
<td>15</td>
<td>GOOD</td>
</tr>
<tr>
<td>5</td>
<td>50x50</td>
<td>2</td>
<td>Too-low $V_{bd}$</td>
</tr>
<tr>
<td>6</td>
<td>50x50</td>
<td>12</td>
<td>GOOD</td>
</tr>
<tr>
<td>7</td>
<td>25x100</td>
<td>&gt;80</td>
<td>GOOD</td>
</tr>
<tr>
<td>8</td>
<td>50x250</td>
<td>12</td>
<td>GOOD</td>
</tr>
<tr>
<td>10</td>
<td>50x50</td>
<td>&gt;80</td>
<td>regulator broken</td>
</tr>
</tbody>
</table>
Bump Bonding to FE-I4: Source Scan

Note, only 20% of the pixels are read out w/ FE-I4.

²⁴¹Am Source Scan@Genova
**Noise measurements**

![Graph showing noise measurements for different module sizes and thresholds.](image)

- **Threshold scan with HV-on.**

- **Tuning was successful for the 3 modules in the all tuning targets.**

- **Wrt. 50x250 µm², 50x50µm² gives slightly less noises while 25x100µm² slightly more (consistent with each capacitance).**
Test Beam Setup - (CERN SPS H6A, Aconite)

- SPS H6A beam line, Aconite telescope.
- CIS4–W8–4 (single planar) as the reference.
- A tricky mechanical configuration due to the sub-optimal shape of the readout boards – needs improvements in the future.
- Tilt angle is not very accurately controlled (around 5° in row direction)
- Acquired dataset:
  - 2 cycles of HV scan at a fixed tuning (coarse/fine steps)
  - 1 set of tuning variation (threshold, ToT).
Short notes on data analysis

- Sparse readout for 50x50µm² and 100x25µm² sensors. → Customly implemented specialised geometry configurations.
- Acceptance of 50x50µm² and 100x25µm² is approximately 20%.
- Constraints on the cluster size:
  - 50x50 µm²: maximum size of 2 in the column direction.
  - 100x25 µm²: maximum size of 2 (1) in the column (row) direction.
HV Scan: Pixel-internal Efficiency (thr = 1500e, ToT = 10BC / 10ke)

- 250x50µm²
- 50x50µm²
- 100x25µm²

Odd/even columns are folded by mirror flipping (same for the following slides).
HV Scan: Cluster size vs. Position: 250x50µm² (thr = 1500e, ToT = 10BC / 10ke)

- { inefficient, size=1, size=2 } from top to bottom.
- Clear change of efficient region as a function of bias voltage.
Pixel Hit Map vs. Cluster size — 50x50 (F01-76-06)

Aug 2016, H6A Batch14 (Genova)
DUT 21 (FBK F01-76-06 / 50x50 μm²):
thr = 1500 e⁻, ToT = 10 BC / 10 ke⁻, V_{bias} = 10 V

Leaking
Sharing

Similar story for 100x25
ROI mask definition for hit efficiency estimation (Tentative)

- 250x50: unbiased.
- 50x50: hypothetically unbiased.
- 100x25: inevitably biased!!
**HV Scan: Hit efficiency (after masking)**

![Graph showing hit efficiency vs. HV for different sensor sizes.](image)

- **250×50μm²**: Efficiency is >99% above ~10 V. Ramping up up to ~10 V.
- **50×50μm²**: Keeping almost flat ~98% efficiency in 2 < HV < 15 V. Slight increasing of ~1%.
- **100×25μm²**: shown just for reference. Qualitatively similar trend to 50×50μm².
Variation of hit efficiency by tuning (after masking)

- A reasonable gradual change of efficiency by 1–2% is observed.
- 100x25μm²: shown just for reference.
Showing simple average for each cell (not doing Landau fitting for each cell).
Average cluster sum ToT gradually increases as a function of HV.

Somewhat varying by the sensor type.

But also need to take into account the sampled readout for 50x50μm² and 100x25μm².

Dispersion of 50x50μm² does not improve much by masking, and it is larger than 250x50μm².
A first batch (9 wafers) produced in 2016

9 modules from W76 (130µm active thickness) were assembled to FEI4 and checked.

- IV-curve
- FE functionality
- Source Scan (bump bonding check)

Selected non-irradiated 3 modules of 50x50µm$^2$ (1E), 100x25µm$^2$ (1E), 250x50µm$^2$ (1E) are studied with the test beam dataset.

Preliminary analysis results are given for:

- Noise vs. HV
- Hit efficiency vs. HV and tuning
- Pixel-internal position dependence of efficiency, cluster size, cluster ToT

The first look of the test beam results is generally reasonable wrt. expectation.

Outlook: tests for high-irradiated samples to be carried out (being planned).
Backup
New single-sided approach to 3D + Planar Active Edge

- Single-sided processes from the face is preferred for thin sensors, esp. for 6-inch wafers.
- Thin sensors on support wafer: SiSi or SOI → Substrate qualification
- Process Tests:
  - Ohmic columns/trenches depth > active layer depth (for $V_{bias}$)
  - Junction columns depth < active layer depth (for high $V_{bd}$)
  - Reduction of hole diameters to ~5 µm
  - Holes filled with poly-Si (at least partially)
Pixel Layouts (150 µm thickness, 130 µm n⁺-column depth)

- Two newer pixel dimensions are considered: 50x50 and 25x100 (2E).
- Column diameter of φ=5 µm.
- 25x100 is challenging for clearance.
- Simulation calculates the capacitance is compatible with the RD53 specification of 100 fF, and the breakdown is high enough.
Simulated Performances - Signal Efficiency

- Very high average signal efficiency.
- True values will be smaller due to pixel edge effects.

The signal efficiency depends on the internal position of the pixel; qualitatively explained by Ramo’s theorem.
Quick Output (Last August)

1 run in 1500e, 10BC@10ke, 10V

- 50µm×250µm Average: 8.1
  RMS: 3.5

- 25µm×100µm Average: 9.3
  RMS: 3.6

- 50µm×50µm Average: 7.1
  RMS: 3.3

- Reference Planar Average: 5.6
  RMS: 2.9
Hit map — adapted to the customised pixel sizes

- Interpreting the pixel sensor size properly.
- Clustering is also accurate to take into account of geometries.