This work aims to present the laboratory measurements of 3D devices optimized for the High Luminosity LHC Phase-2 upgrades, when the ATLAS tracker will be replaced to cope with the higher peak and total luminosities. The sensor technology and design are optimized for extreme radiation hardness ($2 \times 10^{16} n_{eq} cm^{-2}$) and pixel layout is compatible with the present FE-I4 chip of ATLAS and the future RD53A. While waiting for a new small pixel cell readout chip, some devices have been assembled with FE-I4 readout electronics.

3D first batch: 9 wafers produced, best two bumped in Leonardo (former Selex). Wafer 76: 6 inch, 130 µm active thickness. 130 µm n+-column depth, with poly-cap, ~10 kG are expected for a MIP.

- Ohmic columns/trenches depth > active layer depth (for bias)
- Junction columns depth < active layer depth (for high Vbd)
- Reduction of hole diameters to ~5 µm
- Holes (at least partially) filled with poly-Si

Mean noise measurements have been performed with ST Control software, recording the I-V curve for every module and selecting a suitable range of values for bias voltage.

This test has been performed for the three types of modules at three different threshold values, at a fixed ToT tuning dependence of 10BC@10ke. Measurements of threshold scans with HV on, give noise values related to bias voltage selected. Results showed are related to the threshold set at 2500e.

As presented in the graph, modules of 50x250 µm² and 50x50 µm² pixel are slightly less noisy than the 25x100 µm² device. This result is consistent with measurements performed at threshold values of 3000e and 1500e.