The impact of applying WildCards to disabled modules for FTK pattern banks on efficiency and data flow

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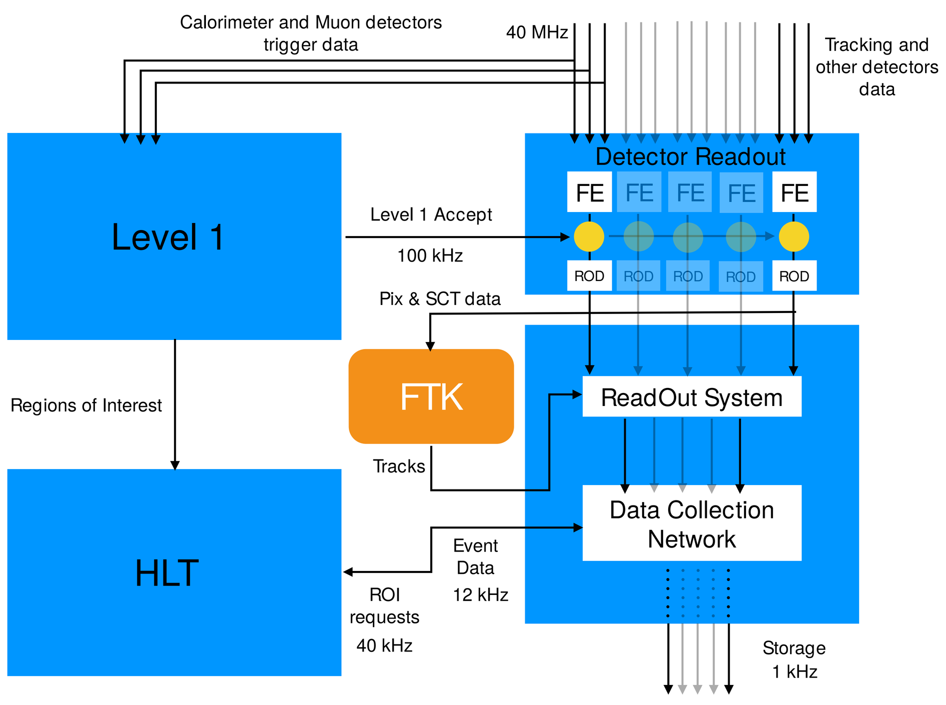
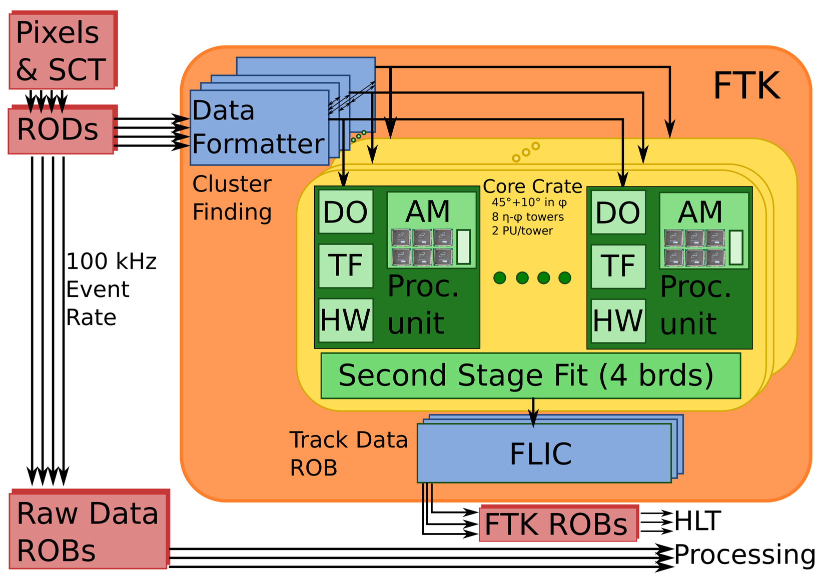
1 ATLAS Fast TracKer [1]

- A custom electronics system that reconstructs tracks in all events passing ATLAS L1 trigger [2];
- Reads data from silicon pixel and strip (SCT) detectors including Insertable B-layer (IBL) and operates up to $3 \times 10^{34} cm^{-2} s^{-1}$;
- Highly parallelized: divided into 4x16 ϕ x η regions ("towers") that process data simultaneously ;
- Provides track parameters and associated hits to HLT for all tracks with $p_T > 1$ GeV.



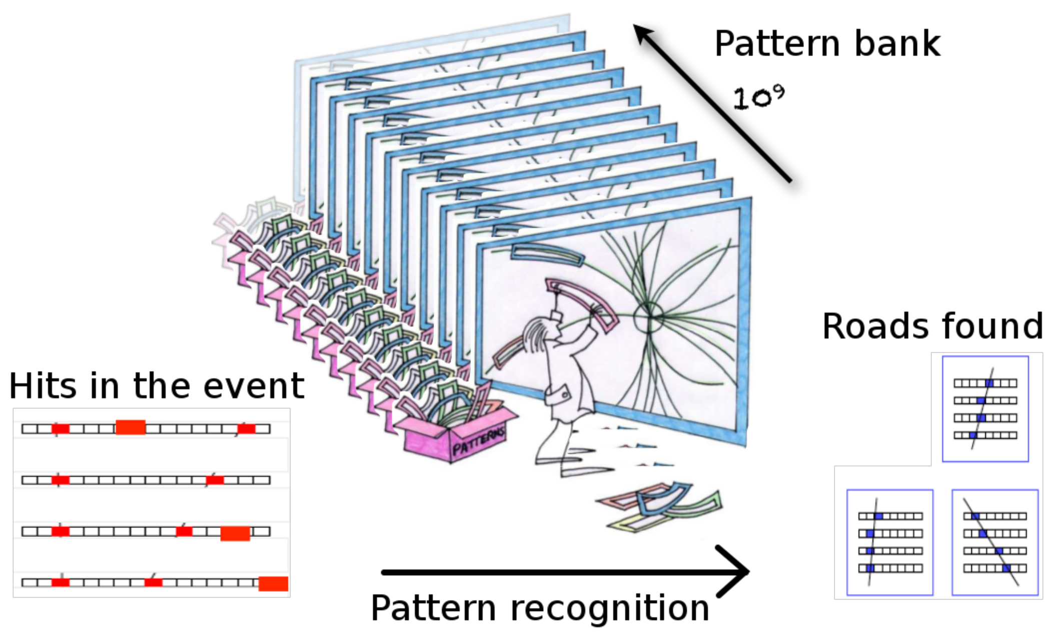
2 FTK System Design



- Pixel and strip data are transmitted from the Read Out Drivers (ROD) to the Data Formatters (DF).
- DF perform cluster finding and distribute hits according to FTK geometric segmentation ($\eta - \phi$ towers).
- The Associative Memories (AM) compare hits to 10^9 preloaded track patterns simultaneously.
- The Data Organizer (DO) receives the road ID number from the AM and fetches the associated full resolution hits then sends them to the Track Fitter (TF).
- Duplicate track removal is carried out by the Hit Warrior (HW).
- The Second Stage Boards (SSB) perform fit for the remaining 4 layers not used in the 1^{st} fit.
- The FTK Level 2 Interface Card (FLIC) organizes the tracks and sends them to the HLT ROSs.

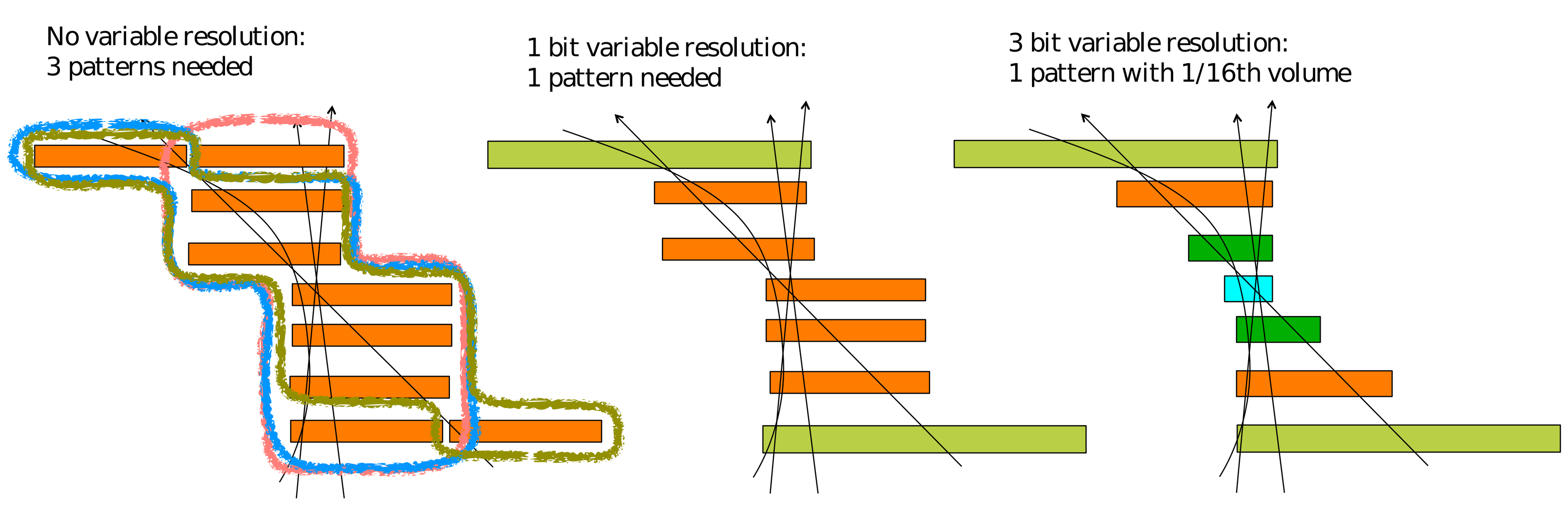
3 Pattern recognition

- The pattern recognition is the heart of FTK, a special Content Addressable Memory with 128K addresses per AM chip (1 billion in system) operating at 100 MHz.
- Data is simultaneously compared to predefined hit patterns (from simulated muons).
- Valid roads (matched patterns) where 7 or 8 layers have a match are used for the track fit.
- Pattern recognition is complete shortly after the last hit has been transmitted from the RODs.



4 Variable resolution (Don't Care (DC) bits)

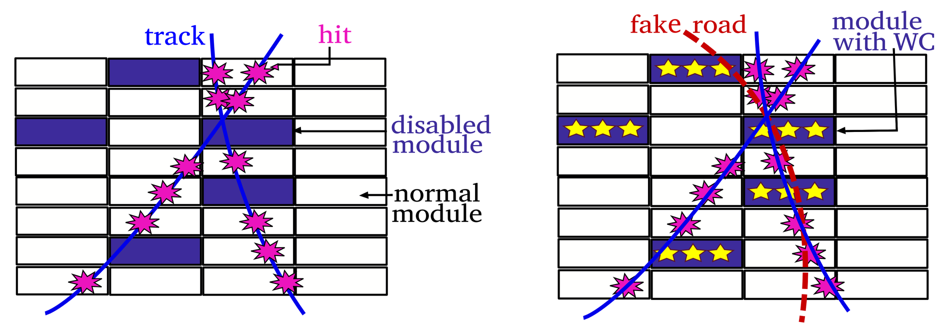
- To prepare the patterns bank used in the pattern recognition, one billion patterns per tower are generated. $\rightarrow$ Only 16.8M addresses are available in the AM chips.
- As a solution, variable resolution patterns is implemented using DC bits[3].

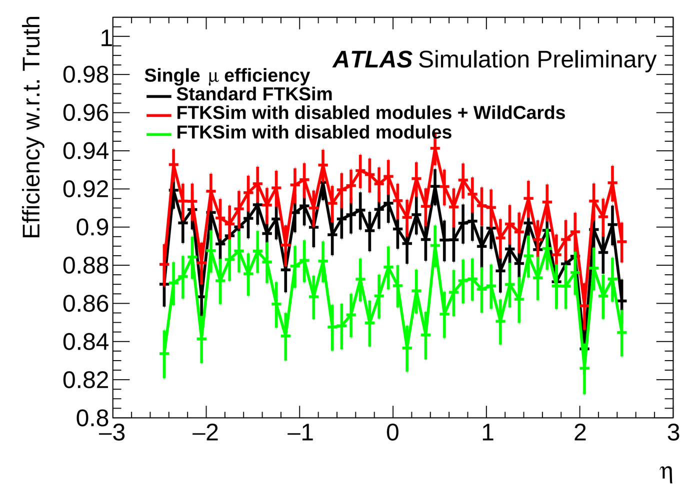


- Similar patterns, which differ only at the ternary bit positions, are merged in a single address.
- Variable resolution reduces the number of patterns and fake matches.

5 WildCards algorithm

- In the real state, there are some disabled modules in the pixel and in the SCT detectors, which cause a decrease in tracking efficiency by $\Delta\varepsilon \sim 2-4\%$.
- To recover the efficiency loss, we will use **WildCards (WC)** algorithm, which treats all strips/pixels in disabled modules as if they have hits always.
- WC algorithm improves efficiency while increasing the number of fake tracks which causes higher data flow, that may exceed the hardware limitation.
- To overcome this, WC penalty algorithm is used which control how to use WildCards with ternary bit, and thus avoids putting WildCards and wide patterns at the same time.





6 WildCards optimisation

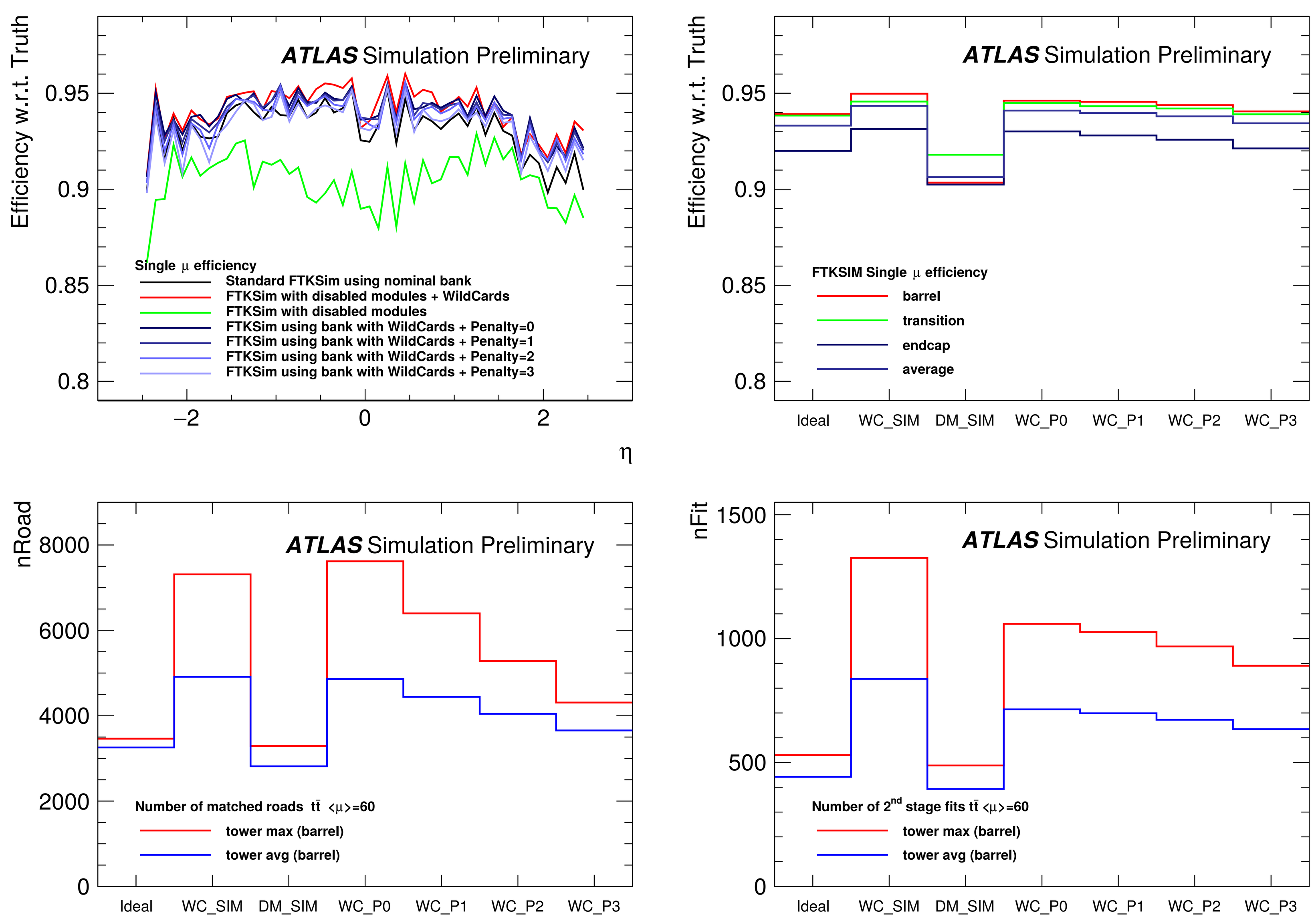
To optimize how to apply WC algorithm to achieve better performance we compare :

5 different patterns banks :

- Patterns bank for ideal detector (nominal bank);
- Four banks with WildCards and Penalty (from 0 to 3).

7 different FTK Simulation[4] with Single muons and $t\bar{t}$ $<\mu> = 60$.

- FTK Simulation using nominal bank (no disabled modules and no WildCards) (ideal) ;
- FTK Simulation using nominal bank with WildCards *set in simulation step* (WC_SIM);
- FTK Simulation using nominal bank with disabled modules *set in simulation step* (DM_SIM).
- Four FTK Simulations using bank with WC and Penalty(WC_P0, WC_P1, WC_P2, WC_P3).



7 Conclusions

- The patterns bank has direct effect on the patterns recognition and thus on the full FTK system.
- The existence of disabled modules leads to tracking inefficiency at level of $\Delta\varepsilon \sim$ 2-4%.
- With WildCards algorithm we can recover efficiency but we get also higher data flow.
- WildCards with penalty equal 3 seems to be the best choice: we can have a data flow close to the ideal bank while recovering the inefficiencies caused by disabled modules to a large extent.

References

[1] Annovi A et al. *ATLAS Fast TracKer (FTK) Technical Design Report, CERN-LHCC-2013-007, ATLAS-TDR-021, Geneva: CERN.* 2013.

[2] The ATLAS TDAQ Collaboration. *The ATLAS Data Acquisition and High Level Trigger system.* 2016.

[3] Stefan Schmitt. Am chip pattern recognition with optimized ternary bit usage. *Connecting the dots, Orsay, France*, 2017.

[4] Jahred Adelman et al. Atlas ftk challenge: simulation of a billion-fold hardware parallelism. *Procedia Computer Science*, 66:540–545, 2015.

Acknowledgements

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