Software-based data acquisition system for Level-1 end-cap muon trigger in ATLAS Run-3

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Upgrades for the ATLAS Run-3

- The ATLAS experiment will be upgraded for Run-3 (2021-2023).
  - The beam energy: $\sqrt{s} = 13 \rightarrow 14$ TeV
  - Luminosity: $L = 2 \times 10^{34} \rightarrow 3 \times 10^{34}$ cm$^{-2}$s$^{-1}$

- New inner muon station will be installed.
  - New trigger electronics has been developed for the Level-1 endcap muon trigger.
    - Maximum Level-1 trigger rate is limited to 100 kHz even in an increasing energy/luminosity.
    - More precise trigger logics needed to suppress the Level-1 trigger rate.

- The existing DAQ electronics also has been reformed.
  - Software-based data acquisition system (SROD)

![Diagram of ATLAS detector showing new trigger logic board and FPGA](image.png)
Figure 1.1: Cut-away view of the ATLAS detector. The dimensions of the detector are 25 m in height and 44 m in length. The overall weight of the detector is approximately 7000 tonnes. The ATLAS detector is nominally forward-backward symmetric with respect to the interaction point. The magnet configuration comprises a thin superconducting solenoid surrounding the inner-detector cavity, and three large superconducting toroids (one barrel and two end-caps) arranged with an eight-fold azimuthal symmetry around the calorimeters. This fundamental choice has driven the design of the rest of the detector.

The inner detector is immersed in a 2 T solenoidal field. Pattern recognition, momentum and vertex measurements, and electron identification are achieved with a combination of discrete, high-resolution semiconductor pixel and strip detectors in the inner part of the tracking volume, and straw-tube tracking detectors with the capability to generate and detect transition radiation in its outer part.

High granularity liquid-argon (LAr) electromagnetic sampling calorimeters, with excellent performance in terms of energy and position resolution, cover the pseudorapidity range $|\eta| < 3$. The hadronic calorimetry in the range $|\eta| < 1.7$ is provided by a scintillator-tile calorimeter, which is separated into a large barrel and two smaller extended barrel cylinders, one on either side of the central barrel. In the end-caps ($|\eta| > 1.5$), LAr technology is also used for the hadronic calorimeters, matching the outer $|\eta|$ limits of end-cap electromagnetic calorimeters. The LAr forward calorimeters provide both electromagnetic and hadronic energy measurements, and extend the pseudorapidity coverage to $|\eta| = 4.9$.

The calorimeter is surrounded by the muon spectrometer. The air-core toroid system, with a long barrel and two inserted end-cap magnets, generates strong bending power in a large volume within a light and open structure. Multiple-scattering effects are thereby minimised, and excellent muon momentum resolution is achieved with three layers of high precision tracking chambers.
ATLAS Trigger and Data Acquisition System

Figure 1.1: Cut-away view of the ATLAS detector. The dimensions of the detector are 25 m in height and 44 m in length. The overall weight of the detector is approximately 7000 tonnes.

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High granularity liquid-argon (LAr) electromagnetic sampling calorimeters, with excellent performance in terms of energy and position resolution, cover the pseudorapidity range $|\eta| < 3.2$.

The hadronic calorimetry in the range $|\eta| < 1.7$ is provided by a scintillator-tile calorimeter, which is separated into a large barrel and two smaller extended barrel cylinders, one on either side of the central barrel. In the end-caps ($|\eta| > 1.5$), LAr technology is also used for the hadronic calorimeters, matching the outer $|\eta|$ limits of end-cap electromagnetic calorimeters. The LAr forward calorimeters provide both electromagnetic and hadronic energy measurements, and extend the pseudorapidity coverage to $|\eta| = 4.9$.

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- Thanks to the software-based system:
  - it is flexible for modifications.
  - it is easy to debug.

- SROD can take advantage of the latest developments in computing industry.
Endcap muon trigger logic boards calculate muon $p_T$.  
- **Send the results to Central Trigger Processor.**

Magnetic fields bends the track  
(For example, $1.03 < |\eta| < 1.9$)  
Experimental hall  
Counting room  

**Endcap Level-1 Muon Trigger and Readout System**

**5**  

**ATLAS Muon Spectrometer Sub-systems:**  
- CSC – Cathode Strip Chambers  
- MDT – Monitored Drift Tubes  
- RPC – Resistive Plate Chambers  
- TGC – Thin Gap Chambers

**Trigger chambers**  
(on-detector electronics)  

**Other detector**  

**Trigger logic boards × 12**  

**Central trigger processor**  

**Special Interface Electronics**  

**Distributor of Timing, Trigger and Control signal**  

**10 GbE Network switch**  

**Ethernet**  

**SROD**
Level-1 trigger decision is done by CTP.

- **Muon system receives a signal related to the Level-1 trigger.**

(For example, $1.03 < |\eta| < 1.9$)

Experimental hall

Counting room

<table>
<thead>
<tr>
<th>Level-1 Trigger</th>
<th>The maximum rate is <strong>100 kHz</strong></th>
</tr>
</thead>
</table>

(For example, $1.03 < |\eta| < 1.9$)

Experimental hall

Counting room
Endcap Level-1 Muon Trigger and Readout System

- To record raw data related to the Level-1 trigger
  - Each board sends the hit information to SROD via Ethernet.

![Diagram of Endcap Level-1 Muon Trigger and Readout System]

- Data size ~ 2000 bit/event/board
- Data size: 160 bit/event

(For example, $1.03 < |\eta| < 1.9$)

Experimental hall

Counting room

Distributor of Timing, Trigger and Control signal

SiTCP realizes the TCP/IP communication!

10 GbE Network switch

SROD

Central trigger processor

ROS

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To record raw data related to the Level-1 trigger:

- Each board sends the hit information to SROD via Ethernet.

Central trigger processor

- Trigger logic boards × 12
- Distributor of Timing, Trigger and Control signal
- SROD × 1

This unit:
- trigger logic boards × 12
- Sync-signal distributor × 1
- SROD × 1

is for 1/6 endcap muon system.

(For example, 1.03 < |η| < 1.9)

Experimental hall

Counting room

Ethernet

10 GbE
Network switch
To record the hit information related to the Level-1 trigger:

- Each board sends the hit information to SROD via Ethernet.

Central trigger processor

SROD: Multi-process architecture

**Sub-systems:**
- CSC – Cathode Strip Chambers
- MDT – Monitored Drift Tubes
- RPC – Resistive Plate Chambers
- TGC – Thin Gap Chambers

**Precision chambers:**

**Trigger chambers:**

(For example, \(|\eta| > 1.9\))

**Special Interface Electronics**

**Sync-signal distributor**

**Trigger logic boards**

× 12

**Ethernet**

**Network switch**

**10 GbE**

**Cavern**

**Counting room**

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Kosuke Takeda (Kobe University)
Collector processes:
- The total number of processes is 13.
- Collect data from each electronics.
  - The number of these processes equal to the number of boards.
- Write it to the subsequent shared memory.
To record the hit information related to the Level-1 trigger:

- Each board sends the hit information to SROD via Ethernet.

**Central trigger processor**

- **A TLAS Muon Desk Shifter Training - General Introduction**

**Sub-systems:**

- CSC – Cathode Strip Chambers
- MDT – Monitored Drift Tubes
- RPC – Resistive Plate Chambers
- TGC – Thin Gap Chambers

**Precision chambers**

- **Trigger chambers**

- **on-detector electronics**

- **other detector on-detector electronics**

**Counting room**

- **Cavern**

**Ethernet**

**Special Interface**

**Electronics**

- **Sync-signal distributor**
- **Trigger logic boards**

**Ring buffer:**

- The total number of memories is 13.
- is the shared memory to absorb arrival delays.
  - The number of the share memory equal to the number of the collector processes.
- has control parameters.
  - The collector processes check this parameter when they write data to this buffer.
To record the hit information related to the Level-1 trigger:

- Each board sends the hit information to SROD via Ethernet.

Central trigger processor

The ATLAS Muon Spectrometer sub-systems:

- CSC – Cathode Strip Chambers
- MDT – Monitored Drift Tubes
- RPC – Resistive Plate Chambers
- TGC – Thin Gap Chambers

Precision chambers

Trigger chambers

Event builder process:

- builds an event.
  - Read data from the ring buffers
  - Check the IDs
- sends it to ROS.
  - By using the special PCIe card.

SROD: Multi-process architecture
To record the hit information related to the Level-1 trigger, each board sends the hit information to SROD via Ethernet.

The ATLAS Muon Spectrometer Sub-systems:
- CSC – Cathode Strip Chambers
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Counting room → Cavern → Ethernet (For example, $|\eta| > 1.9$)

10 GbE Network switch

MsgReporter process:
- collects messages from each process and posts it to the ATLAS message reporting system.

RunControlDriver process:
- to synchronize the process sequence with the central system.
After building an event, SROD sends it to ROS via S-LINK. S-LINK is a CERN specification. ROS collects data and serve it to high-level trigger.

New PCIe card for S-LINK connection[2]
- Developing with TokushuDenshiKairo Inc.
  - Using Xilinx Kintex-7 FPGA XC7K160T
  - PCIe x4
- Three types of output ports
  - Optical output × 2 (SFP+)
    - To send data to subsequent systems
  - Open-drain output
    - To send BUSY signal to the external system
  - NIM output × 1 and NIM input × 2

SROD performance

- The SROD performance has been measured.
  - In Run-3:
    - The average Level-1 trigger rate is 100 kHz.
    - The average event size is ~ 2000-bit.

- SROD has good performance.
  - The processing speed is higher than the requirement.
    - This bottleneck is coming from the network switch.
Software-based DAQ system has been developed for the Level-1 endcap muon trigger at higher luminosity run.

- To receive trigger data from new trigger logic boards.
  - Current DAQ system can’t handle these large data at high rate.

- Basic concepts:
  - Multi-process architecture
  - A special PCIe card is implemented.

Performance test has been done.

- This system can run at 100 kHz.

- The measured processing speed on SROD is enough good to use at Run3.
  - Current error handling procedures should be improved.
  - Monitoring functions should be more enhanced.
backup slides
The upgrade motivation

- Fake triggers will be more reduced by the new inner detectors.
  - New Small Wheel
    - $1.3 < \eta < 2.4$
  - RPC BIS 7/8
    - $1.0 < \eta < 1.3$ in small sectors

The coincidence between TGC-BW and these detectors will be used in Run-3

The existing inner detector:
- Tile Calorimeter
  - $1.0 < \eta < 1.3$
- EIL4
  - $1.0 < \eta < 1.3$ in Large sectors

RPC BIS 7/8

$1.0 < \eta < 1.3$ in small sectors

The existing inner detector: Tile Calorimeter

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RPC BIS 7/8

$1.0 < \eta < 1.3$ in small sectors

The existing inner detector: Tile Calorimeter

- $1.0 < \eta < 1.3$
Firmware has two main flows.

- Trigger data can be used for the online monitoring, trigger analysis, and commissioning.

This technology connects FPGA to Ethernet.

- SROD can correct data using TCP/IP.

The trigger Logic board for Run-3

Optical inputs and outputs
- SFP+ with GTX in FPGA
- 12 optical inputs from NSW, Tile Calorimeter, RPC BIS 7/8.
- 2 optical outputs to MuCTPi. (10 optical outputs for spares.)

Optical inputs
- SFP RX + G-Link RX chip
- 14 optical inputs from TGC-BW and EIL4.

FPGA (Xilinx Kintex-7 XCK410T)
CPLD (XC2C256-7PQ208C) for VME control
BPI (PC28F256P30TF) for FPGA configuration
RJ45 connector for readout (SiTCP)
16-pin connector for TTC
LEMO IN/OUT
Data size

Input data to SROD

- This input data will be suppressed at the trigger logic board.
  - [31:16] : header
  - [15:0] : data

<table>
<thead>
<tr>
<th>[31:16]</th>
<th>[15:0]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Trigger decision data</td>
<td>256 bit (Fixed)</td>
</tr>
<tr>
<td>Trigger decision data</td>
<td>1152 bit</td>
</tr>
<tr>
<td>Data from NSW</td>
<td>192 bit (Fixed)</td>
</tr>
<tr>
<td>Data from new RPC</td>
<td>192 bit</td>
</tr>
<tr>
<td>Data from new RPC</td>
<td>96 bit</td>
</tr>
<tr>
<td>ID information from NSW</td>
<td>32 bit (Fixed)</td>
</tr>
<tr>
<td>ID information from new RPC</td>
<td>200 bit</td>
</tr>
<tr>
<td>Data from Tile Calorimeter</td>
<td></td>
</tr>
<tr>
<td>Data from TGC-BW</td>
<td></td>
</tr>
<tr>
<td>Data from TGC-BW</td>
<td></td>
</tr>
<tr>
<td>Data from inner TGC</td>
<td></td>
</tr>
</tbody>
</table>

96 bit [Header&trailer] 
+ (256 + 192 + 32) × 4 
+ (1152 + 192 + 96 + 200 + 32) × 10^{-3} 
= 1922 bit/event/board