



LHCb MiniDAQ Control System CHEP 2018

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Outline

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- Experiment Control System (ECS)
- FSM
- MiniDAQ
- fwMiniDAQ
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- Integration
- Features
- Summary

Motivation

LHCb upgrade (starting 2018)

- Bottleneck LO trigger will be removed
 - Reduced the data from 40MHz to 1.1MHz
- Trigger-less readout
- Full software trigger
- New/upgraded sub-detectors
 - New electronics to cope with the new data rate
- New readout system

→Upgraded Experiment Control System (ECS)



Current Experiment Control System

- LHCb has designed and implemented a coherent and homogeneous control system
- Controls the complete experiment
 - Run Control, DCS, ...
- Is operated by only 1 person
- Is almost completely automated



LHCb Control System Size Picture: Courtesy of the CMS DCS Team

Experiment Control System (ECS)

Based on WinCC OA 3.15 SCADA

- Provides the UI, archiving, drivers, alarm-handling, ...
- Allows for custom developments
- Panels
- Scripts/Libraries
- Managers/Drivers
- Developments can be packaged and distributed
 - Components
- CERN JCOP Framework
 - Provides a set of WinCC OA components
 - Provides guidelines for component/application developments
 - Common components for common devices
 - Cooling and Ventilation
 - ELMBs
 - Power supplies

ECS Finite State Machine (FSM)

- LHCb Control System modelled with an FSM tree
- Actions propagate down the tree, states propagate up the tree
- 2 type of Units
 - Control Units
 - Nodes that logically group other nodes
 - State depends on the nodes below
 - Can be partitioned
 - Device Units
 - Nodes that correspond to a real device (HW/SW)
 - State depends on the real state of the device
 - Perform "real" actions



ECS Run Control

- LHCb is composed of multiple Sub-detectors
- Each Sub-detector can be run independently in a partition
- Each partition is controlled by a Run Control
- Run Control manages the whole FSM hierarchy of a SD
 - makes sure it's ready for data taking
- A global Run Control is used for global operation
 - Controls all the sub-detectors and systems

MiniDAQ

- Development server for the upgrade
 - Each SD has 1+ for developments
 - Contains 1 PCIe40 board
 - PCle board with a programmable FPGA
 - Provides the readout board (TELL40), a readout supervisor (SODIN) and an interface board (SOL40)
 - Stand-alone system
- Basic component of the upgrade
- Needs a Control System



fwMiniDAQ component



- Pre-configured Run Control FSM
- Pre-configured with all the necessary instantiated devices for a running system
 - Front-End electronics excluded as they're specific for each SD
- Once installed, little configuration is needed for a running system

fwMiniDAQ Readout board - TELL40

Pre-instantiated TELL40 (readout board)

X Status Data

Messages

- Full control for the TELL40
 - Configure all the parameters
 - See all data links status
 - Inject data into the memory
 - Memory snooping
 - Hooks for SD specific functionalities

	TELL40_Dev1_1: TOP (MINIDAQ2_2 - I	MINIDAQ2; #2) X		
Device TELL40_Dev1	State	Fri 29-Jun-2018 15:43:48	-	
tatus Data Format LLI Decod	ding Alignment TFC Processing Data Processing	Event ID Injection Bypass Memory Monitoring		
Data Format Fixed Data Format Fixed Data Format Order First E FE Data Transmission Protoc Wide	header / Fixed Lenth 00000004 XXD in MSB 0000001 Bus 00000070			
Header Information		TELL40_Dev1_1: TOP (MINIDAQ2_2 - MINIDAQ2; #2)	_ ×	
BXID field size	Device S	State	Fri 29-Jun-2018 15:43:52	
Use data length field size	TELL40_Dev1_1 RU	annus - 🗸 🛣		
Others	Status Data Format LLI Decoding Alignment	t TFC Processing Data Processing Event ID Injection Bypass	Memory Monitoring	
5111C Pattern	Summary			
Channel size	Dec Blocks State Error			
No of channels NZS frame size	Block 0 Not Active Not A Block 1 Not Active Not A Block 2 Not Active Not A	TELL40_Dev1	_1: TOP (MINIDAQ2_2 - MINIDAQ2; #2)	_ ×
Active fibers	Block 3 Not Active Not A Block 4 Not Active Not A Block 5 Not Selected Not S	Device State	Fri 29-Jun-2018	15:43:56
Fibers to align	Block 6 RUNNING OK Block 7 RUNNING OK Block 9 RUNNING OK			
MiniDAQ 2 Instan	Block 9 RUNNING OK Block 10 RUNNING OK	Status Data Format LLI Decoding Alignment TFC Proces	ssing Data Processing Event ID Injection Bypass Memory Monitoring	
	Block 12 RUNNING OK Block 13 RUNNING OK	Decoding Block 6	FIFOs	
	Block 14 RUNNING OK Block 15 Not Selected Not S Block 16 RUNNING OK	Synchronization Valid Frames Idle Frames	Mac1/255	
	Block 17 Not Selected Not S Block 18 Not Active Not A Block 19 Not Active Not A	Events Processed 3'507'852'229 Events Valid 3'506'124'139	Avg: 9	
essages	Block 20 Not Active Not A Block 21 Not Active Not A Block 22 Not Active Not A	Events Error 1 SYNC Frames 10		
	Block 23 Not Active Not A	NZS Frames 0	Data dec Info data dec	
		Current BXID 2510	TELL40_Dev1_1: TOP (MI	NIDAQ2_2 - MINIDAQ2; #2) _ ×
		Errors	Device State	Fri 29-Jun-2018 15:44:01
		BCID only 0	TELL40_Dev1_1 RUNHING - V	
		Parameters 0 BCID comparison BCID order 0 A 1	Status Data Format LU Decoding Alignment TFC Processing Data	Processing Event ID Injection Bypass Memory Monitoring
		BCID desync 0 BCID sync 1	Options Unk Selection:	Current Configuration
		Debug Sync OFF	Auto Write 📄 Write Manually	Loop Status No Loop Write Status and write
	Messages	IDLE Frames 1'115 Valid Frames 40	Mem Write False 🛛 💷 Mem Write True	and a second sec
		Sync ON IDLE Frames 0	From data_valid Specific Pattern From Spec Pattern From Pattern not 0	Start From data_valid
		Valid Frames 3'506'970'076	Frame Pattern	Write on Mem option
			Mask FFFFFFFF FFFFFFFF FFFFFFFF Apply	Write on Ris edge
			Write on Ris Edge 🛛 🗁 Write on ON	Write Signal Status
		Messages	Reset Write Signal	Selected Fiber
			Source LLI -	Source LL
			1 #1 #2 #3 #4 SBB 00000000 0000000 00000000 00000000	Memory
			992 00000000 0000000 0000000 0000000 996 00000000 00000000 0000000 0000000 1000 0000000 0000000 0000000 0000000	Pointer
			1004 00000000 0000000 0000000 0000000 1008 0000000 0000000 0000000 0000000 1012 00000000 00000000 00000000 00000000	Export Table
			1016 0000000 0000000 0000000 0000000 1020 0000000 0000000 0000000 0000000	Open Table
			Messages	
				Close

fwMiniDAQ Timing and Fast Control

 Pre-instantiated Super ODIN (timing/trigger control) and 6 SOL40 Links (controls interface)

Me

- Full control for Super ODIN and SOL40
 - Trigger configurations
 - Sub-detector settings

Device State			Fri 29-Jun-2018	15:44:53			
Link1 RUNNING	▲ ∨						
icoNamo:			Version D	ate			
IIDAO2 2:SOL 40 GBTtest Link1			5.01.02 201	71220.00			
Command SM] [Co.	unters				
	BXID R	eset	16	76047			
40 ···> SODIN Delay 0	0						
40> TELL40 Delay 0	0						
40> FE Delay 0	0 EID Re	set		2			
> SOL40 Delay 0	0 FE Res	set		2			
Apply			SODIN_GBTte	st/Core0: TOP (MINIDAQ2_2 - MII	NIDAQ2; #2)	-
							Fri 29-Jun-2018 15:44
x address 0x1	CERNY	Device	State	- / A			111 20 041 2020 2011
mmands FIFO flags Responses FIFO flags Apply	M	00100					
detector Type Test	MINIDAQ2_2:SC MINIDAQ2_2:SC	DIN_GBTtest.C DIN_GBTtest.C	ore0 ore0			Ve	rsion Date 5.00.06 20171220.00
B GBT slave PRBS e-links e-links tuning Olick letur	Status/Enables	Trig Monitoring	Cmds Monitoring	Trig Config Crr	nd Config		
		Statistics	and status			TFC Enables 1	TFC Enables 2
commands from external ODIN Enb O Apply	Orbits	1398940	Periodic Trin A	0	0.00 kHz	Periodic Trg 1	✓ Snapshot
	Bunch IDs	0x2FA	Periodic Trig. R	0	0.00 kHz	Fast Periodic Trg 1 O	Synch
FE generator	Event ID	1000	Calib. Trig. A	2797894	25.21 kHz	Periodic Trg 2 Fast Periodic Trg 2	BX Veto
(23 -> 0) 000000000000000000000000000000000	Total Triggers	1001	Calib, Trig, B	0	0.00 kHz	Calibration Trg A	✓ Header Only
imit # events	Trigger Rate	0.00 kHz	Calib. Trig. C	0	0.00 kHz	Calibration Trg B C	V EVID Cnt
	Gated Triggers	1000	Calib Trig. D	0	0.00 kHz	Calibration Trg D	MEP Dyn Dest
LDB GBTX Test GBT Logic	Gated Tro Rate	0.00 kHz	Random Trig. A	0	0.00 kHz	Random Generator	▼ BX Type
	Inst Tra Loss	0.100 %	Random Trig. B0	0	0.00 kHz	Random Trg B	✓ Throttle
ages	Synch	20	Random Trig. B1	0	0.00 kHz	Random Trg D	✓ NZS/IAE throttle
-	Snapshot	99	Random Trig. B2	0	0.00 kHz		BE Reset throttle
	BY VETO	0	Random Trig. B3	0	0.00 kHz	NZS Mode O NZS Consecutive	MEP throttle
	BA VEIO	689067525	Random Trig. C	0	0.00 kHz	🗌 Lumi Trg 🔷 🔾	FE Reset VETO
	NZS Mode	0	Random Trig. D	0	0.00 kHz	External trigger	SYNCH VETO
	EE Basat	2	External Trig	690849524	44921.38 kHz	L0 trigger	External TFC
	PE Reset	2	Physics	0	0.00 kHz	Ext trg edge select	Rate throttle
	BE Reset	2	MER Accented			Ext trg edge enb O	Ext EviD Rst
	FID Reset	2	ALL Accepted	1000	0.00 KHz	Scan Enb O	Ext EvID Match
	Throttle	689067526	UTC time start run	1970.0	1.01 01:00:00.000	Apply Enables	Apply Enables
		Ful Reset	Regs Reset	Logic Reset	Stop RUNNING	Counter Reset Single shi	ots
	Messages						

fwMiniDAQ Event Writer

- 1 Event writer controller
- Start/stop synchronously

	Device	State		Fri 29-	Jun-2018 15:45:14
ÉRN X	Ibminidaq2-02	RUNNING	▲ ×		
Command /usr/bi	n/pcie40_daqserver				Set
Output path	/tmp		Set		
Maz size (bytes)	16384		Set		
Buffer blocks	0		Set		
ssages					

Open 👻			pcie40_20180629_154220_main_slot_05000_link_0_run_0.dat							Save				- 1		_												
											/tm	1p	_															
1 Openin	ng f	ile p	cie40_	20180	J629_	154220	_mair	_slo	ot_05	5000)_li	nk_	0_ru	ın_(0.f	rg												
2 -110 1	nead	er:	1																									
3 For	mat	versi	on: 1	-	15.40		10																					
4 11m	esta	mp:⊩	ri Jur	1 29 .	15:42	:20 20	18																					
5 Str	eam	type:	MAIN	000		~																						
5 SUD	dete	ctor	type:	UXUUI	30000	9																						
/ Sen	der:	slot	05:00	1.0, 1	LINK	Θ.																						
8 Reci	eive	r: LD	minida	1q2-04	z.cer	n.cn																						
9 51Ze:	0.0	0 618																										
11 MED.	10.6		/ 1	700																								
11 MEP: .	13 1	ragme	nts (1	.768 [oytes	1	DVT	0.10	· · ·			10	c															
12 EVID:			BXID:	1/98	, GUL	:1000,	BTIE	5:12	9 (*	4 nc	1F +	12	5 G	ita.)	~ ~				~~	~~	~~	~~	~~	~~	~~	00	
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4 0x002	0		00 00		30 00	00 00	00 0	0 00	000	00	00	00	00 0	10 0	00	00 0	0 0	00 00	00	00	00	00	00	00	00	00	00	1
.5 0x004	0		00 00		30 00	00 00	00 0	0 00	000	00	00	00	00 0	10 0	00	00 0	0 0		00	00	00	00	00	00	00	00	90	1
6 0X006	0	00 00	00 00	1000	30 00	00 00	00 0	0 00	000	00	. 00	00	00 0	10 0	00	00 0	000	00 00	00	00	00	00	00	00	1			
L/EVID:		1,	BXID:	16	, GDL	:1000,	BYIE	S:12	9 (4	4 ho	ir +	12	5 da	ita)													
18 0X0001	0	00 10	10 10	/ 10 1	10 10	10 10	10 1	0 10	10	61	01	91	01 0	11 (91	01 0	11 0	1 01	01	U1	00	10	10	10	10	10	10	1
9 0x002	0	10 10	10 10	/ 10 .	10 01	01 01	01 0	1 01	. 01	01	01	01	01 0	91 (90	10 1	.0 1	0 10	10	10	10	10	10	10	10	10	01	1
20 0x004	0	01 01	01 01	. 01 (31 01	01 01	01 0	1 00	9 10	10	10	10	10 1	.0	10	10 1	.0 1	0 10	10	01	01	01	01	01	01	01	01	1
21 0x006	0	01 01	01 01	. 00 .	10 10	10 10	10 1	0 10	9 10	10	10	10	10 0	91 0	91	01 0	01 0	01 01	01	01	01	01	01	01				
ZEVID:		<u>ک</u> م	BXID:	1/98	, GUL	:1000,	BILE	5:12	9 (4	4 no	1r +	12	5 08	iτa)	~~ /		-		~~	~~	-	~~	~~	~~	~~	-	
3 0x000	0	00 20	20 20	1 20 2	20 20	20 20	20 2	0 20	20	02	02 1	02	02 0	12 0	92	02 0	12 0	2 02	02	02	00	20	20	20	20	20	20	
24 0x002	0	20 20	20 20	1 20 2	20 02	02 02	02 0	2 02	2 02	02	02 1	02	02 0	12 0	90	20 2	20 2	20 20	20	20	20	20	20	20	20	20	02	
25 0x004	0	02 02	02 02	. 02 (JZ UZ	02 02	02 0	2 00	20	20	20 .	20	20 4	0	20	20 4	0 4	20 20	20	02	02	02	02	02	92	02	02	1
26 0X006	0	02 02	02 02	00	20 20	20 20	20 2	0 20	20	20	20 :	20	20 0	12 0	92	02 0	12 6	12 02	02	02	02	02	02	02				
27 EVID:		J,	BXID:	16	, GDL	:1000,	BAIF	5:12	9 (4	4 no	1r +	12	5 08	ita.)					~~	~ ~	~ ~	~ ~	~ ~	~ ~	~ ~	~ ~	
28 0X0001	0	00 30	30 30	1 30 :	30 30	30 30	30 3	0 30	30	03	031	03	03 0	13 (93	03 0	13 0	13 03	03	03	00	30	30	30	30	30	30	1
29 0x002	0	30 30	30 30	1 30 :	30 03	03 03	03 0	13 03	3 03	03	031	03	03 0	13 (00	30 3	10 3	30 30	30	30	30	30	30	30	30	30	03	1
30 0x0041	0	03 03	03 03	; 03 (33 03	03 03	03 0	13 00	30	30	30	30	30 3	30	30	30 3	10 3	30 30	30	03	03	03	03	03	03	03	03	1
31 0X006	0	03 03	03 03	, 00 :	30 30	30 30	30 3	0 30	1 30	30	30.	30	30 0	13 (93	03 0	13 0	13 03	03	03	03	03	03	03	1			
32 EVID:		4,	BXID:	1/98	, GDL	:1000,	BYIE	S:12	9 (4	4 nc	1r +	.12	5 08	πa)				~ ~	~ 4	~ ~		40		4.0			
33 UXUUU	0	40 40	40 40	/ 40 4	+0 40	40 40	40 4	40	40	04	04	04	04 0	14 (04 00	4 0	14 0	14 04	04	04	00	40	40	40	40	40	40	1
34 0X0020	0	40 40	40 40	1404	10 04	04 04	04 0	4 04	104	04	04 1	04	04 0	14 (00	40 4	10 4	10 40	40	40	40	40	40	40	40	40	04	1
35 0X0041	0	04 04	04 04	. 04 (14 04	04 04	04 0	4 00	40	40	40 4	40	40 4	0	40	40 4	10 2	10 40	40	04	04	04	04	04	04	04	04	1
36 0X006	0	04 04	04 04	, 00 4	10 40	40 40	40 4	0 40	1 40	40	40 4	40	40 0	14 (94	04 0	14 0	14 04	04	04	04	04	04	04				
37 EVID:		5,	BXID:	16	, GDL	:1000,	BYIE	5:12	9 (4	4 nc	1r +	12	5 08	πa)				0.5	05	~~							
38 0X000	0	00 50	50 50	150 5	30 50	50 50	50 5	0 50	50	05	05 0	05	05 0	15 1	95	05 0	15 0	15 05	05	05	00	50	50	50	50	50	50	1
39 UXU020	0	00 DC	DU 50	50 5	20 05 05 05	05 05	05 0	5 05	0 05	05	05	05	05 0	00	00	50 5	0 5	0 50	50	50	50	50	20	20	20	50	05	1
40 0X0041	0	05 05	05 05	05 0	30 US	05 05	05 0	0 00	50	20	50	50	50 5	00 5	00	50 5	0 5	00 50	50	05	05	05	05	05	5	05	50	1
41 0X006	0	05 05	05 05	1700	20 50	50 50	50 5	0 50	1 50	50	50	50	50 0	15 (05	05 0	15 (15 05	05	69	05	69	69	05	1			
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13 UX0001	0	00 60	00 60	1 60 6	JU 60	00 60	00 0	0 60	00	90	00	00	00 0	10 (00	00 0	0 0	10 00	06	06	00	60	60	00	60	00	00	1
14 UX002	0	00 00	00 00	00 0	30 06	00 00	06 0	00 00	00 00	00	00	00	00 0	10 (00	00 0	0 0	0 60	00	00	00	00	00	00	00	00	00	1
45 UXU041	0	00 06 00 00	05 06	000 0	30 06	05 06	06 0	00 00	1 60	60	00	00	00 6	006	00	00 6	0 6	00 60	60	06	06	06	06	06	96	06	90	1
40 UXU06	0	00 00 7	05 06	000	JU 60	00 60	50 6	0 60	1 60	60	00	00	000	10 (90	00 (0 0	00 06	06	96	06	06	06	96	1			
47 EVID:		· · ·	RXID:	16	, GUL	:1000,	BALE	5:12	(9 (4	+ no	1r +	12	5 da	ita	1					07	00	70	70	70	70	70	70	
48 0×0001	0	00 70	/0 70	/ /0 /	/0 70	/0 70	/0 7	0 70	9 /0	07	0/1	9/	0/0	1/ (9/	0/ 0	1/ 0	07	07	07	00	/0	/0	/0	/0	/0	/0	1
49 0x002	0	/0 70	/0 /0	/ /0 /	/0 07	0/ 0/	07 0	/ 07	0/	07	0/1	9/	0/0	1/ (00	10 7	0 /	0 70	/0	/0	/0	/0	/0	/0	/0	/0	07	1
50 0x004	0	0/0/	0/ 0/	0/0	3/ 0/	0/ 0/	0/0	00	1 /0	/0	/0	70	/0 /	. 0	/0	10 1	0 /	0 70	/0	0/	07	0/	0/	07	6/	07	6/	1
51 0X006	0	0/0/	0/0/	00	/0 /0	/0 /0	/0 /	0 /0	1 /0	/0	/0	/0	/0 0	1/ (9/	0/ 0	17 6	17 G)	0/	0/	0/	0/	0/	0/				
SZ EVID:		8,	BVID:	1/98	, UDL	:1000,	BYIE	5:12	:9 (4	+ nc	11. +	12	D da	ita,)													

fwMiniDAQ Top panel

- Check the readiness of the system
- Quickly configure your system
- Quickly change your settings

Tella0: HMTUPAC2 2:TELL40 09 MMTUPAC2 2:TELL40 09 MMTUPAC2 2:TELL40 09 MMTUPAC2 2:Tell40 17 MMTUPAC2 2:Tell40 19 Set TOP: MMTUPAC2 2:TOP 09 MMTUPAC2 2:TOP 09 MMTUPACA 2:TOP 00 MMTUPACA 2:TOP 00 MMTUPACA 2:TOP 0	Add Del Sub Unsub	SODIN: MINIDA02 2:SODI MINIDA02 2:Sodir MINIDA02 2:sodir MINIDA02 2:sodir MINIDA02 2:LLI 0 MINIDA02 2:LLI 0 MINIDA02 2:LLI 0 MINIDA02 2:LLI 0 MINIDA02 2:LLI 0	9 BRest 000	Add Del Sub Unsub	SOL40: MINDAQ2 2:501 MINDAQ2 2:301 MINDAQ2 2:301 MINDAQ2 2:301 MINDAQ2 2:301 MINDAQ2 2:301 MINDAQ2 2:20 MINDAQ2 2:0 MINDAQ2 2:0	40 09 40 09Test 10 17 MINIDAQ Link 0 Link 1 Link 2 Link 3 Link 4 Link 5 Link 6 Link 7 Link 8 Link 9	Add	P_GBTtest.Top -2033326601 2518501048 2337341916 2337341983 2351933057 2337341953 2337341953 2337341919 2337341919	Link 12 Link 13 Link 14 Link 15 Link 16 Link 17 Link 18 Link 19 Link 20 Link 21	Corr	nmands (MINIDAO2 2337341842 2337341842 2337341825 2337341802 2337341802 2337341803 2518447221 2337341813 2518437517 251843894 2518428073 2518428073 2518424249	2- 2 - MINID Js and Cou Link 24 Link 25 Link 26 Link 27 Link 28 Link 30 Link 31 Link 32 Link 33	AQ2; # Inters - ([(] (] (] (] (] (] (] (]	2218412613 2518406793 2518406793 2518404978 2518404978 2518309729 2518393729 2518393729 2518395775 2518381945 2518377762	Link 36 Link 37 Link 38 Link 40 Link 41 Link 42 Link 43 Link 44 Link 45	 Rese 0 <li< th=""><th>t All Counters 2518363256 2518355408 2518355756 2518351736 251834733 2518344080 251833902 251833602 25183328412</th><th>×</th></li<>	t All Counters 2518363256 2518355408 2518355756 2518351736 251834733 2518344080 251833902 251833602 25183328412	×		
Set			Set			Link 10	•	2337341919	Link 22	•	2518420282	Link 34	•]	2518373962	Link 46	•	2518324595			
Writers: Ibminidag2-02 Ibminidag2-09		Known GBT Server Ibdagesc8000 Ibminidag2-02	·					MiniDAQ: TOP (MIN	IIDAQ2_2 - MII	VIDAQ	2; #2)				- ×	•	2518320771			
Ibminidaq2-17	Add	lbminidag2-08 lbminidag2-09 lbminidag2-17	GERNY		System	Stat	e							Fri 29-Jun-2018	15:42:36		Close	5		
	Del Sub	pclhcb195	M		MiniDAQ	RUNNI	IG -													
	Unsub		Sub-Sy	/stem Q	State RUNNING	-	Svste	System Status												
			ME	P	RUNNING	System Status														
			TFO	c	RUNNING	- 8	GB1													
· · · · · · · · · · · · · · · · · · ·			MiniDAQ_	Runinfo	RUNNING	- /	Re	gisters Subscription	Configu	re Subs	scriptions		TELL	40 500	DIN					
								Ctri Managers	Resta	art Ctrl M	lanagers									
								Test System	Exp	ort Syst	em Info									
								.40												
							Co	nfigure Links	Status											
							Tri	iggers from TFC: 1'00	0											
							EV	vents Accepted:												
							S	SODIN Master MINIDA	Q2 2:SODIN 0	BTtest										
							TFC	Master Links MINIDA		.Link0										
TFC quick control Click to disable ALL FE																				
All Subdetector Type Multiple> Multiple>																				
							Other	r Devices												
							prbs	s_8000 👻 🗆	LI PRB	S	RXReady									
							Step	Run				а								
							E	nabled	No of	triggers	:: [10000									
							Curr	rent step:	End step:		Apply									
														FW Version	ns					
			Messages																	
															Close					

fwMiniDAQ/fwMiniDAQ_configureMulti.pnl (MINIDAQ2_2 - MINIDAQ2; #2)

Domains

- Several domains are provided in the component
 - DAQ
 - TFC
- Provide all the required states and transitions
- Provide automation
- The same for all the Sub-Detectors
- Facilitate integration

DAQ Domain







Integration

- The domains implemented on fwMiniDAQ serve as the base for the final upgrade system
- Templates are distributed to all the Sub-detectors
- Make the system homogeneous and coherent
- DAQ domain will be exactly the same
- TFC domain will remain the same but will be moved to the global Run Control hierarchy
- fwMiniDAQ component probably be split into several independent WinCC OA components
 - fwTell40
 - fwTFC
 - IbDomains

Other Features

- Usage of Recipes
 - Named sets of configuration
 - Applied depending on the requirements at a given time (e.g. PHYSICS, CALIBRATION, ...)

SCAN runs

- Runs with a set number of steps, each with a set limit of triggers
- Between steps, settings are changed on the devices
- Find the best settings for each application
- Autopilot
 - Base for automatic actions

Summary

- The fwMiniDAQ provides an easily installable and configurable component for the MiniDAQ
- Speeds up testing and development by the Sub-detector teams
 - Can concentrate on the SD specific parts
- Provides several helpful features
 - SCAN runs
 - Recipes
- Serves as base for the future central ECS
- Makes the system homogeneous from early stages of development
- Support and training is easier